TI

THUNDERBIRD TAS5100EVM

Evaluation Module for the TAS5100 Digital Audio PWM Power Output Stage

Preliminary User's Guide

February 2002 *Digital Audio/Application*

Claus Reckweg

SLEU009A

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60C. The EVM is designed to operate properly with certain components above 60C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This manual describes the operation of the TAS5100EVM evaluation module from Texas Instruments.

How to Use This Manual

This document contain the following chapters:

- Chapter 1 – Introduction.
- Chapter 2 – Description of the EVM board.
- Chapter 3 – EVM board operation overview.
- Chapter 4 – Hints for measurements of performance.

Information about Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION
This is an example of a caution statement. **A caution statement describes a situation that could potentially damage your software or equipment.**

WARNING
This is an example of a warning statement. **A warning statement describes a situation that could potentially cause harm to you.**

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related documentation from Texas Instruments

The following is a list of data manual that have detailed descriptions of the integrated circuits used in the design of the TAS5100 EVM. The data manuals can be obtained at the URL http://www.ti.com.

Part Number	Literature Number
TAS5001PFB	SLES009
TAS5010PFB	SLAS328
TAS5100DAP	SLLS419b
TAS3002PFB	SLAS307b
DIR1703E	SLES007
LMV311IDBVR	SLCS136d
SN74LVU04APWR	SCES130e
SN74LVC1GU04DBVR	SCES215h
SN74AHC1G08DBVR	SCLS314h
SN74LVC08APWR	SCAS283g
SN74LVC1G14DBVR	SCES218f
SN74LVC1G32DBVR	SCES219e
SN74LV123APWR	SCLS393e
SN74LV132APWR	SCLS394d
TPS3705-33DGN	SLVS184b
TPS75333QPWP	SLVS241a
TPS76433DBVR	SLVS180b

Additional TAS5100EVM documentation

The CD-ROM attached the TAS5100EVM package include the following documentation:

- TAS5100EVM User's Guide, Literature No. SLEU009 (this document)
- TAS5100EVM Design Document, Literature No. SLEU010 (schematic, parts list, PCB layout)
- TAS5100EVM Data Report, Literature No. SLEU011 (audio performance and efficiency)
- TAS5100EVM EMI Test Report, Literature No. SLEU012
- TAS5100EVM Gerber Files
- Audio Precision Test Files (require AES17 filter installed at the measurement equipment)
- EQ-GUI Software and User's Guide
- Application Notes
- Data Manuals

Photograph of TAS5100EVM

Figure 1-1: Components included in the TDAA reference design are surrounded with a white line on the PCB.

Contents

1. INTRODUCTION

The TAS5100 customer evaluation module (EVM) is demonstrating two integrated circuits TAS5010 and TAS5100 from Texas Instruments (TI). The TAS5010 is a cost-effective, high performance 24-bit stereo digital modulator based on Equibit™ technology. This IC converts input PCM serial digital audio data to a Pulse Width Modulated (PWM) audio data stream. The TAS5010 PWM modulator accepts sample rates up to 192 kHz. Maximum sample rate for the TAS5001 is 96khz. Pin-outs are identical for both modulators. The TAS5010 is designed to implementation together with the TAS5100 true digital output stage for driving a loudspeaker.

Together the TAS5010 and two TAS5100 provide the complete conversion of a 3.3 volts digital audio input stream into 30 watt for loudspeakers in the 4 to 8 ohm impedance range. The chipset is ideal for applications requiring excellent audio quality, minimum size and weight, and high power efficiency. The chipset can be used in a range of products such as micro-components systems, home theater in a box, DVD receivers, or TV sets.

The TAS5100EVM is a complete true digital amplifier including S/DIF receiver, I2S audio interface, volume control, interface to personal computer through the parallel port, and required control logic. The TDAA reference design is surrounded with a white line on the PCB.

TAS5100EVM Features

- TDAA reference design (double-sided plated-through PCB layout).
- S/PDIF receiver with coaxial and optical input (Sampling rate: 32kHz – 96kHz).
- I2S audio interface (Sampling rate: 32kHz – 192kHz).
- On board volume control.
- Auto-mute function.
- Self-contained protection system (short circuit & thermal).
- Digital Audio Processor (DAP), which include 24 bit volume control, digital gain, bass and treble control, parametric equalization, dedicated speaker equalization, loudness control, and adjustable dynamic range compression/expansion.
- DAP control through PC software (GUI software from TI).
- Default DAP settings is downloaded to an EEPROM with the GUI software.
- Analog line input (use internal analog-to-digital converter in DAP).
- Analog line output (use internal digital-to-analog converter in DAP).

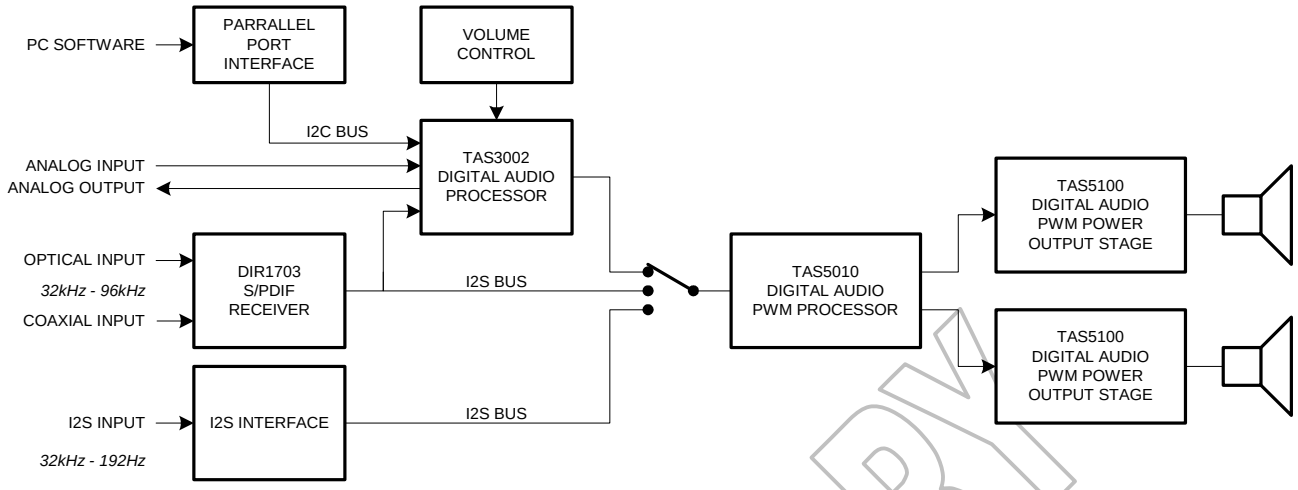

Figure 1-1: Simplified TAS5100EVM Block Diagram

The DIR1703 IC from Burr-Brown is used as S/PDIF receiver and system clock generator. This product is a Digital audio Interface Receiver (DIR) which receives and decodes audio data up to 96kHz sampling rate. DIR1703 is running in a configuration where it automatically switches between PLL-mode and crystal-mode. When the DIR1703 is connected to an active digital source, it is running in PLL-mode. System clock (SCKO) frequency depends on the incoming sampling rate (fs): SCKO = 256*fs. When no digital source is represented, the DIR1703 switches to crystal-mode. The system clock in crystal-mode depends on the external crystal. On the TAS5100EVM board the crystal-mode system clock is 12.288MHz.

Crystal-mode operation is used to generate a fixed clock when the TAS5100EVM board is connected to an analog source. The external anti-aliasing filter for the A/D-converter is optimized to the on board 48kHz sampling rate.

The TAS3002 IC from Texas Instruments is used as digital audio processor. All features in the DAP can be controlled through the I2C interface. Adjustment of sound level can both be executed through the I2C bus and with two push buttons on the EVM board.

During power-up the TAS3002 settings and coefficients are loaded from an external serial EEPROM. The TAS3002 coefficients control all features in the DAP. Customized start-up settings can be downloaded to the EEPROM. This operation is easy to execute with a personal computer, GUI software, a cable between TAS5100EVM and the computer. The TAS5100EVM is connected to the LPT-port at the computer.

2. Description of the EVM board

This chapter describes the TAS5100EVM board in regards to board layout, jumpers, switches, buttons and connectors.

2.1 Board outline with connectors, switches, jumpers & indicators

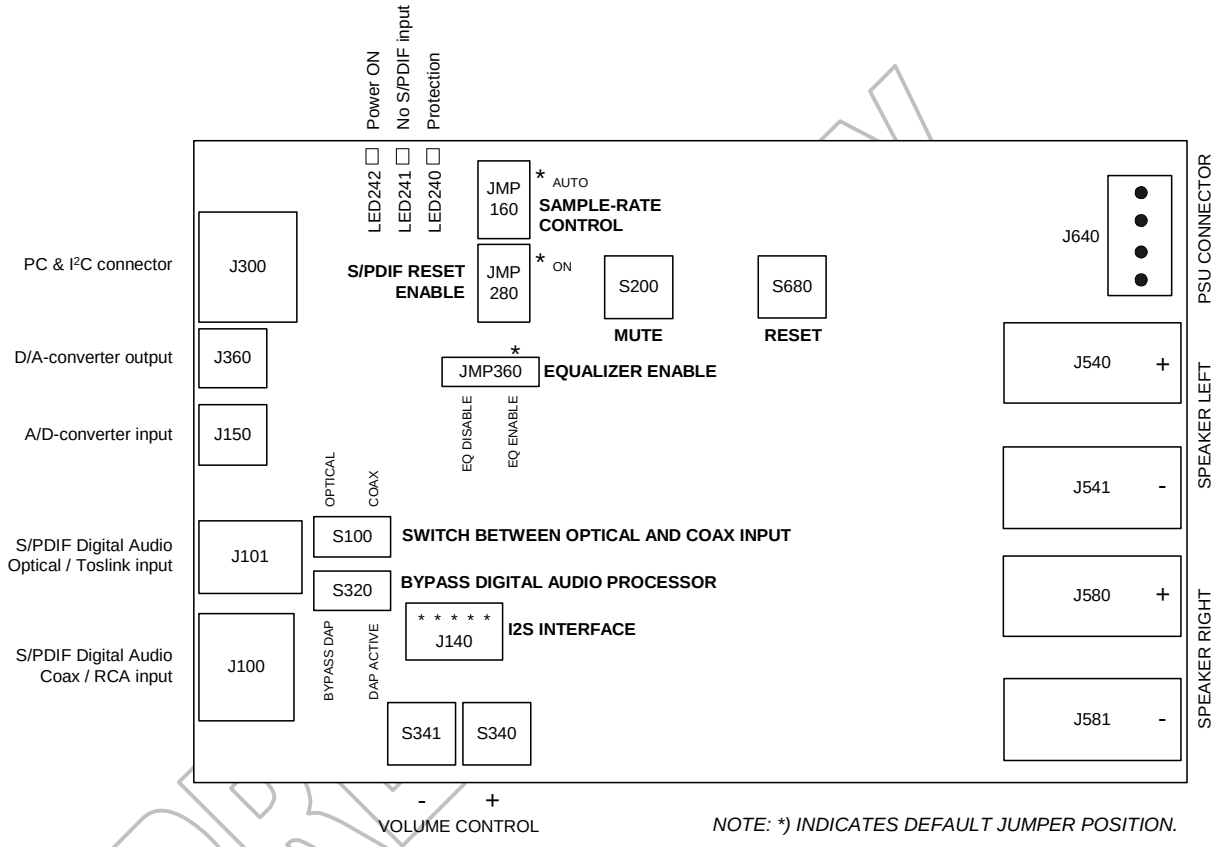

Figure 2-1: TAS5100EVM outline with reference-designators for connectors, switches, jumpers & indicators.

2.2 PCB key map

Physical structure for the TAS5100EVM is illustrated in Figure 2-2. Block headings refer to page headings at the TAS5100EVM schematic.

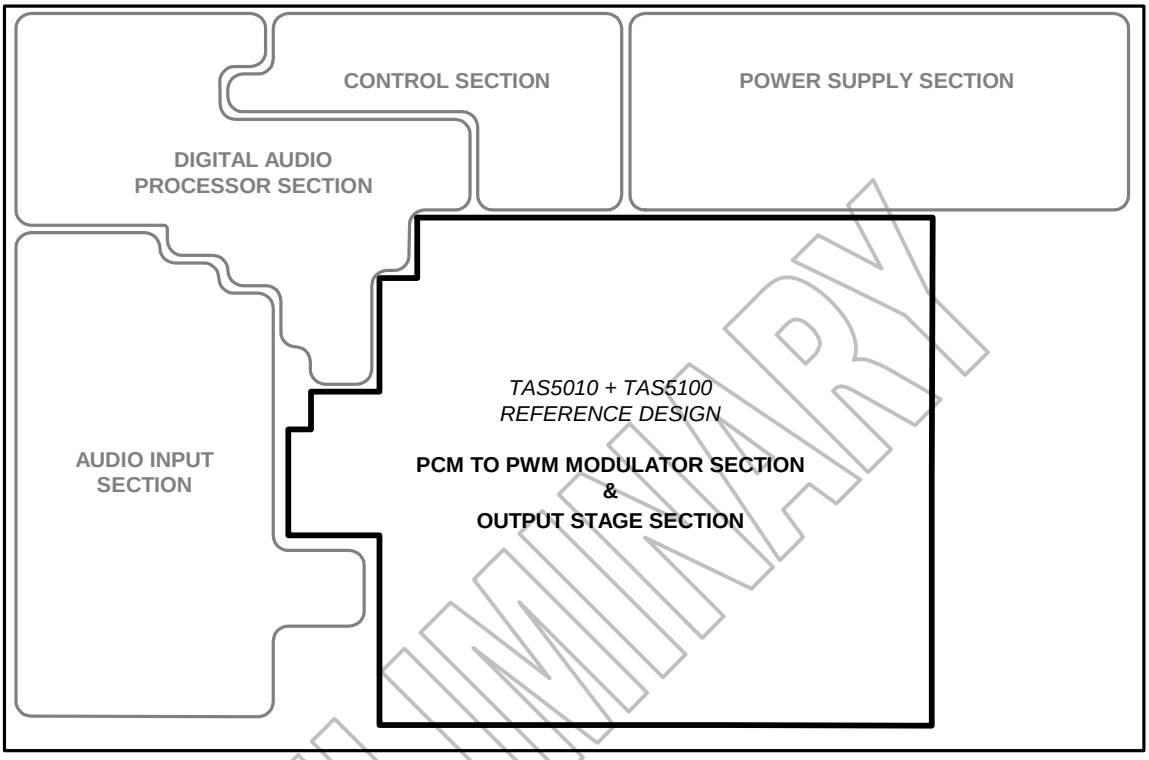

Figure 2-2: Physical structure for TAS5100EVM (rough outline).

2.3 Description of jumper settings

There are tree jumpers on the EVM board (J140 is a I2S interface – see description in section 2.4).

JMP160: Controls the double-speed pin at TAS51010

JMP160 is used to set the double-speed pin at TAS5010 (DBSPD, pin 39). If the DBSPD is connected to 0V, the TAS5010 is in single-speed mode. If DBSPD is connected to +3.3V, the TAS5010 is in double-speed mode. Single-speed is required for sampling rate at 32kHz, 44.1kHz, 48kHz & 192kHz. Double speed is required for 88kHz & 96kHz sampling rate.

The S/PDIF receiver automatically controls the DBSPD-pin if JMP160 shunts pin 1 and 2 (default setting). If JMP160 shunts pin 2 and 3, the TAS5010 is in single-speed mode. If JMP160 shunts pin 3 and 4, the TAS5010 is in double speed mode.

JMP280: Enable/disable UNLOCK signal from S/PDIF receiver

JMP280 is used to disable the "UNLOCK" warning signal from the S/PDIF receiver. The UNLOCK signal is high until the PLL in DIR1703 detects and locks on an incoming digital signal. The warning signal is used to shutdown the output stage (the H-bridge stop switching). To obtain click and pop reduced shutdown it is necessary to mute the output stage before reset on TAS5010 is pulled down.

When the EVM board is connected to an analog source or to a digital source through the I2S interface, is it necessary to disable the "UNLOCK" warning. This is done with the JMP280 jumper. When JMP280 shunts pin 1 and 2 the "UNLOCK" warning is enabled (default setting). If JMP 280 shunts pin 2 and 3 the warning signal is disabled.

JMP360: Bypass equalizer function in the Digital Audio Processor

JMP360 is used to disable the equalizer function in the DAP. The equalizer function is enabled if JMP360 shunts pin 1 and 2. The equalizer is disabled when JMP360 shunts pin 2 and 3.

Note: Bass- and treble-control is bypassed when equalizer is bypassed.

Default jumper positions

Default jumper positions are illustrated in Figure 2-3.

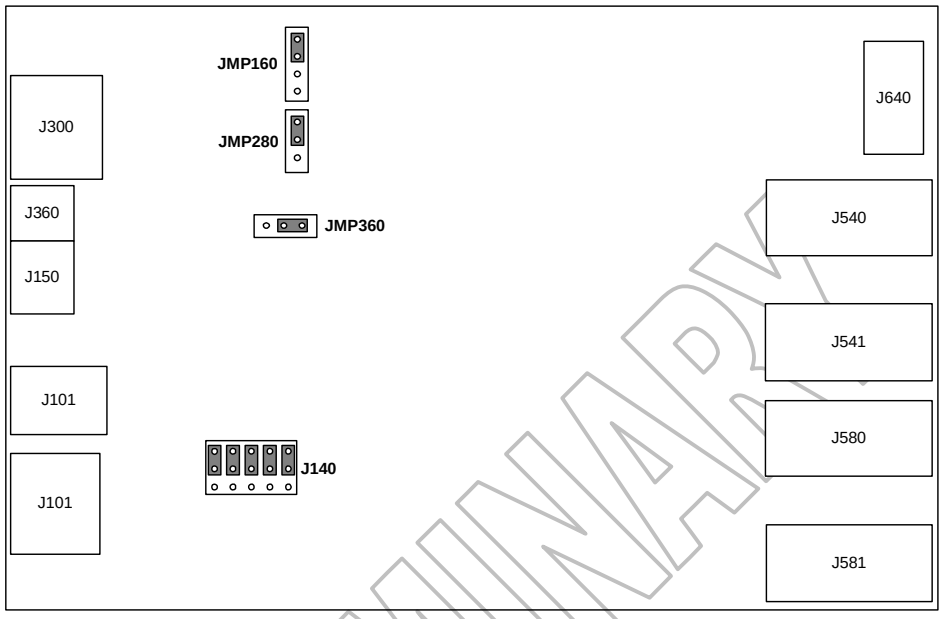

Figure 2-3: Default jumper positions.

2.4 Description of connectors

S/PDIF Digital Audio Coax/RCA input (J100)

The RCA connector can be connected to a digital S/PDIF source through a coaxial cable with 75 ohms characteristic impedance (e.g. RG59 cable). Maximum sampling rate at this input is 96kHz.

S/PDIF optical (J100)

The Toslink connector can be connected to a digital S/PDIF signal through an optical cable. Maximum sampling rate at this input is 96kHz.

I2S connector (J140)

I2S interface directly to TAS5010. Jumpers are needed for normal operation using S/PDIF input signal. When the I2S connector is used, the DAP is not in the signal path. Maximum sampling rate at this input is 192kHz.

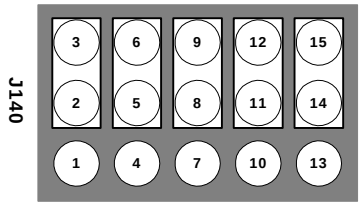

Figure 2-4: Pin numbers at I2S interface. Rectangles indicate default jumper positions.

Pin #	Pin description	Net name at TAS5100EVM schematic
2	System master clock input (256*f_s)	TA50XX-MCLK
5	Audio bit clock input (64*f_s)	TA50XX-SCLK
8	Left/right clock input (f_s)	TA50XX-LRCLK
11	I2S data input	TA50XX-SDATA
14	Reset output stage input (active low)	/RESET-I2S-INTERFACE
1,4,7,10,13	0 volt	GND

Table 2-1: I2S interface pin connections.

Serial Interface Adaptor SIA-2322 from Audio Precision can be connected to the I2S interface.
Note: Unlock signal from S/PDIF shall be disabled (JMP280) when the I2S interface is connected to an external source.

Analog input (J150)

Analog sources can be connected to the A/D-converter through J150. The analog line input is optimized for an input signal with a maximum voltage at $2.1V_{RMS}$.

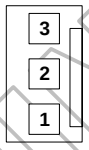

Figure 2-5: Pin numbers at line input connector and the line output connector (top view).

Pin #	Description
1	Left channel input
2	Ground
3	Right channel input

Table 2-2: J150 pin description.

Analog output (J360)

Analog output from the Digital Audio Processor is available at the connector. Maximum output level is $0.7V_{RMS}$. Pin numbers for J360 is equal to numbers at J150.

Pin #	Description
1	Left channel out
2	Ground
3	Right channel out

Table 2-3: J360 pin description.

PC & I^2C Interface (J300)

PC interface using attached special cable to parallel/printer port on PC. This makes it possible to control the TAS3002 Digital Audio Processor totally from the PC using the special EQ-GUI software saved on the TDAA CD-ROM.

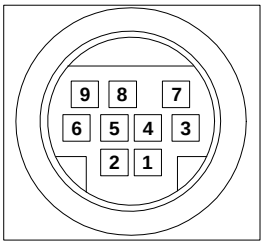

Figure 2-6: Pin numbers at Parallel Port Interface/I2C interface (J300).

Pin #	Pin description	I/O	Net name at schematics
1	Power ON Reset	Output	/POWER-ON-RESET
2	Serial Data Line (SDA)	Bi-directional	SDA-BI
3	Serial Clock Line (SCL)	Bi-directional	SCL-BI
4	Serial Data Line In	Input	SDA-IN
5	Serial Clock Line Out	Output	SCL-OUT
6	Not Used	-	-
7	Serial Data Line Out	Output	SDA-OUT
8	Serial Clock Line In	Input	SCL-IN
9	0 volt	-	GND

Table 2-4: J300 pin description. Pin 2 (SDA) & pin 3 (SCL) are used for communication between an external micro-controller and the Digital Audio Processor.

The connector can also be used to control the TAS3002 from an external micro controller of your own choice.

Loudspeaker connectors (J540, J541, J580 & J581)

All speaker connectors accept standard 4mm plugs. Use of high quality plugs and speaker cable is recommended.

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (eq. through an oscilloscope).

Pin #	Pin description
J540	Left speaker positive output terminal
J541	Left speaker negative output terminal
J580	Right speaker positive output terminal
J581	Right speaker negative output terminal

Table 2-5: Description of loudspeaker connectors.

Power Supply connector

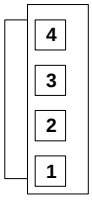

Figure 2-7: Pin numbers at PSU connector (Top view).

Pin #	Description	Net name at schematic
1	Supply voltage for output stage (VHBR)	POWER-OUTPUT-STAGE
2	Supply voltage for control and gate-drive (V+)	-
3	Ground	GND
4	Ground	GND

Table 2-6: J640 pin description

2.5 Description of switches and buttons

S/PDIF input selector switch (S100)

S100 switch between optical and coaxial S/PDIF input. When the lever is pressed in the direction of J101, optical S/PDIF input is selected. When the lever is pressed in the direction of the output stage, coaxial S/PDIF input is selected.

Bypass Digital Audio Processor switch (S320)

When the lever is pressed in the direction of J101, the DAP is bypassed. When the lever is pressed in the direction of the output stage, the DAP is in the signal path. Below S320 is a label (DAP ON), which indicate the position of lever, for DAP inserted in signal path.

WARNING CAUTION
Bypass DAP is equal to maximum output power (attenuation = 0dB). This might be very loud and could possible damage your loudspeakers and ears.

Reset board button (S680)

Reset board incl. TAS3002/DAP settings (volume = default programmed setting) at single push on button.

Mute button (S200)

The output stage mute when button is pressed down. Output stage un-mutes when button is released.

Volume control (S340 & S341)

S341 & S340: Volume control of TAS3002 DAP. Press and hold S341 button to decrease output power level. Press and hold S340 button to increase output power level.

Note: Change of listening level is very slow. It takes approximately 25 seconds to change attenuation from –70dB to 0dB.

The TAS3002 device implements a soft volume control. This feature allows a change from one volume level to another over the entire range of volume control (+18dB to mute). Above 0dB there is risk of signal clipping. Distortion of output signals is the result of signal clipping.

Note: Significant signal clipping might result in activation of the current protection system.

Description of indicators

Power ON LED (LED242)

Green LED indicates that the TAS5100 EVM board control circuit is powered on.

No S/PDIF input LED (LED241)

Yellow LED indicates that the S/PDIF input signal is missing.

Reasons to "No S/PDIF" warning:

- Lever at S/PDIF input selector switch (S100) is placed in wrong position.
- S/PDIF signal is missing. Some DVD players removes S/PDIF output signal when drawer is opened.

Note: When UNLOCK signal from S/PDIF receiver is disabled (JMP280 shunted pin 2 & pin 3), the "No S/PDIF" indication is disabled.

Protection LED (LED240)

Red LED indicates that protection circuit is engaged and the output is in shutdown mode.
Reasons to shutdown mode:

- Two speaker terminals are shorted.
- The amplifier is constantly overloaded (decrease volume level).
- Speaker terminal is shorted to ground (e.g. through an oscilloscope).
- Output stage is in thermal shutdown.

Please check setup and board carefully, and remove causing failure before pressing RESET (S680) to disengage protection mode.

3. EVM Board Operation Overview

This chapter describes the TAS5100EVM board operation.

3.1 Power the TAS5100EVM

The TAS5100EVM can be powered from one or two external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

Note: Length of power supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Power the EVM by one power supply

A single power supply can be connected to the TAS5100EVM board. Short VHBR and V+ at the power cable (red and white plugs).
Voltage for the connected power supply is not allowed to be below 18V. Maximum supply voltage depends of the speaker load resistance. Please check up the recommended maximum supply voltage in the TAS5100 datasheet.

	R_{LOAD} = 4 ohm	R_{LOAD} = 6 ohm	R_{LOAD} = 8 ohm
Supply voltage (VHBR & V+)	18 - 20V	18 - 23V	18 - 26V

Power the EVM by two external power supplies

When two supplies power the TAS5100EVM, it is possible to adjust the listening level with the level of the voltage "VHBR" (pin 1 at J640). Minimum VHBR voltage is 0 volt. Maximum voltage depends of the load resistance. Please check up the recommended maximum supply voltage in the TAS5100 datasheet.

	R_{LOAD} = 4 ohm	R_{LOAD} = 6 ohm	R_{LOAD} = 8 ohm
Maximum VHBR voltage	20V	23V	26V
V+ voltage	18V – 27V	18V - 27V	18V - 27V

Required power-up and power-down sequence

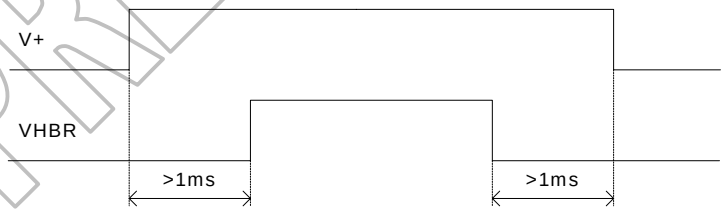

Figure 3-1: Recommended power-up & power-down sequence.

3.2 Setup TAS5100EVM with S/PDIF input.

Connect the EVM board as shown in Figure 3-2. Select between coaxial or optical input signal, at the input selector switch (S100).

Press lever at S320 in the direction of the output stage if TAS3002 DAP is wanted in the signal path (recommended during normal listening tests). There is no attenuation if DAP is bypassed. If the DAP is in the signal path, the start up volume level depends on what is programmed in the serial EEPROM on the EVM board. Default startup volume level is initially programmed to 12dB below full scale, which on some speakers still might be loud. Default volume level can be changed with the GUI software on the PC.

Note:

- All jumpers are in default position.
- Speakers, power supply, and if required cable for PC communication are initially connected to the EVM board.
- The TAS5100EVM can powered with either one or two power supplies (see section 3.1). Power Supplies are initially switch OFF.
- Music player is initially switch OFF.
- PC connection is optional.

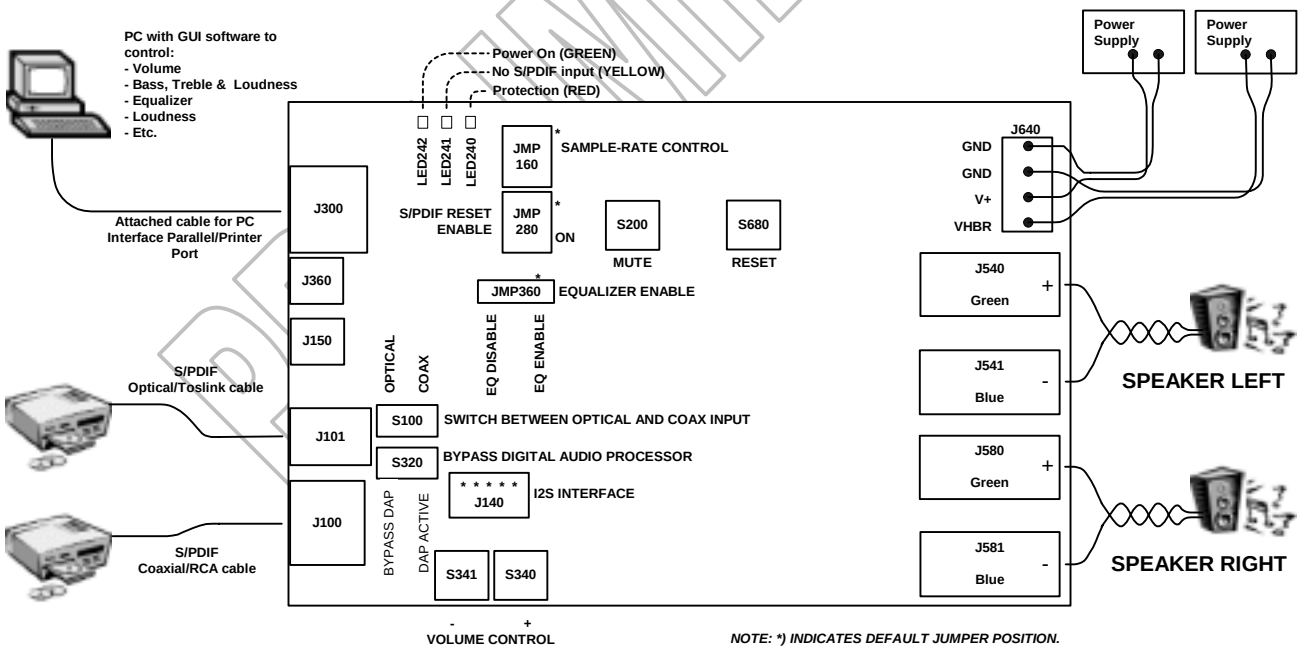

Figure 3-2: Board connected to S/PDIF sources & personal computer.

Startup sequence

1. Turn on power supply/supplies. Please follow the power-up and power-down sequence described in section 3.1. Observe that green "Power ON" LED and the yellow "No S/PDIF" LED are shining.
2. Run GUI Software (EQGUI.EXE) from PC desktop if the DAP is activated (S320) and the attached cable is connected from J300 to PC.
3. Turn on the CD/DVD-player and play the test CD. Observe that the yellow "No S/PDIF" now is OFF.

⇨ Observe Digital Audio coming from Left and Right Speaker.

3.3 Setup TAS5100EVM with analog line input

1. Disable "UNLOCK" warning from S/PDIF receiver (JMP280: jumper shunts pin 2 & 3).
2. Connect TAS5100EVM board and PC with the attached cable.
3. Connect analog source to analog input (J150).
4. Power-up the TAS5100EVM board.
5. Enable TAS3002 analog input with the EQ-GUI software.
6. Disable TAS3002 digital input (both SDIN1 & SDIN2) with the EQ-GUI software.
7. TAS5100EVM board is ready to play with analog source.

3.4 Interfacing the analog line output

Default is the analog line output (J360) active. The analog line output can be connected to analog tape recorders or analog amplifiers (e.g. subwoofer).

3.5 Controlling the DAP with PC software

Operating instructions for the EQ-GUI software are described in the user guide "Operating Instruction EQ-GUI X.X & Command Tool X.X" (X.X is the software version identification).

4. Hints for measurement of performance

Please read the application note 'Digital Audio Measurements' (TI literature number SLAA114) for an introduction to measurements on True Digital Audio Amplifiers.

You are welcome to use the Audio Precision test files available on the TDAA CD-ROM. Note that an AES17 filter is required to reach the shown measurements. Specifications for the AES17 filter are described in "AES standard method for digital audio engineering – Measurement of digital audio equipment " (AES17 standard is available from Audio Engineering Society – www.aes.org).

When evaluating the performance of the digital amplifier section, bypass the Digital Audio Processor with S320 or adjust all settings to neutral and attenuation to 0dB.

Connect the TAS5100EVM to a regulated power supply with a short cable. Length of PSU cable must not exceed 0.3 meter.