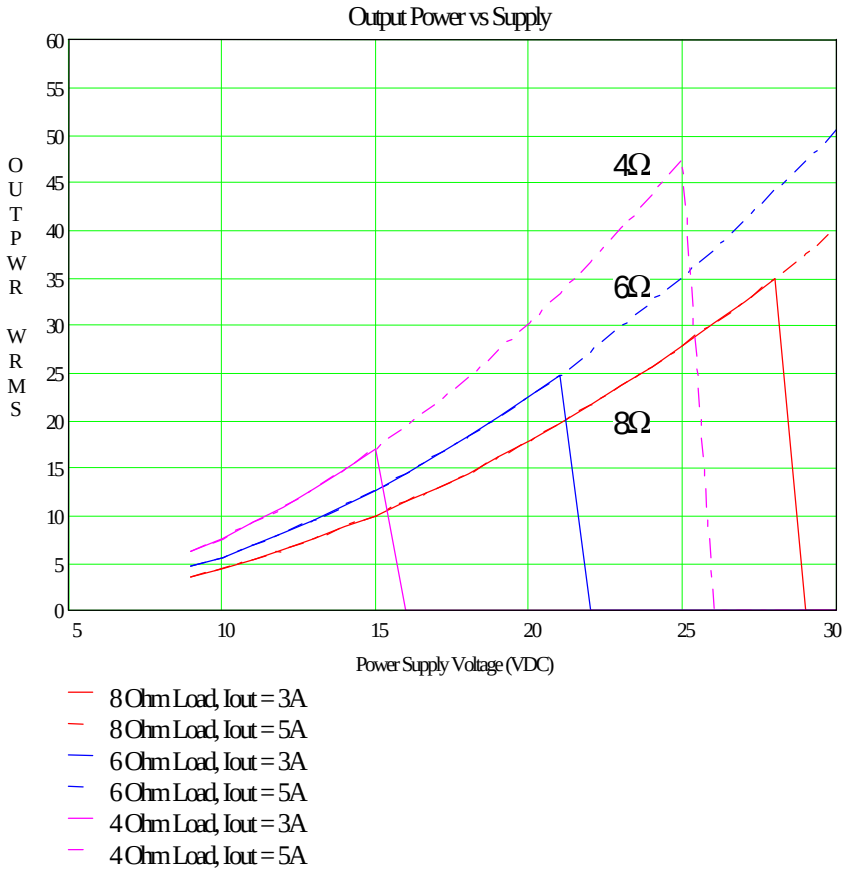
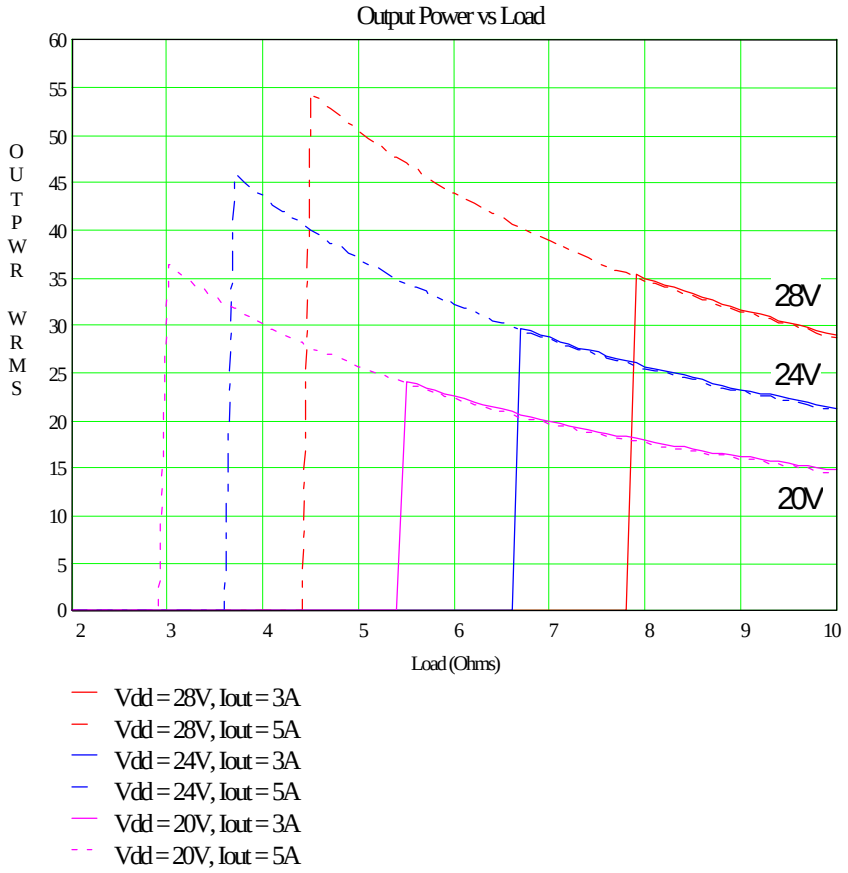
Apogee Technology
Direct Digital Amplification

Application Notes
April 02, 2001

Doc #13000001-01

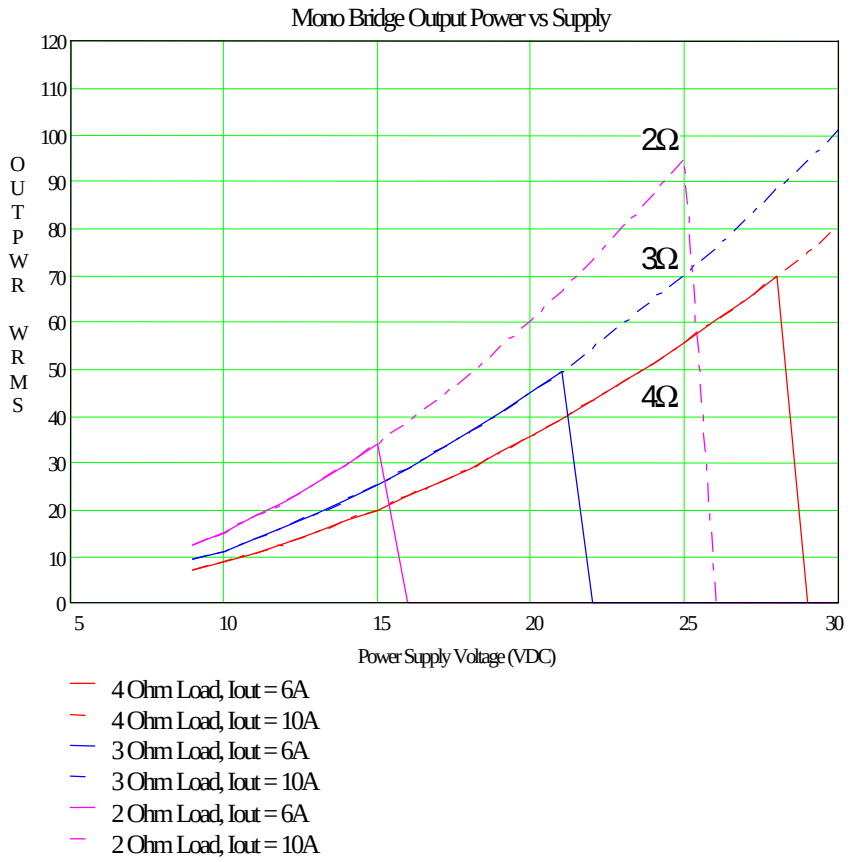
DDX System Design

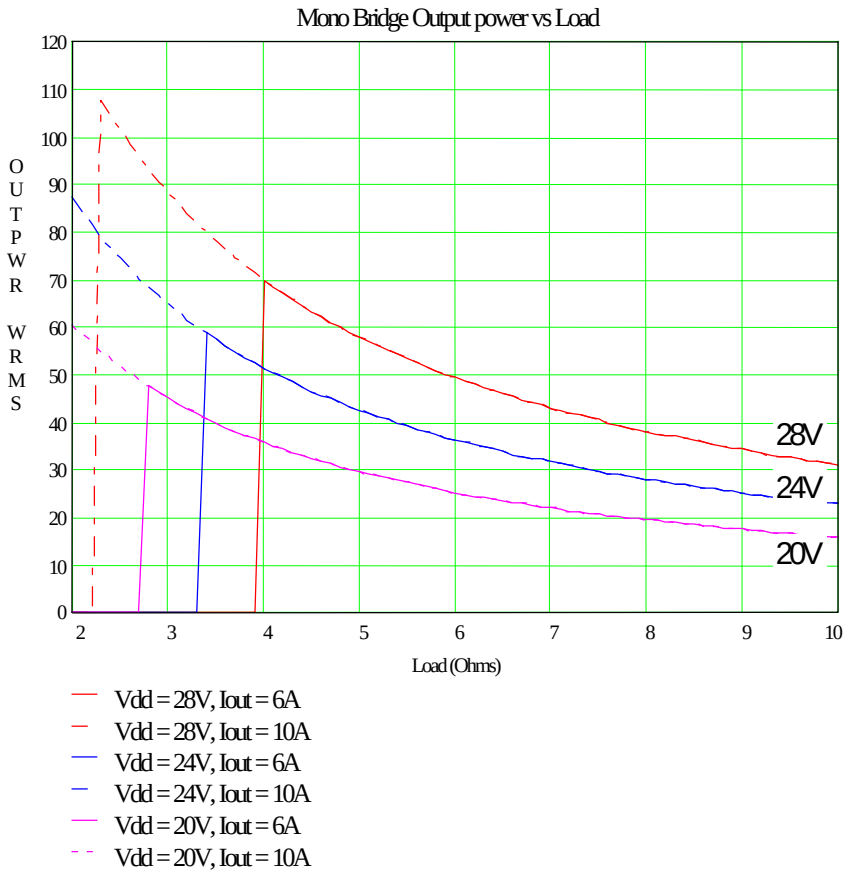




APOGEE TECHNOLOGY, INC.

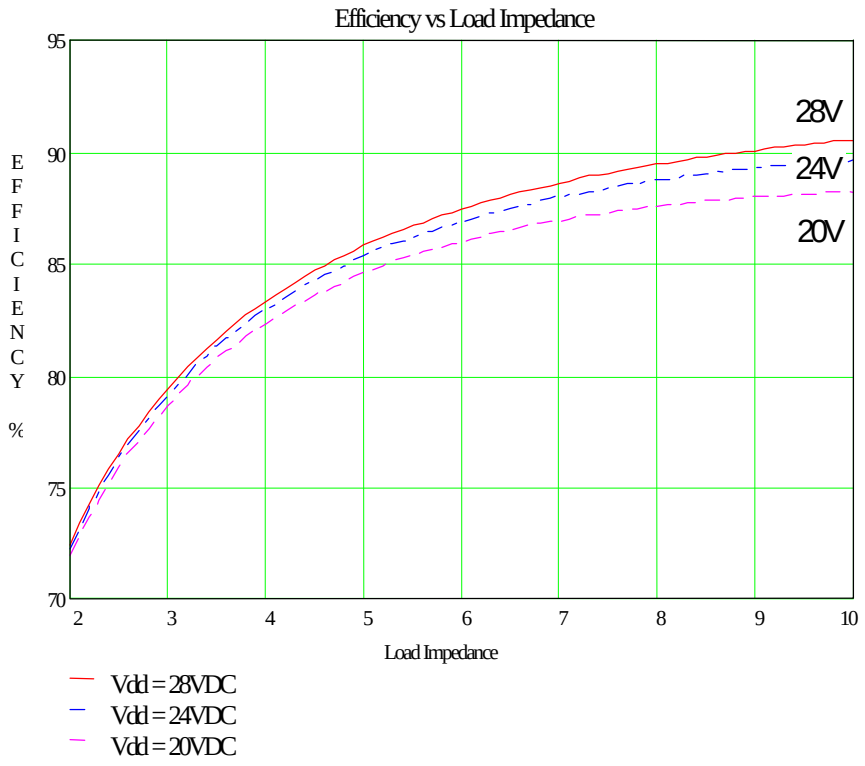
DDX System Design cont.

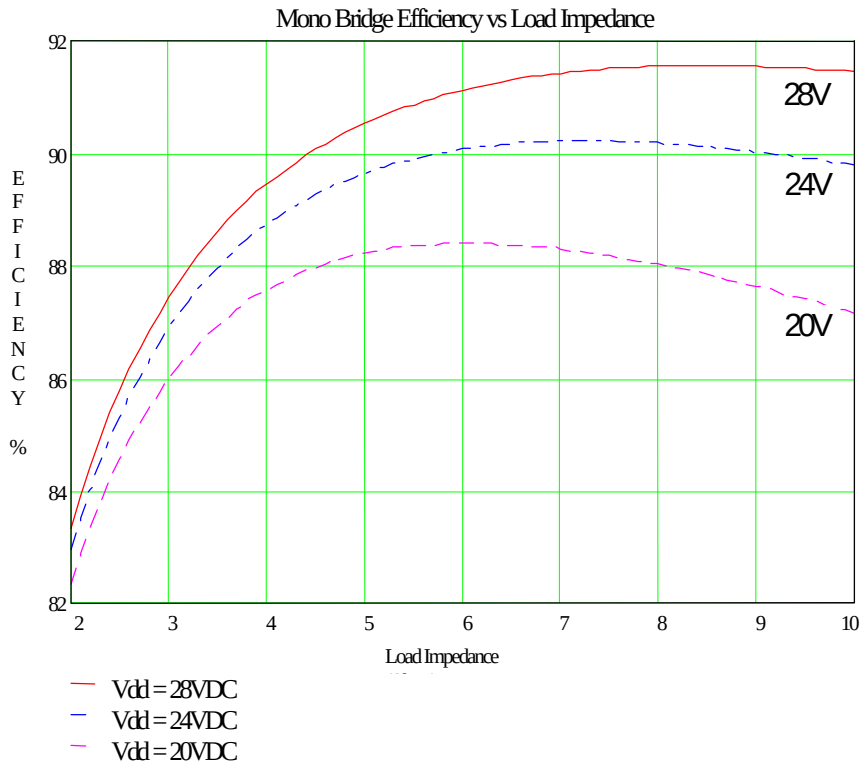




APOGEE TECHNOLOGY, INC.

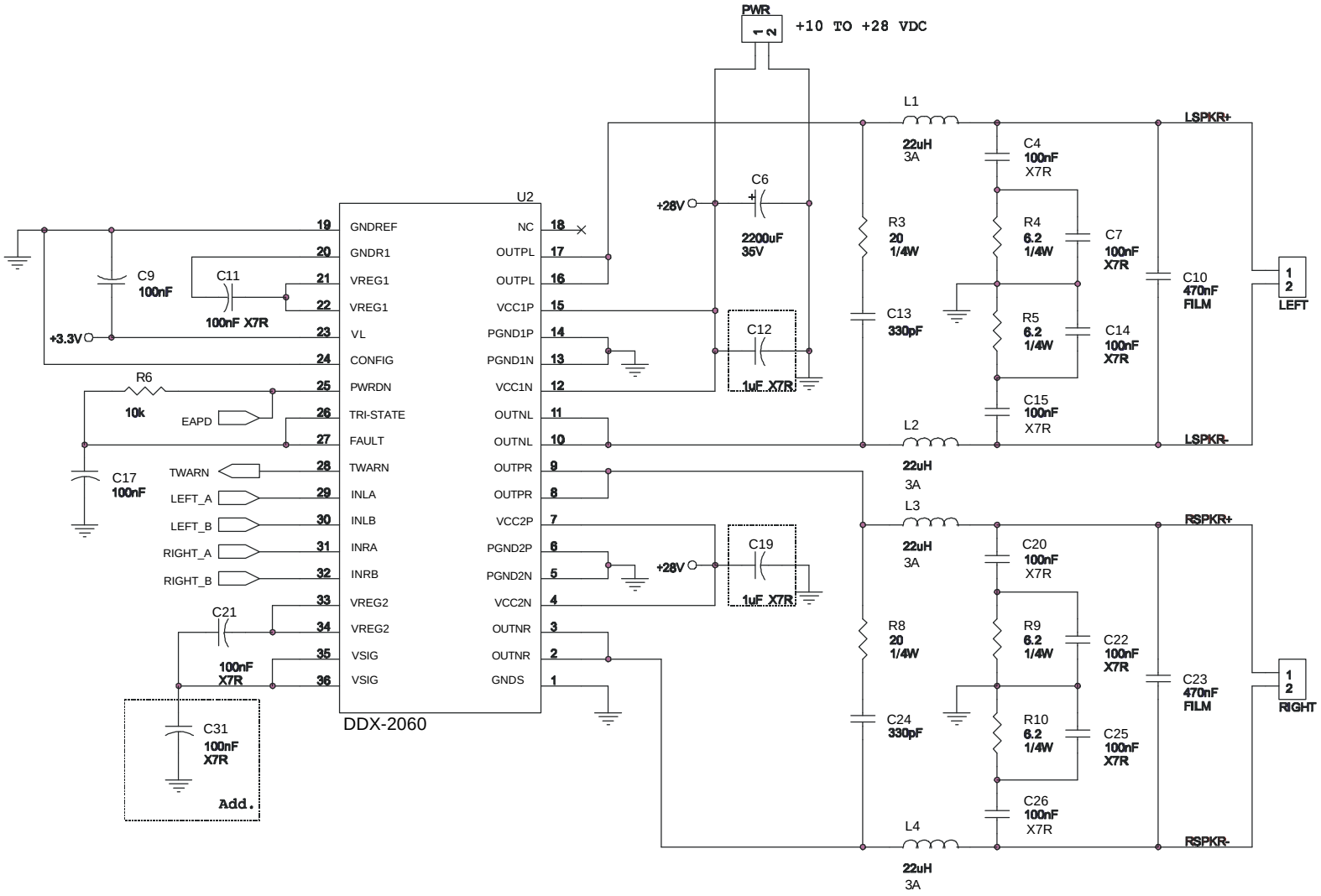
DDX System Design cont.





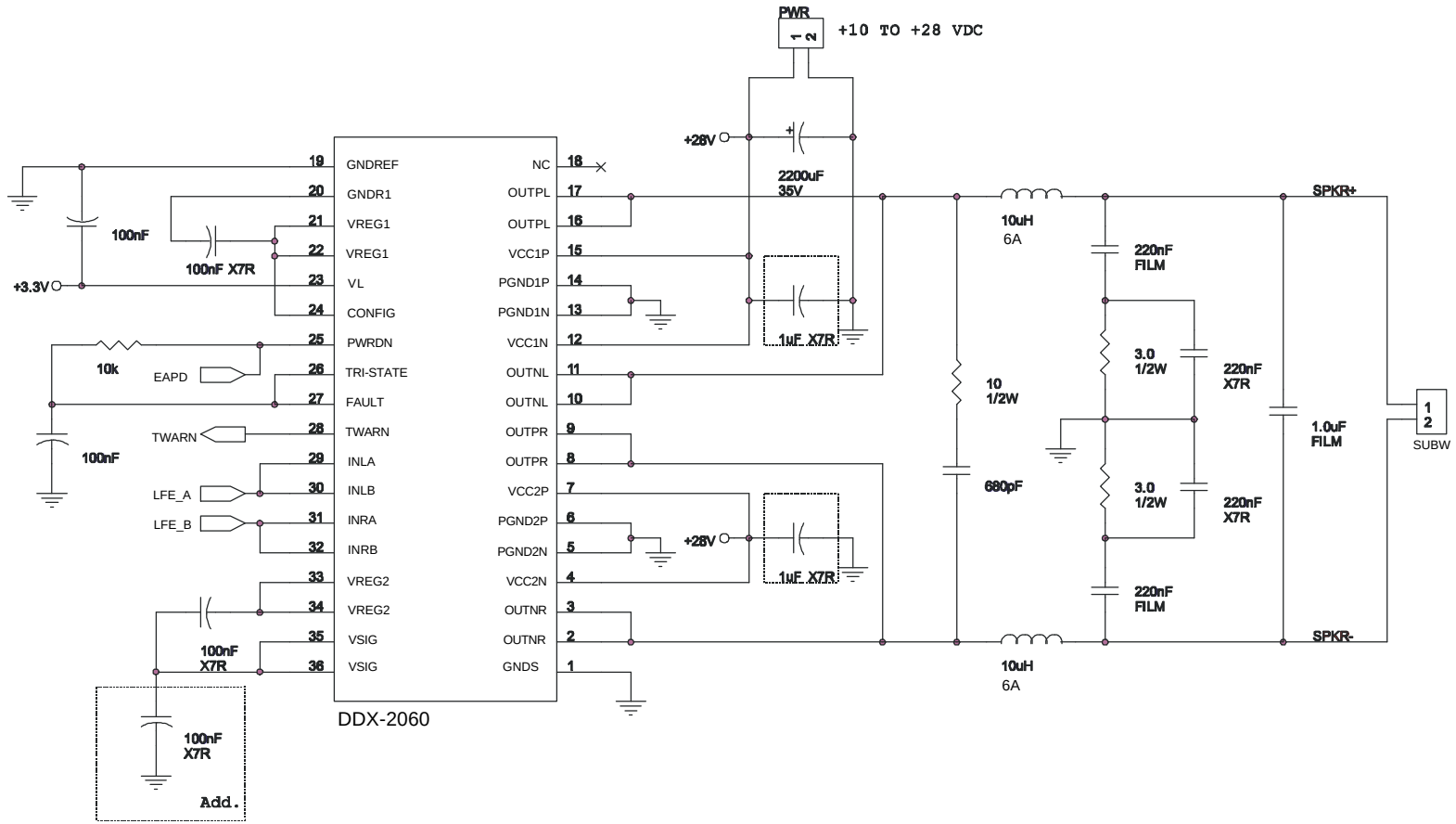
APOGEE TECHNOLOGY, INC.

Recommended Stereo Circuit



APOGEE TECHNOLOGY, INC.

Recommended Mono Circuit



APOGEE TECHNOLOGY, INC.

Layout Considerations

Power Supply Decoupling

- Minimize inductance loop area for SMD ceramic bypass capacitors configured to pins VCC1,2, VSIG, VREG2, VREG1, and VL on DDX-2060.

Power Routing

- Provide star configuration power routing to each DDX-2060 circuit on a multichannel amplifier. Minimize inductance loop area between each DDX-2060 and its respective bulk bypass capacitor. Do not route DDX-2060 power connections under output filter inductors, to prevent coupling to the speaker outputs.

Ground Plane

- PWM logic signals and DDX-2060 H-Bridge outputs should be routed over a continuous ground plane.

- Ground plane areas are also used as thermal dissipating elements on the PCB.

Layout Considerations

Snubber Circuits

- Locate snubber circuits as close as practical between the outputs of the DDX-2060. (Snubbers = R3+C13, R8+C24 per recommended circuit).

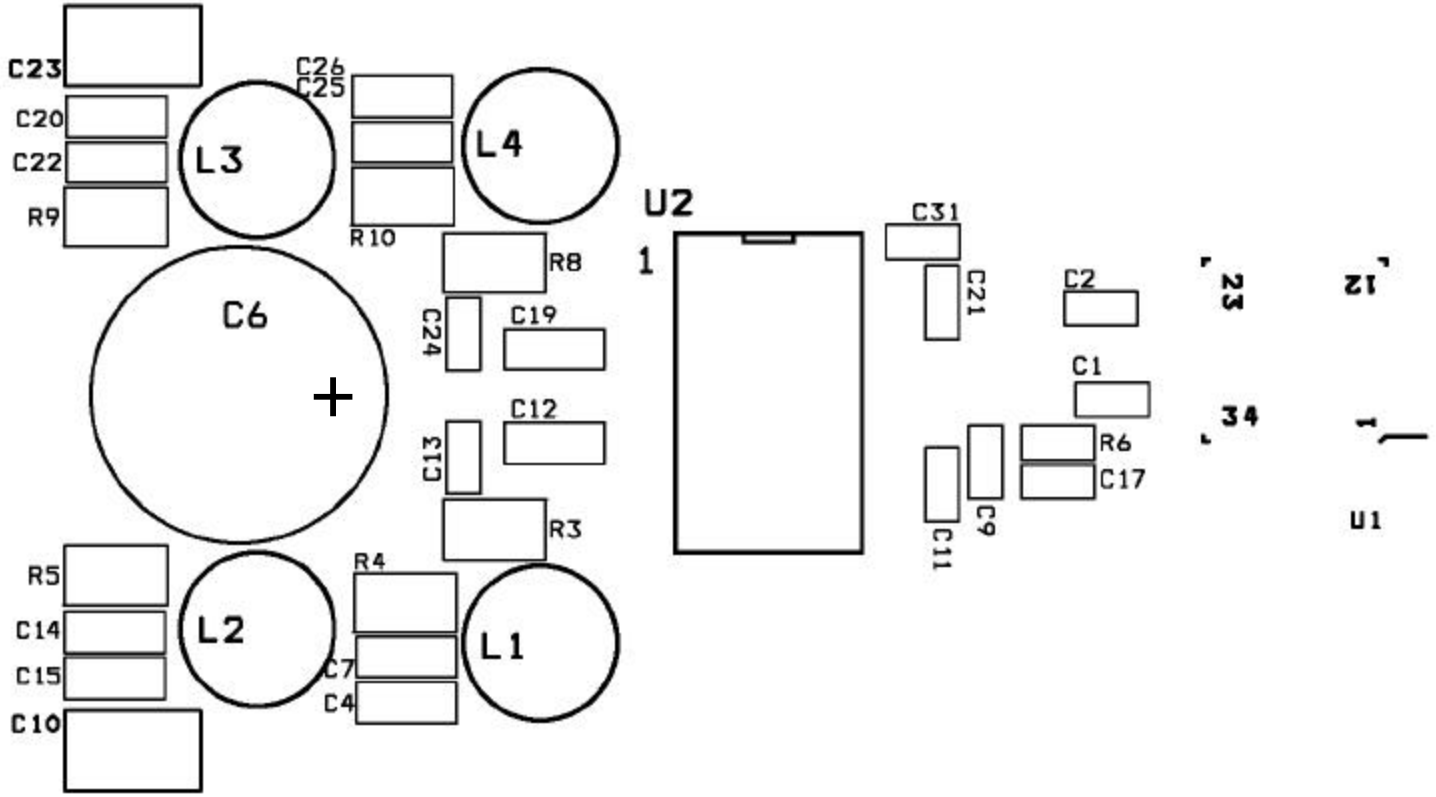
Output Routing

- **Inductor placement** - Maintain a minimum physical separation of one inductor's diameter, particularly between inductors of different channels. Place inductors as close as practical to the DDX-2060 bridged outputs. Minimize trace length on OUTPx and OUTNx signals. These are the primary EMI offenders!

- **Output traces** - Balance the impedance of traces in the output circuit so as to maintain source matching. Match pcb traces on each output circuit to within 10 milliohms.

Critical Circuit Reference Layout

Stereo Configuration

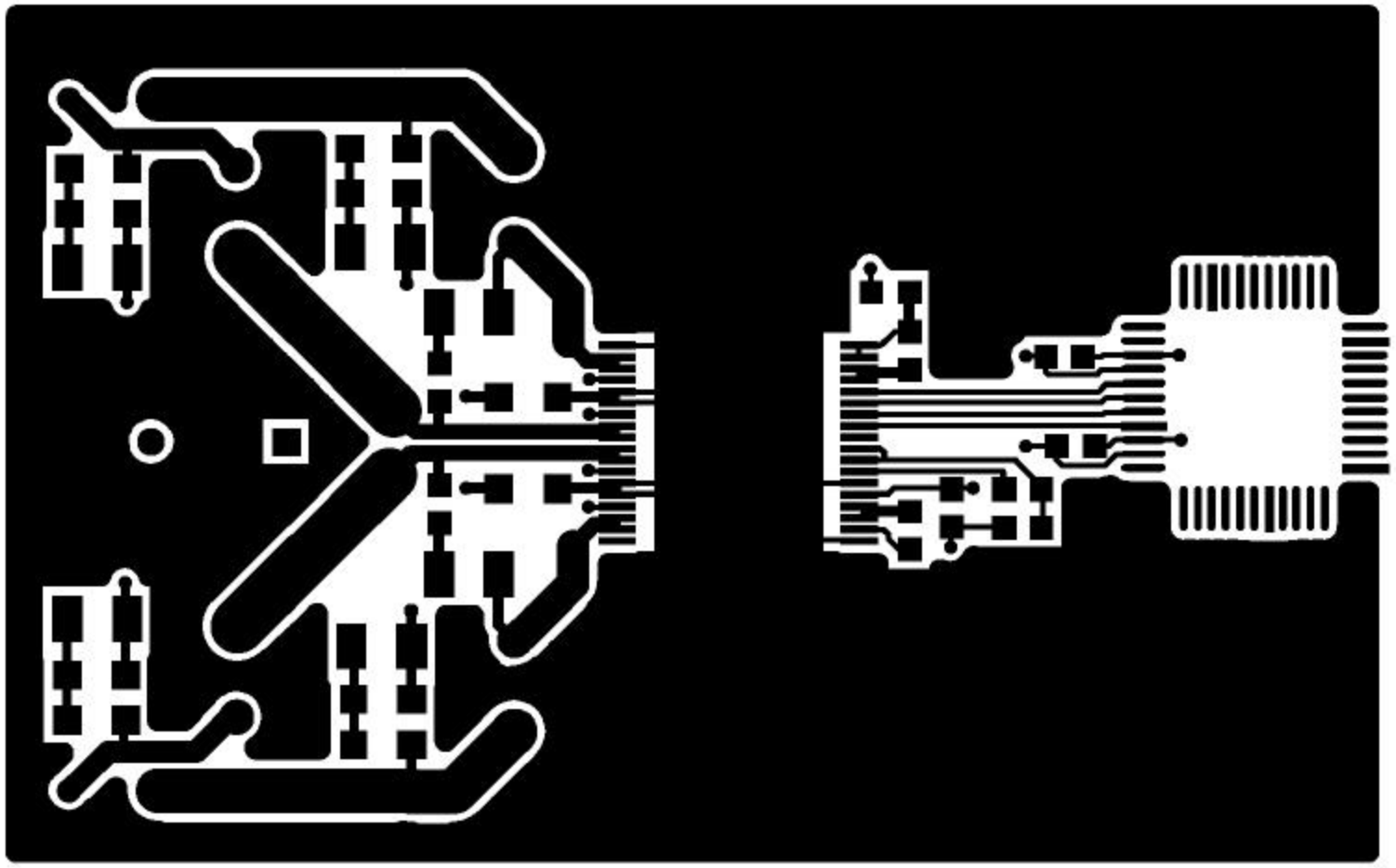


Silkscreen Layer

APOGEE TECHNOLOGY, INC.

Critical Circuit Reference Layout cont.

Stereo Configuration

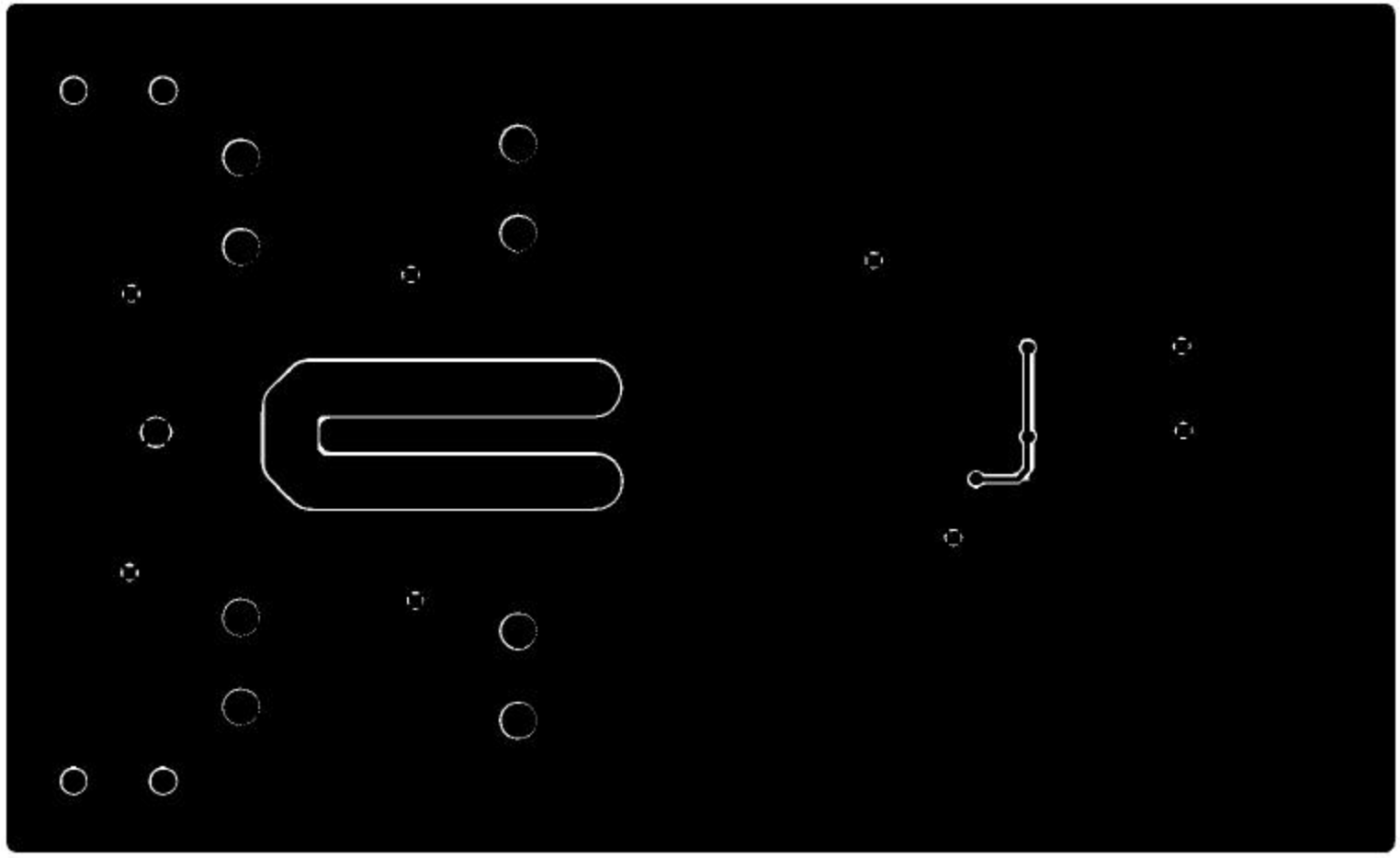


Component Metal Layer

APOGEE TECHNOLOGY, INC.

Critical Circuit Reference Layout cont.

Stereo Configuration

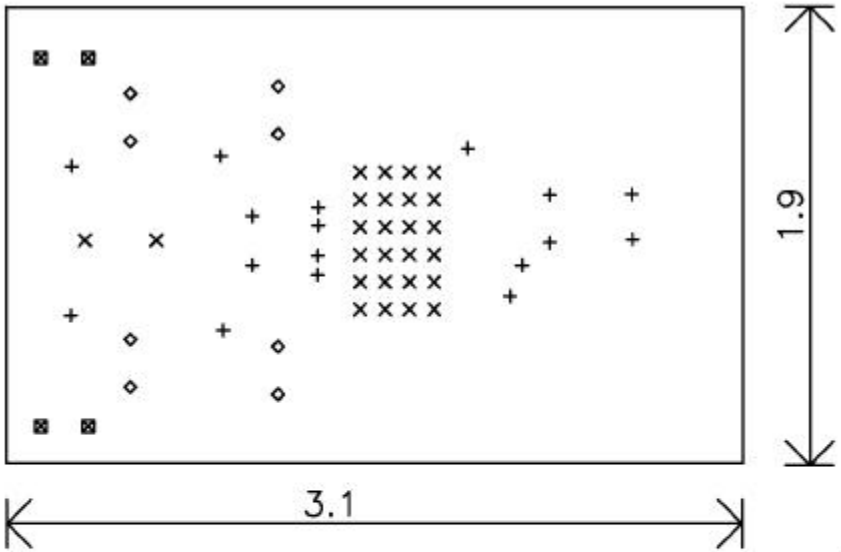


Solder Metal Layer

APOGEE TECHNOLOGY, INC.

Critical Circuit Reference Layout cont.

Stereo Configuration



All Dimensions in Inches

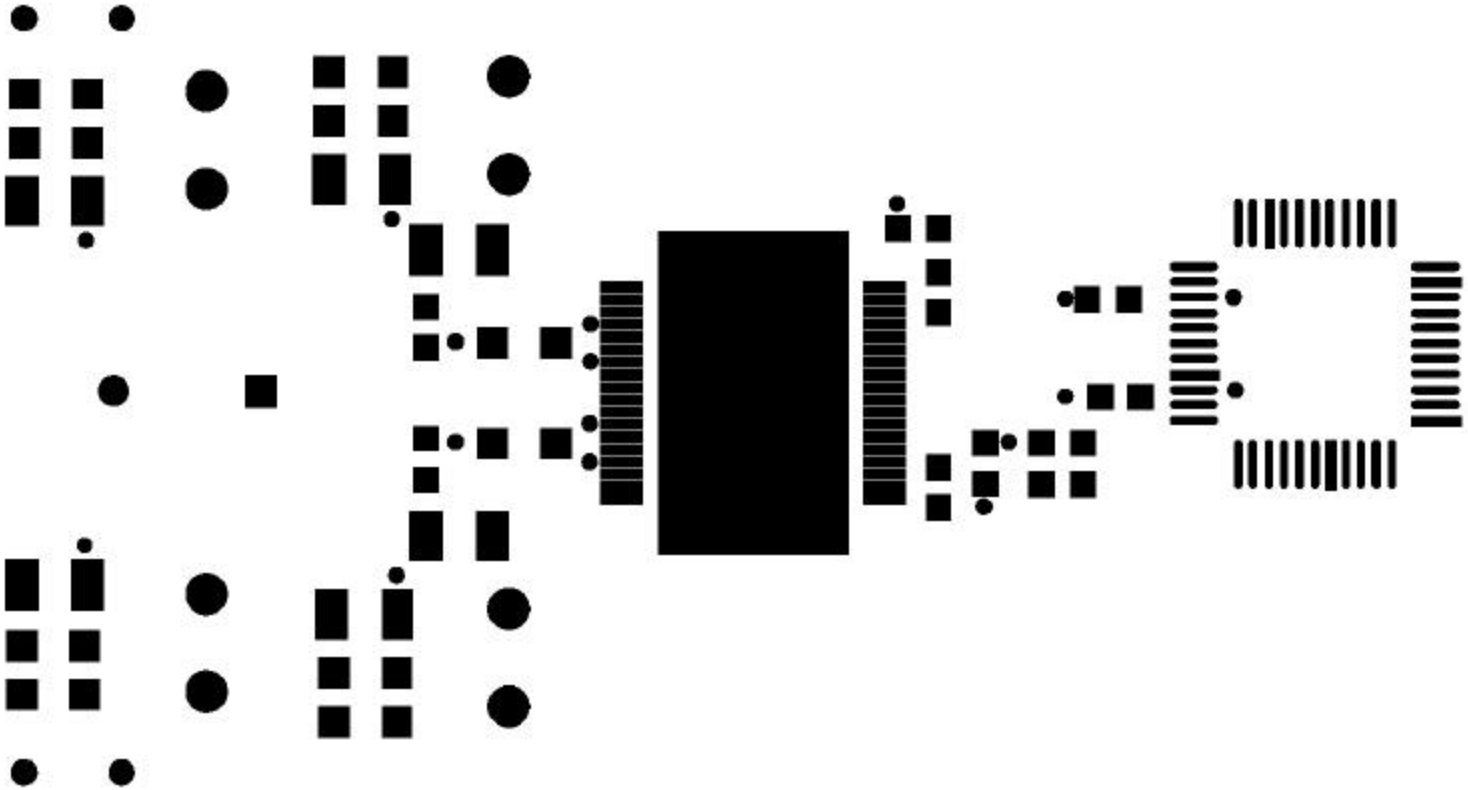
DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
+	0.015		17	
⊠	0.031		4	
×	0.040		26	
◇	0.046		8	
TOTAL			55	

Drill Template

APOGEE TECHNOLOGY, INC.

Critical Circuit Reference Layout cont.

Stereo Configuration



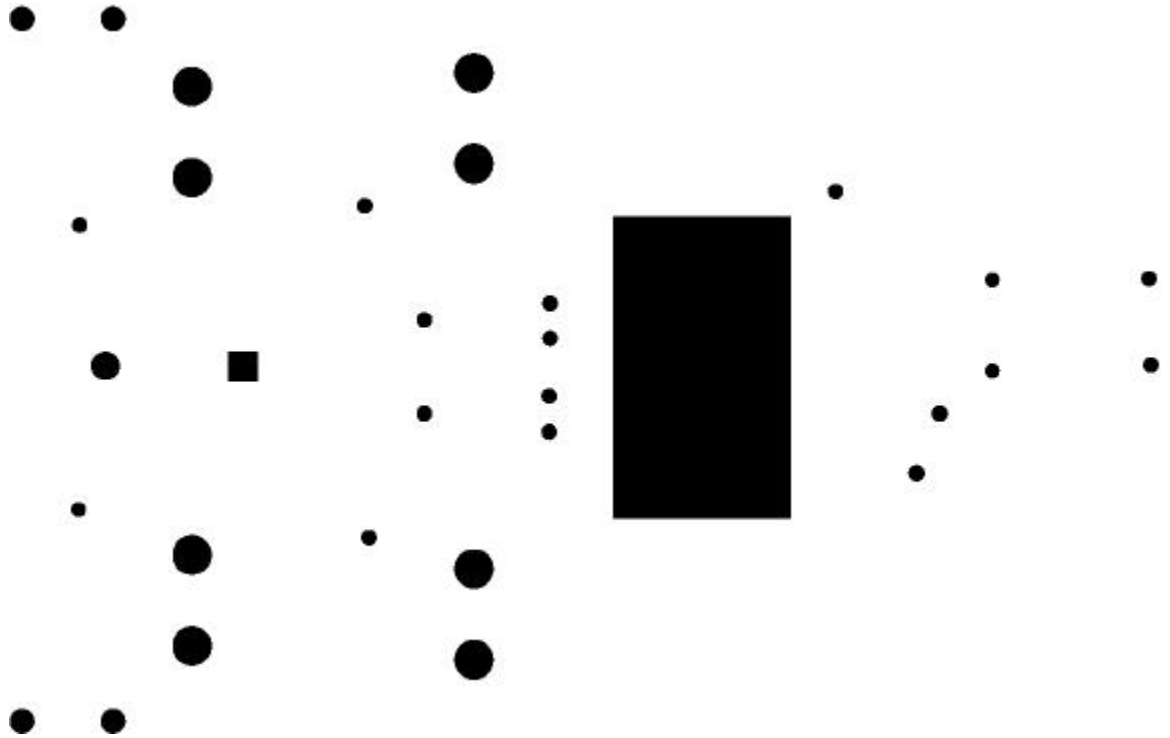
Soldermask Top Layer

Note: Soldermask under DDX-2060 IC facilitates soldering of thermal pad.

APOGEE TECHNOLOGY, INC.

Critical Circuit Reference Layout cont.

Stereo Configuration

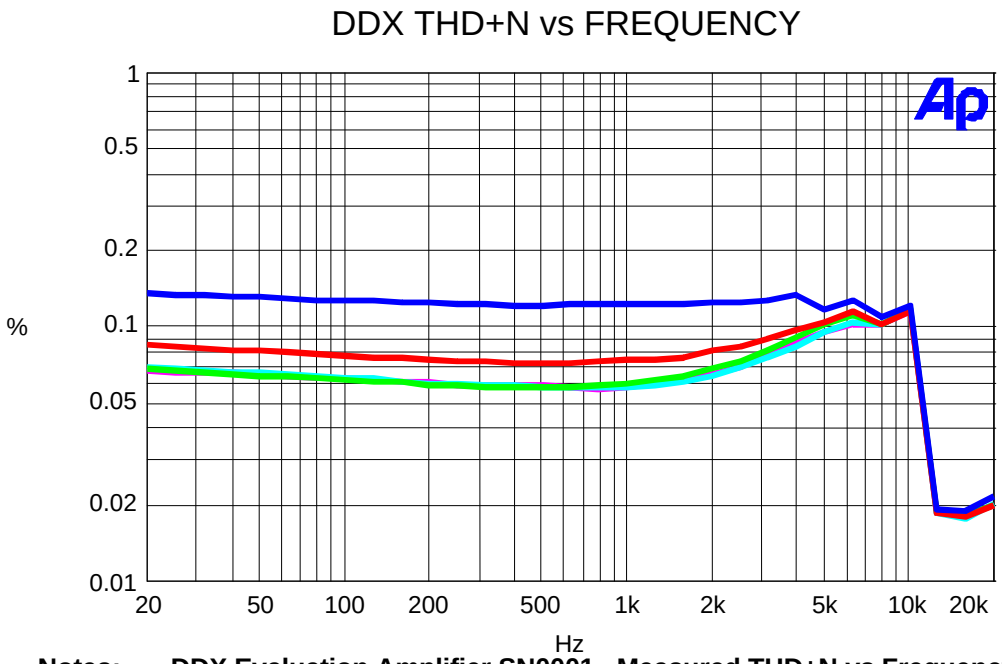


Soldermask Bottom Layer

Note: Soldermask under DDX-2060 IC facilitates soldering of thermal pad.

APOGEE TECHNOLOGY, INC.

DDX-2060 IC Bypassing

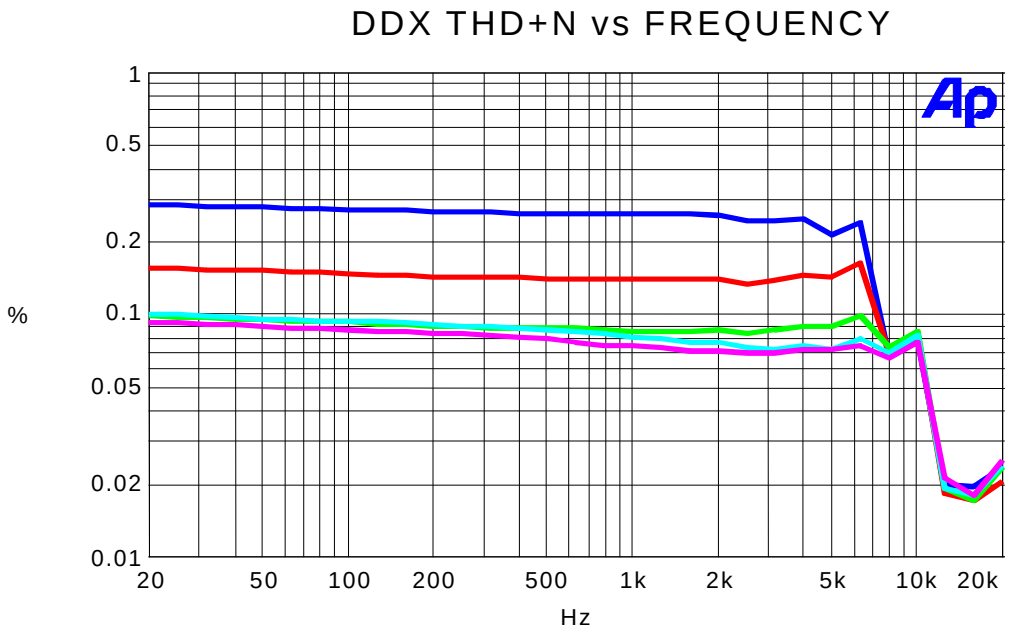


Notes: DDX Evaluation Amplifier SN0001. Measured THD+N vs Frequency for various Bulk Bypass Capacitors. CH1 driven and measured. Input Voltage = 28V using Regulated Lab Supply. Volume = 0dB. Fs = 48KHz. Digital Source = -3.0dBFS. Output power = 17.6W into an 8 Ohm load.

Blue -- 10uF.	**SNR = 92dBr A-WTG.**
Red -- 100uF.	**SNR = 92dBr A-WTG.**
Green -- 390uF.	**SNR = 92dBr A-WTG.**
Cyan -- 1000uF.	**SNR = 92dBr A-WTG.**
Magenta -- 2200uF.	**SNR = 93dBr A-WTG.**

APOGEE TECHNOLOGY, INC.

DDX-2060 IC Bypassing cont.



Notes: DDX Evaluation Amplifier SN0001. Measured THD+N vs Frequency for various Bulk Bypass Capacitors. CH1,2 driven. CH1 measured. Input Voltage = 28V using Regulated Lab Supply. Volume = 0dB. Fs = 48KHz. Digital Source = -3.0dBFS. Output power = 17.6W per channel into 8 Ohm loads.

Blue -- 10uF.	**SNR = 89dBr A-WTG.**
Red -- 100uF.	**SNR = 90dBr A-WTG.**
Green -- 390uF.	**SNR = 90dBr A-WTG.**
Cyan -- 1000uF.	**SNR = 90dBr A-WTG.**
Magenta -- 2200uF.	**SNR = 90dBr A-WTG.**

APOGEE TECHNOLOGY, INC.

Thermal Resistance

Very Low Thermal resistance, SO 36 package

(θ_{JC}) = 2.5ºC/W max

Thermal resistance is to heat flow as Electrical resistance is to Current flow

APOGEE TECHNOLOGY, INC.

PC Board Heat Flow

Considerations for soldering the Power SO-36 package to the PCB

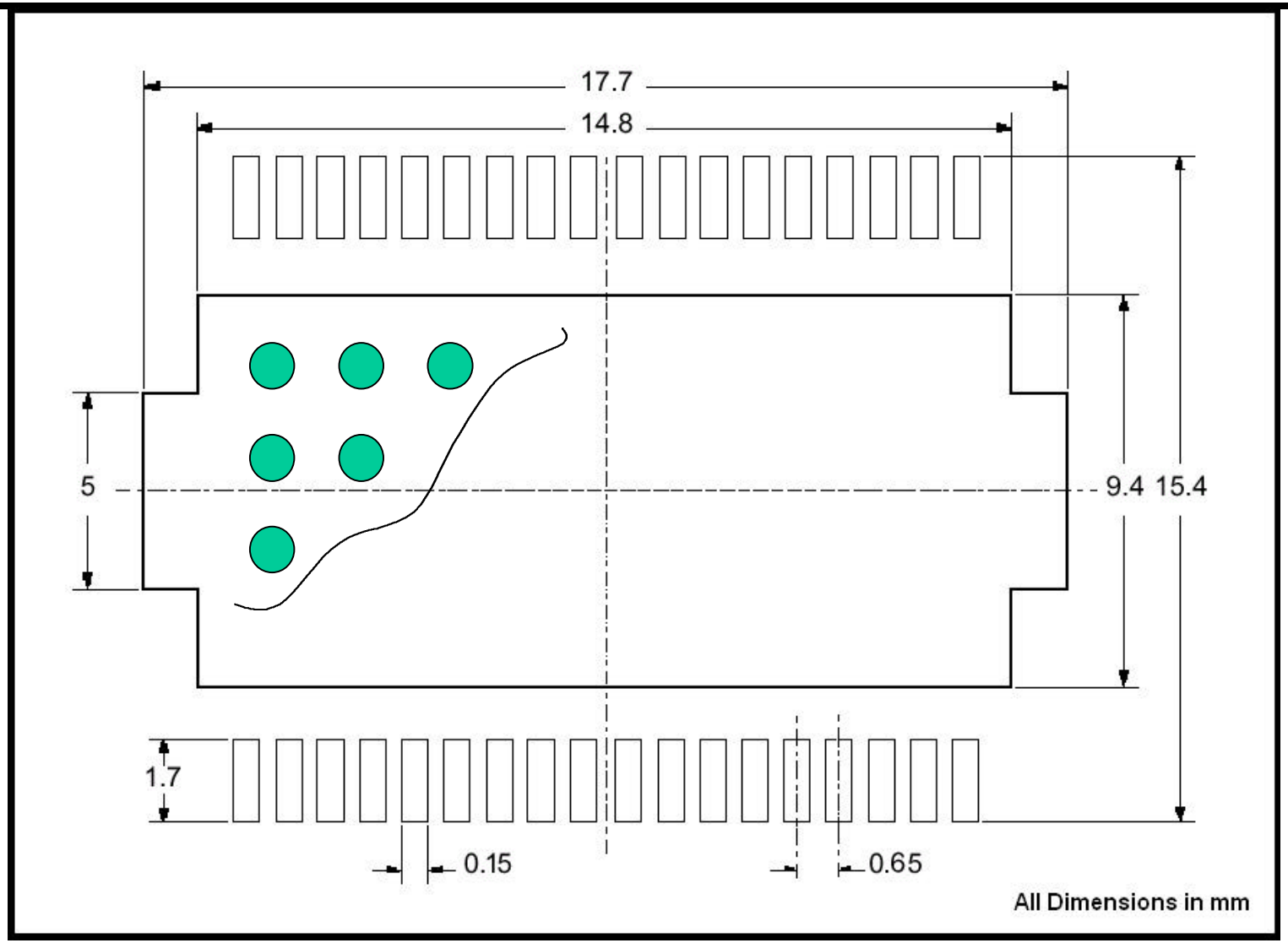
Heat flow through the vias

Proper Thermal management is required to:

- Maximize Power output
- Maximize Reliability

APOGEE TECHNOLOGY, INC.

Recommended PCB Footprint



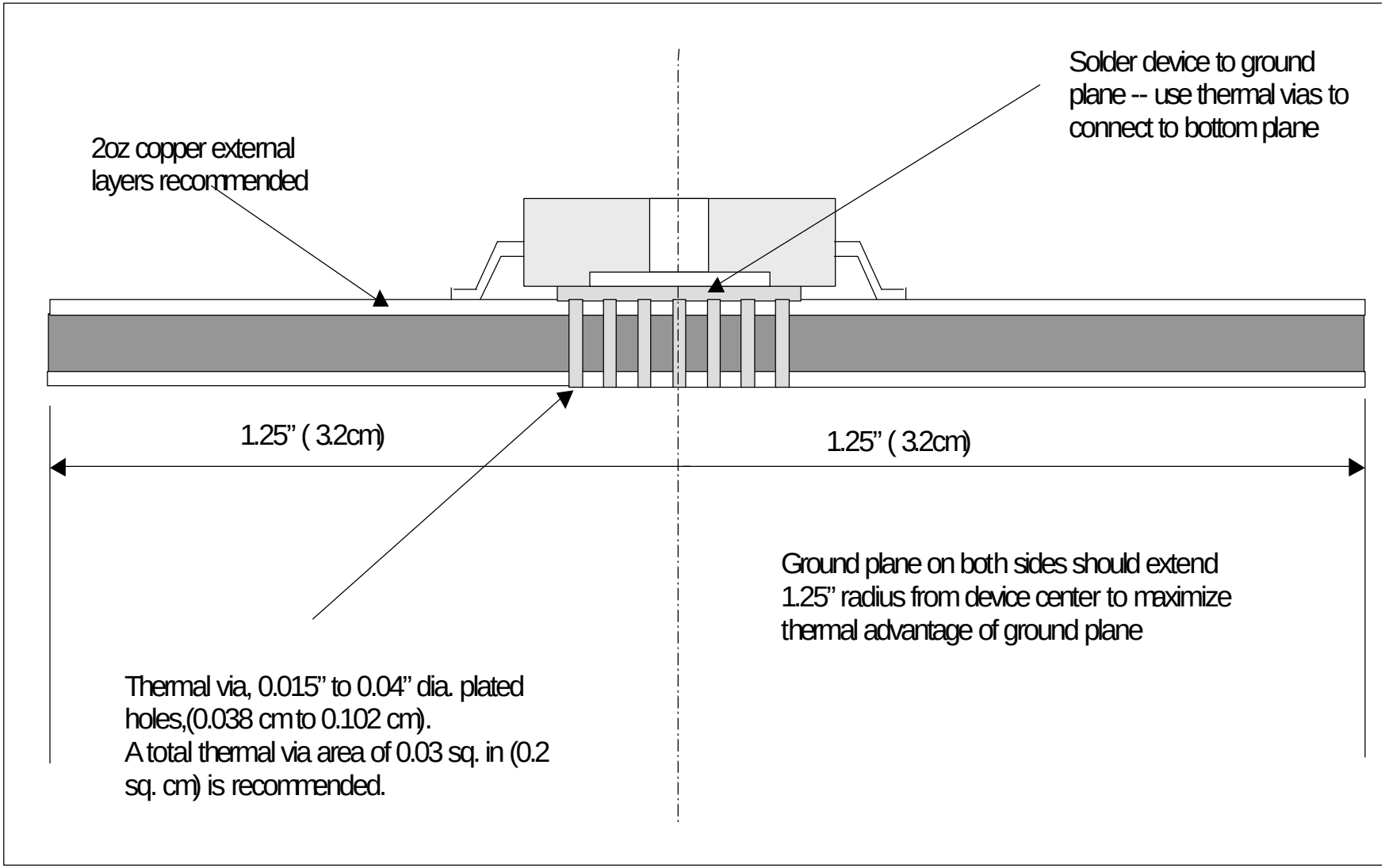
APOGEE TECHNOLOGY, INC.

Surface Convection to Air

- Heat Flow through copper foil decreases with distance
- Limits usable heatsink area to 2.0 - 2.5 in. (51 - 64 mm) diameter circle, 5 in^2 (32.3 mm^2) per board side
- Will improve if heavier copper is used

APOGEE TECHNOLOGY, INC.

Recommended Thermal Planes



APOGEE TECHNOLOGY, INC.