HV Floating MOS-Gate Driver ICs

(HEXFET is a trademark of International Rectifier)

Topics Covered:

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Block diagram of a typical MGD
Bootstrap operation
How to select the bootstrap components
How to calculate the power dissipation in the MGD
How to deal with negative transients
Layouts and other guidelines
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Brushless and induction motor drives
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1. GATE DRIVE REQUIREMENTS OF HIGH-SIDE DEVICES

The gate drive requirements for a power MOSFET or IGBT utilized as a high side switch (drain connected to the high voltage rail, as shown in Figure 1) driven in full enhancement, i.e., lowest voltage drop across its terminals, can be summarized as follows:

1. Gate voltage must be 10-15V higher than the drain voltage. Being a high side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.

2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high side power device, which, in most applications, swings between the two rails.
3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

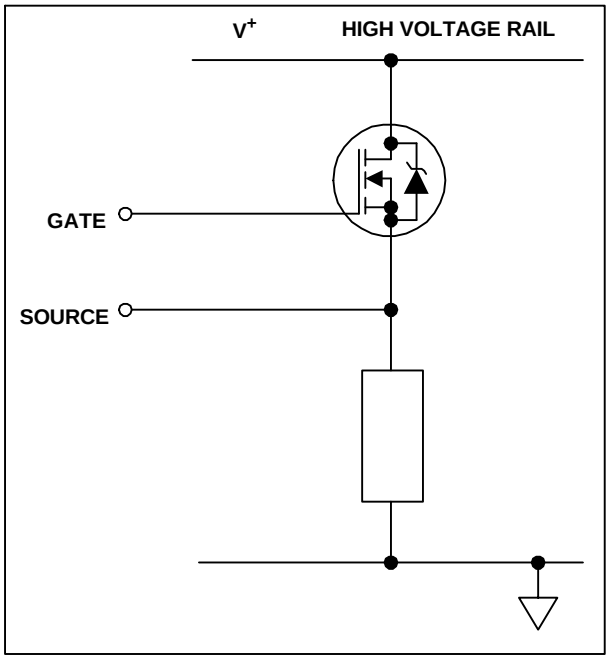


Figure 1. Power MOSFET in high side configuration

With these constraints in mind, several techniques are presently used to perform this function, as shown in principle in Table I. Each basic circuit can be implemented in a wide variety of configurations.

International Rectifier's family of MOS-gate drivers (MGDs) integrate most of the functions required to drive one high side and one low side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, they provide very fast switching speeds, as shown in Table II for the IR2110, and low power dissipation. They can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, they can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz.

2. A TYPICAL BLOCK DIAGRAM

The block diagram of the IR2110 will be used to illustrate the typical structure of most MGDs (Figure 2). It comprises a drive circuit for a ground referenced power transistor, another for a high side one, level translators and input logic circuitry.

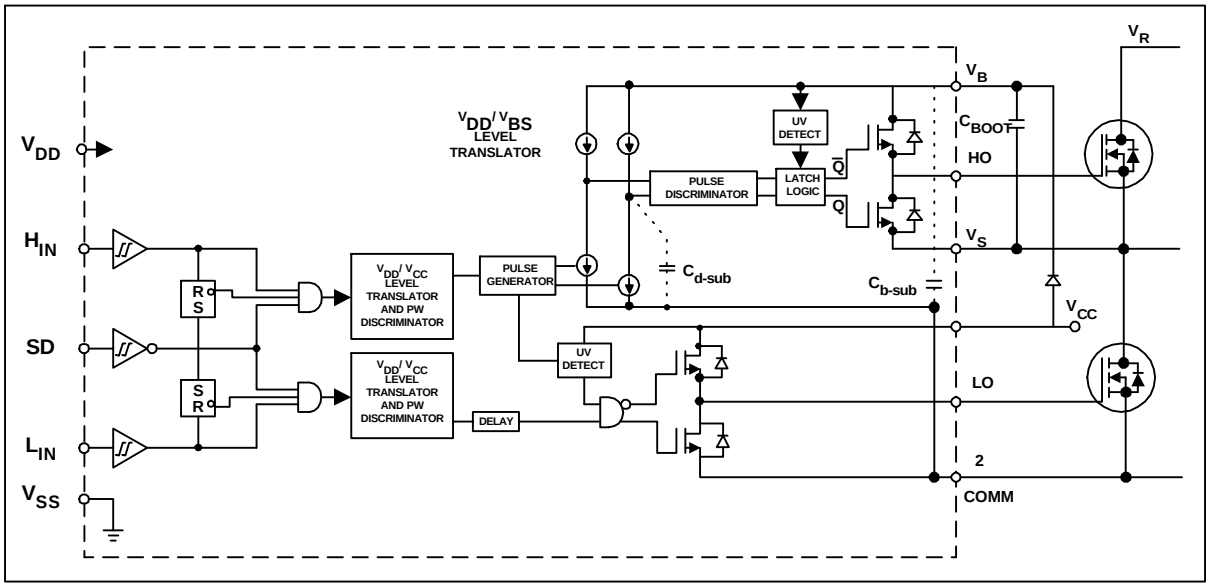


Figure 2. Block Diagram of the IR2110

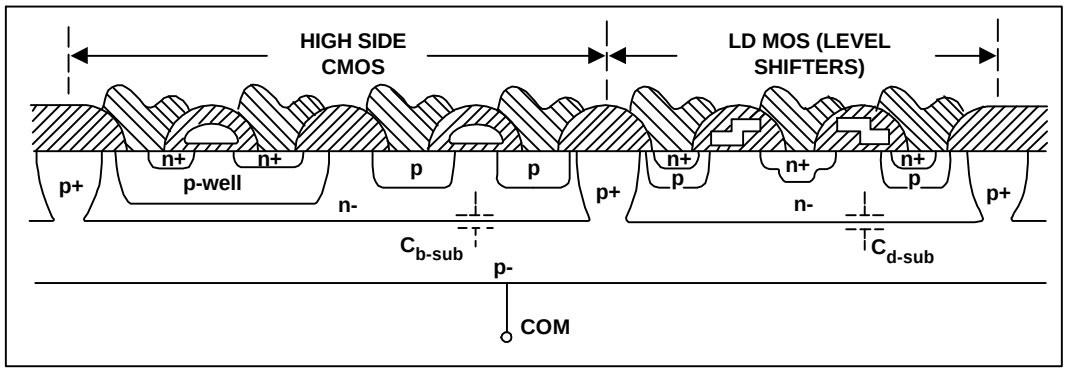


Figure 3. Silicon crossection showing the parasitic capacitances.

2.1 Input logic

Both channels are controlled by TTL/CMOS compatible inputs. The transition thresholds are different from device to device. Some MGDs, (IR211x and IR215x) have the transition threshold proportional to the logic supply V_{DD} (3 to 20V) and Schmitt trigger buffers with hysteresis equal to 10% of V_{DD} to accept inputs with long rise time. Other MGDs (IR210x, IR212x, IR213x) have a fixed transition from logic 0 to logic 1 between 1.5 to 2 V. Some MGDs can drive only one high-side power device. Others can drive one high-side and one low-side power device. Others can drive a full three-phase bridge. It goes without saying that any high-side driver can also drive a low side device. Those MGDs with two gate drive channel can have dual , hence independent, input commands or a single input command with complementary drive and predetermined deadtime.

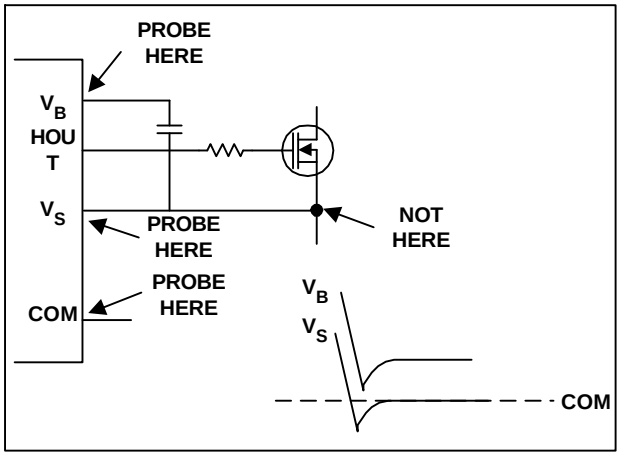


Figure 4. Look at the VS spike during the reverse recovery. Always probe right at the IC pin.

Those application that require a minimum deadtime should use MGDs with independent drive and relay on a few passive components to build a deadtime, as shown in Section 12. The propagation delay between input command and gate drive output is approximately the same for both channels at turn-on (120ns) as well as turn-off (95ns) with a temperature dependence characterized in the data sheet. The shutdown function is internally latched by a logic 1 signal and activates the turn off of both power devices.

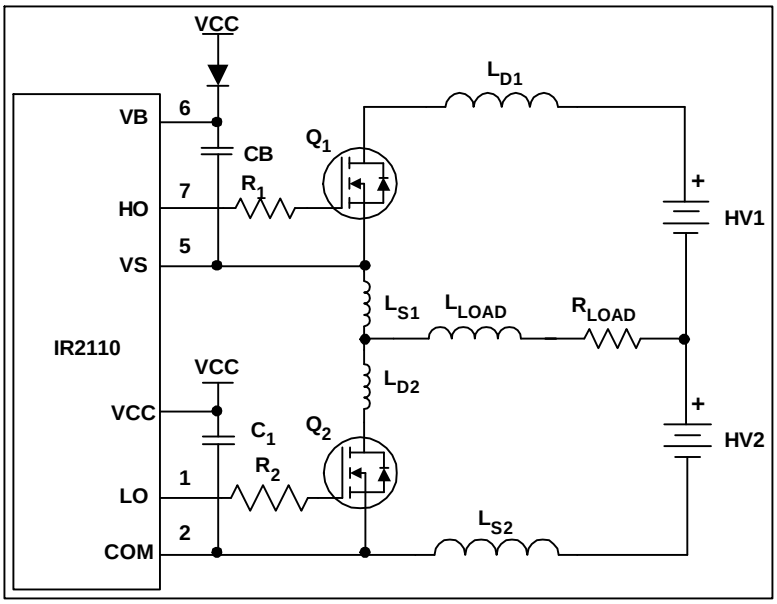


Figure 5a. A typical half-bridge circuit with stray inductances.

The first input command after the removal of the shutdown signal clears the latch and activates its channel. This latched shutdown lends itself to a simple implementation of a cycle-by-cycle current control, as exemplified in Section 12. The signals from the input logic are coupled to the individual channels through high noise immunity level translators. This allows the ground reference of the logic supply (V_{SS} on pin 13) to swing by ±5V with respect to the power ground (COM). This feature is of great help in coping with the less than ideal ground layout of a typical power conditioning circuit. As a further measure of noise immunity, a pulse-width discriminator screens out pulses that are shorter than 50ns or so.

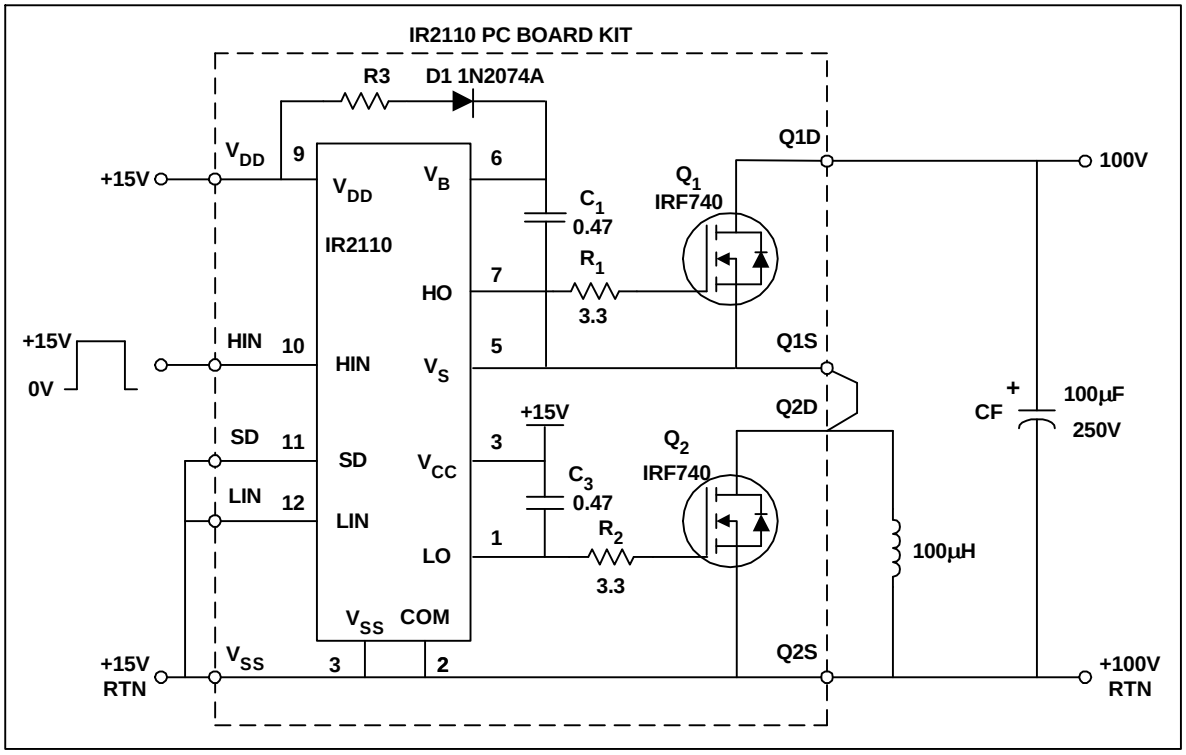


Figure 5b. Test Circuit

2.2 Low Side Channel

The output stage is implemented either with two N-Channel MOSFETs in totem pole configuration (source follower as a current source and common source for current sinking), or with an N-Channel and a P-Channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.25 to 2A, depending on the MGD. The source of the lower driver is independently brought out to pin 2 so that a direct connection can be made to the source of the power device for the return of the gate drive current. The relevance of this will be seen in Section 5. An undervoltage lockout prevents either channel from operating if V_{CC} is below the specified value (typically 8.6/8.2V).

Any pulse that is present at the input command for the low-side channel when the UV lockout is released turns on the power transistor from the moment the UV lockout is released. This behavior is different from that of the high-side channel, as we will see in the next section.

2.3 High side channel

This channel has been built into an "isolation tub" (Figure 3) capable of floating from 500 or 600V to -5V with respect to power ground (COM). The tub "floats" at the potential of V_S, which is established by the voltage applied to V_B. Typically this pin is connected to the source of the high side device, as shown in Figure 2 and swings with it between the two rails.

If an isolated supply is connected between this pin and V_S , the high side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command. One significant feature of MOS-gated transistors is their capacitive input characteristic, i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current. If the high side channel is driving one such device, the isolated supply can be replaced by a capacitor, as shown in Figure 2.

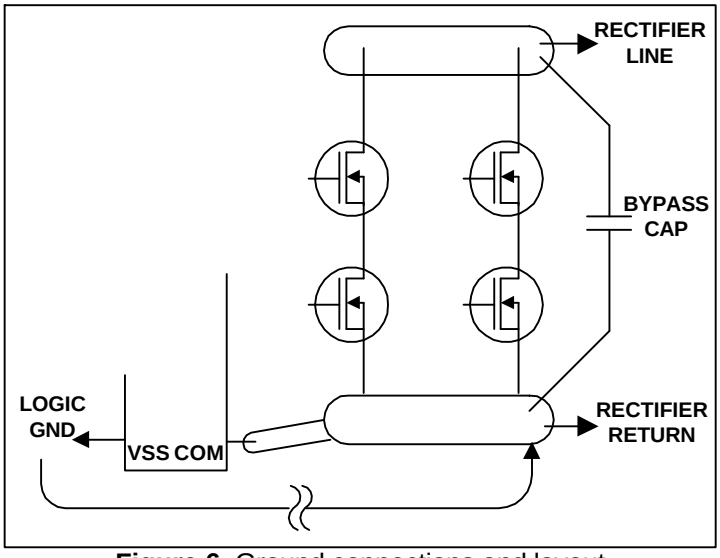


Figure 6. Ground connections and layout

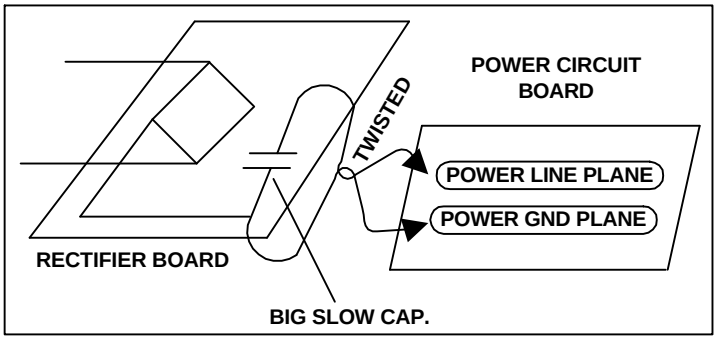


Figure 7. Power Bypass Capacitor

The gate charge for the high side MOSFET is provided by the bootstrap capacitor which is charged by the 15V supply through the bootstrap diode during the time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small. The input commands for the high side channel have to be level-shifted from the level of COM to whatever potential the tub is floating at which can be as high as 500V. As shown in Figure 2 the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential.

The use of pulses greatly reduces the power dissipation associated with the level translation. The pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50V/ns in the power devices will not adversely affect the operation of the MGD. This channel has its own undervoltage lockout which blocks the gate drive if the voltage between V_B and V_S, i.e., the voltage across the upper totem pole is below its limits (typically 8.7/8.3V). The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output. The high voltage level translator circuit is designed to function properly even when the V_S node swings below the COM pin by a voltage indicated in the datasheet, typically 5 V. This occurs due to the forward recovery of the lower power diode or to the Ldi/dt induced voltage transient. Section 5 gives directions on how to limit this negative voltage transient.

3. HOW TO SELECT THE BOOTSTRAP COMPONENTS

As shown in Figure 2 the bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines.

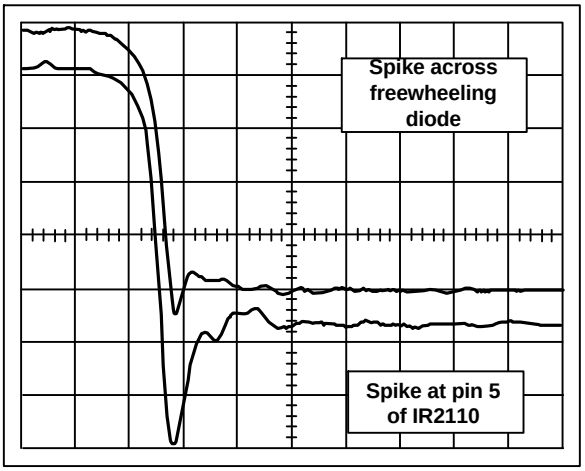


Figure 8. Waveform while Q1 turning off 20A inductive load (20ns/div and 20V/div)

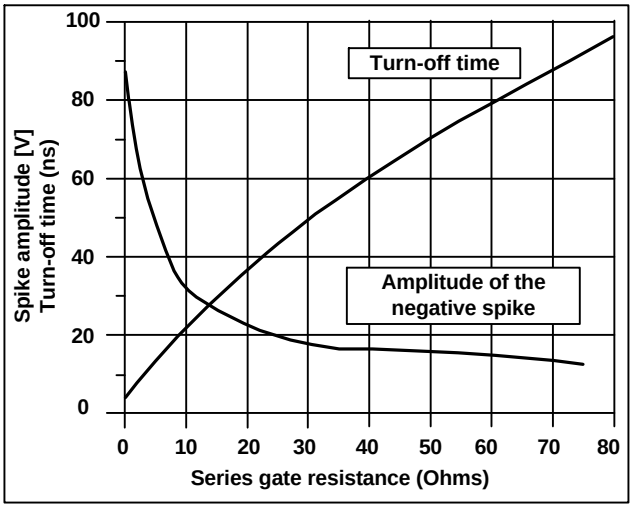


Figure 9. Series gate resistance vs. the amplitude of the negative voltage spike and the turn-off time.

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

a) Gate charge required (see also INT-944). After the turn-on charge has been delivered to the gate, the voltage across the bootstrap capacitor should be significantly higher than the minimum required for full enhancement (10V). Assuming for the sake of illustration a drop of 1.5V on the charging path of the bootstrap capacitor and assuming a voltage drop due to the internal leakage of half the excess gate voltage we have the following constraint:

$$C_{BOOT} >> 2\ Q_G / \ (V_{CC} - 1.5 - 10)$$

In some unusual operating conditions like transient overloads the voltage drop across the lower power transistor can be significantly higher than the 1.5V used in the example.

b) Longest conduction time. The voltage on the gate of the power MOSFET at the end of the longest conduction time must be sufficient to keep it in full enhancement.

The steady state current drawn from C_{BOOT} is equal to the quiescent current of the high side channel (I_{QBS}). Assuming the initial voltage calculated from the previous expression this constraint translates into the following:

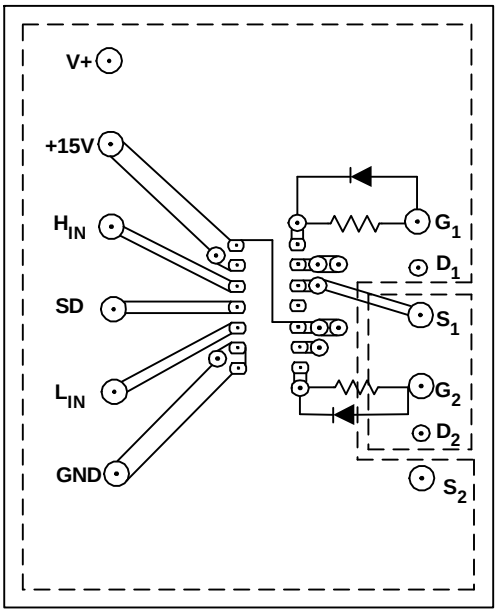


Figure 10. IR2110 test circuit Note: Dotted lines represent pads on bottom side of board. V+, GND, D1, S1, D2, S2, terminals have plated through holes

$$C_{BOOT} >> 2\ I_{QBS} \bullet t_{on} / (V_{CC} - 1.5 - 10)$$

In practice the value of the bootstrap capacitor cannot be less than 0.47 microF for reasons that will be seen in Section 5, and the bigger the better. The bootstrap diode must be able to block the full voltage seen in the specific circuit; in the circuits of Figures 25, 28 and 29 this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100kHz it is approximately 12mA.

The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason it is important that this diode be ultrafast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply.

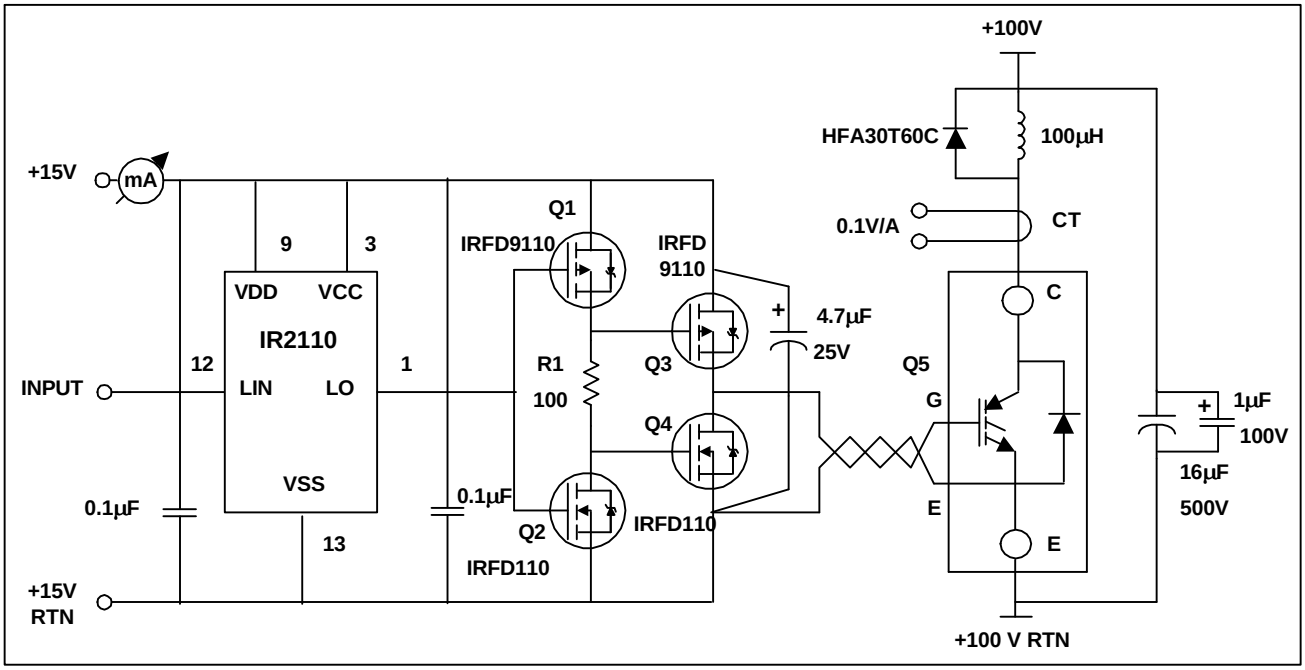


Figure 11. Test Circuit

4. HOW TO CALCULATE THE POWER DISSIPATION IN AN MGD

The total losses in an MGD result from a number of factors that can be grouped under high voltage and low voltage static and dynamic.

a) Low voltage static losses ($P_{D(1v)q}$) are due to the quiescent currents from the three low voltage supplies V_{DD}, V_{CC} and V_{SS}. In a typical 15V application these losses amount to approximately 3.5mW at 25°C, going to 5mW at T_J = 125 °C .

b) Low voltage dynamic losses ($P_{D(lv)SW}$) on the V_{CC} supply are due to two different components:

b1) Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

$$P_G = V \bullet Q_G \bullet f$$

For two IRF450 HEXFETs operated at 100kHz with Vgs = 15V, we have:

$$PG = 2 \bullet 15 \bullet 120 \bullet 10^9 \bullet 100 \bullet 10^3 = 0.36W$$

The factor 2 in the formula is valid in the assumption that two devices are being driven, one per channel. If V_{SS} is generated with a bootstrap capacitor/diode, this power is supplied from V_{CC}. The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances. If the internal resistance is 6 Ohms, sourcing or sinking, and if the gate resistor is 10 Ohms, only 6/16 of P_G is dissipated within the MGD. These losses are not temperature dependent.

b2) Dynamic losses associated with the switching of the internal CMOS circuitry. They can be approximated with the following formula:

$$P_{CMOS} = V_{CC} \bullet Q_{CMOS} \bullet f$$

with Q_{CMOS} between 5 and 30nC, depending on MGD. In a typical 100kHz application these losses would amount to tens of mW, largely independent from temperature.

c) High voltage static losses ($P_{D(hv)q}$) are mainly due to the leakage currents in the level shifting stage. They are dependent on the voltage applied on the V_S pin and they are proportional to the duty cycle, since they only occur when the high side power device is on. If Vs were kept continuously at 400V they would typically be 0.06mW at 25°C, going to 2.25mW at 125°C. These losses would be virtually zero if V_S is grounded, as in a push-pull or similar topology.

d) High voltage switching losses ($P_{D(hv)sw}$) comprise two terms, one due to the level shifting circuit (Figure 2) and one due to the charging and discharging of the capacitance of the high side p-well ($C_{b\text{-}sub}$ in Figure 3).

d1) Whenever the high side flip-flop is reset, a command to turn-off the high side device (i.e., to set the flip-flop) causes a current to flow through the level-shifting circuit. This charge comes from the high voltage bus through the power device and the bootstrap capacitor. If the high side flip-flop is set and the low side power device is on, a command to reset it causes a current to flow from Vcc, through the diode. Thus, for a half-bridge operating from a rail voltage V_R, the combined power dissipation is:

$$(V_R + V_{CC}) \bullet Q_P \bullet f$$

with Qp the charge absorbed by the level shifter, and f the switching frequency of the high side channel. Q_P is approximately 4nC at V_R = 50V, going to 7nC as the rail voltage increases to 500V. In a typical 400V, 100kHz application these losses would amount to approximately 0.3W. This includes the charging and discharging of $C_{d\text{-}sub}$. There is a third possible source for Q_P, when the high side flip-flop is being reset (i.e., the power device is being turned on) and the low side power device is off. In this case the charge comes from the high voltage bus, through the device capacitances and leakages or through the load. The power dissipation is somewhat higher than what would be calculated from the above expression. In a push-pull or other topology where V_S (pin 5) is grounded, both level shifting charges are supplied from V_{CC} with significantly lower losses.

d2) In a high-side/low-side power circuit the well capacitance $C_{b\text{-}sub}$ is charged and discharged every time V_S swings between V_R and COM. Charging current is supplied by the high voltage rail through the power device and the epi resistance. Discharge occurs through the lower device and the epi resistance. The losses incurred in charging or discharging a capacitor through a resistor are equal to QV/2, regardless of the value of resistance. However, much of these losses occur outside the bridge driver, since the epi resistance is negligible compared to the internal resistance of the power devices during their switching transitions. Assuming a charge value of 7nC at 450V and an operating frequency of 100kHz, the *total* losses caused by the charging and discharging of this capacitance amount to:

$$Q \bullet V \bullet f = 7 \bullet 10^{-9} \bullet 450 \bullet 10^{5} = 0.31W$$

almost totally outside the IR2110. For all practical purposes, $C_{b\text{-}sub}$ cannot be distinguished from the output capacitance of the lower power device.
If V_S is grounded the capacitor is charged at a fixed voltage and these losses would be zero. $C_{b\text{-}sub}$ (like $C_{d\text{-}sub}$) is a reverse biased junction and its capacitance is a strong function of voltage. These charges are not temperature dependent.

The above discussion on losses can be summarized as follows:

- The dominant losses are switching and, in high voltage applications at 100kHz or above, the static losses in Item a and Item c can be neglected outright.

- The temperature dependence of the switching losses is not significant;

- The combined losses are a function of the control mode, as well as the electrical parameters and temperature.

Knowing the power losses in the MGD, the maximum ambient temperature can be calculated (and vice-versa) from the following expression:

$$T_{a\,max} = T_{j\,max} - P_D \bullet R_{th\,j\text{-}a}$$

where $R_{th\,j\text{-}a}$ is the thermal resistance from die to ambient.

The following example shows a typical breakdown of losses for two IRF830s in a half-bridge, from a 400 V rail, 100 kHz, no load, no gate resistors.

$P_{D(lv)q}$ 0.004W

$P_{D(lv)SW}$: $P_{CMOS} = 15 \cdot 16 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.024$

$P_G = 2 \cdot 15 \cdot 28 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.084$

$P_{D(hv)q}$ 0.002

$P_{D(hv)sw}$: $(400 + 200) \cdot 7 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.42$

Total 0.534

The value of 200V in the formula to calculate $P_{D(hv)sw}$ is appropriate at no load, since this case would be the third in Section 4.2.d.l, i.e. the output of the half-bridge settles on a voltage that is between the two rails.

The actual junction temperature can be measured while in operation by pulling lmA from the Shutdown pin with the help of an adjustable current source, like the LM334. The voltage at the pin is 650mV at 25°C, decreasing by 2mV/°C.

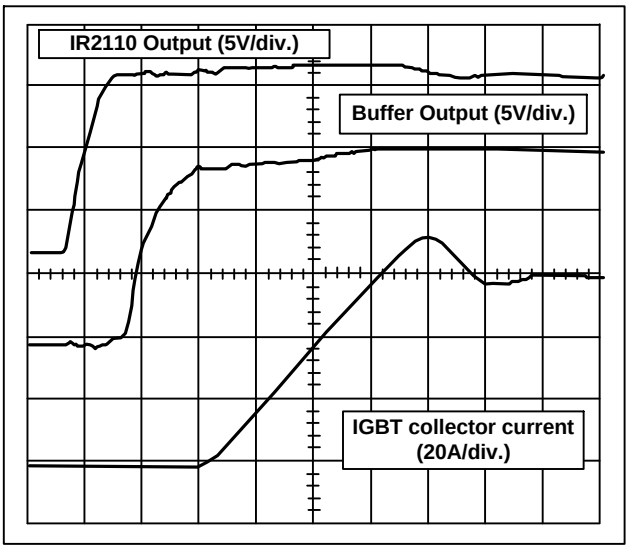


Figure 12a. Waveform, turn-on, IGBT module switching inductive load of 60A. (50ns/div.)

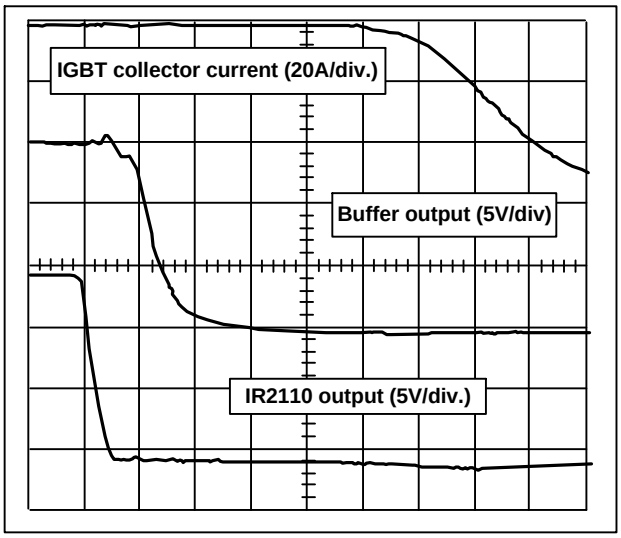


Figure 12b. Waveform, turn-off. Propagation delay is 50ns, fall time is less than 40ns when driving 600nC gate charge of the module 50ns/div.

5. HOW TO DEAL WITH NEGATIVE TRANSIENTS ON THE V_S PIN

The voltage on any pin of an integrated circuit has to be kept between the supply voltages, plus or minus a diode drop, otherwise parasitic diodes in the silicon structure go in conduction and cause erratic operation. This is also true for the MGDs from IR, with two notable exceptions:

- COM and V_{SS} can move with respect to each other by ±5 V
- V_S (the gate drive return of the high side) can go below COM by a voltage that is guaranteed to be no less than 5 V.

In the natural course of bootstrap operation, as V_S goes to ground the bootstrap capacitor recharges to the V_{CC} voltage. However, if V_S goes below ground by a significant amount, the bootstrap capacitor overcharges, and the CMOS circuitry supplied by it, which IR rated at 20 V, may fail. Furthermore, the parasitic diode of the internal structure may go on, causing erratic operation and shoot-through. The following guidelines should be followed to prevent this from happening:

- The bootstrap capacitor should be 0.47 microF minimum, the larger the better. Increasing the value of the bootstrap capacitor reduces the risk of overcharging it.

- A bypass capacitor in the order of 4.7 microF should be mounted right between the V_{CC} , V_{DD} and COM pins.

- The bootstrap diode and capacitors should be close to the bypass capacitor

- A resistor in series with the bootstrap diode is ***not*** advisable, as it may cause the main "C_{sub} diode" of Figure 3 to go in conduction. A zener diode across the bootstrap capacitor is helpful in low power applications or when the spike on the V_S pin is small (-20 V or so)

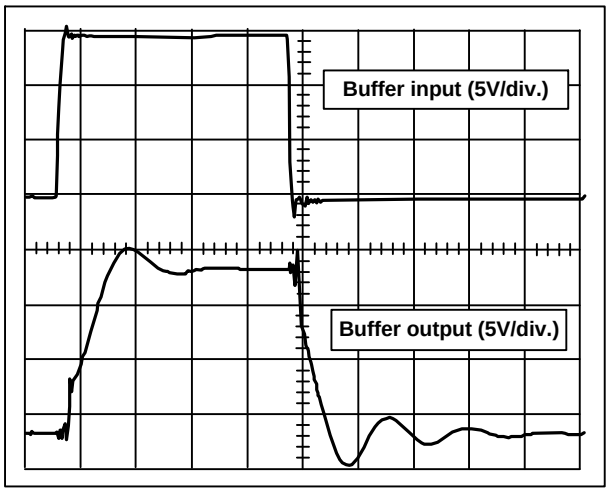


Figure 13. Waveform driving 0.1mF capacitor (250nS/div.)

- V_{SS} and COM should not be shorted together underneath the IC, as this defeats the noise immunity built into the chip. V_{SS} should be connected to the ground of the IC that provides the logic signals to the input of the MGD. COM, on the other hand, is the gate drive return and should be connected to the source or emitter of the power transistor. The current sense resistor, if any, should be ***outside*** of the gate drive loop.

- The stray inductances of the power circuit should be minimized with an appropriate layout, and the switching speed adjusted as indicated in the next section.

The potential discrepancy between V_{SS} and COM should be kept in mind when analyzing waveforms with an oscilloscope. The waveforms will be correct to the extent that the ground lead of the oscilloscope is short and tied to the appropriate reference point. For example, if the gate waveform of the lower device is to be analyzed, the ground probe should be connected to the source pin of the device, and not to a generic "ground." In fact, it is useful to measure the noise voltage between one ground and another while switching high currents. Figure 4 shows how to probe for V_S.

6. LAYOUT AND OTHER GENERAL GUIDELINES

A typical half-bridge circuit is shown in Figure 5a, together with its stray inductances. It shows critical stray inductances located in the high current path which affect the operation of the circuit. L_{D1} and L_{S2} are in a "dc path" and are due to the wiring inductance between the MOSFETs and the decoupling capacitors; L_{S1} and L_{D2} are in an "ac path" and are due to the wiring inductance between the MOSFETs. The stray inductance in a dc path can be cancelled with a capacitor, those in an ac path cannot be compensated for.

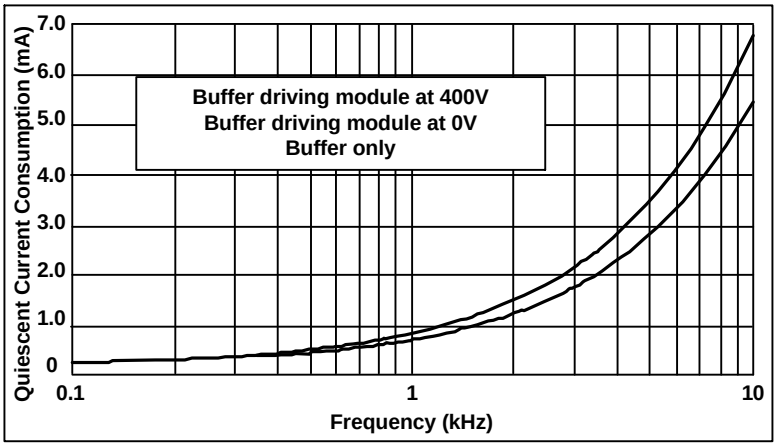


Figure 14. Current consumption vs. frequency

This circuit has been implemented with the printed circuit board included in the IR2110 Bridge Driver Designer's Kit (part number IR2119), as shown in Figure 5b. To eliminate the effects of the inductance of the wiring between the power supply and the test circuit, a 100µF/250V electrolytic capacitor was connected between Q1D and Q2S terminals, as shown in Figures 6 and 7. This virtually eliminates any stray inductance in the dc path. The associated waveforms are shown in Figure 8. When Q_1 turns off, the body diode of Q_2 carries the freewheeling current. The voltage spike across the freewheeling diode is approximately 10V, as shown in the top trace, due to the forward recovery of the diode and the internal packaging inductances.

However, the corresponding negative spike at pin 5 of the IR2110 is 50V, as shown by the lower trace. This is caused by the di/dt in the stray inductances L_{D2} and L_{S2} in the ac path and the fact that these inductances effectively isolate pin 5 from the clamping action of the freewheeling diode. The severity of the problem can be understood considering that by switching 10A in 20ns with a stray inductance of 50nH, a 25V spike is generated. A small paper clip has an inductance of 50 nH. The most effective way of dealing with this spike is to reduce the stray inductance in the ac path. This can be done by mounting the source or emitter of the high-side device very close to the drain or collector of the low-side device, as shown in the layout of Figure 10.

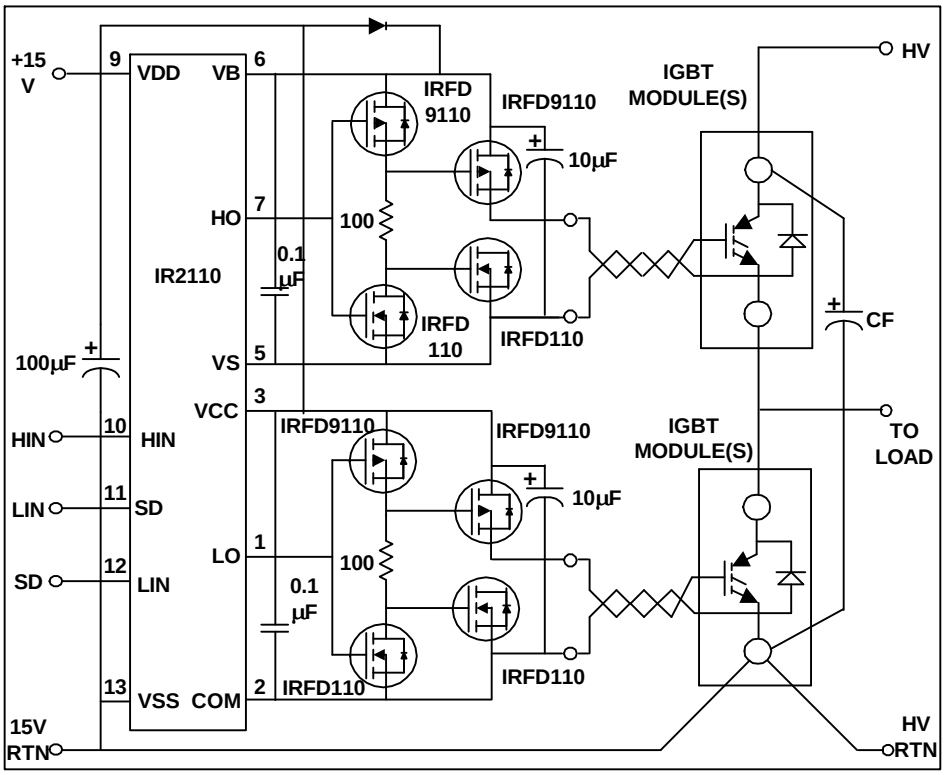


Figure 15. Application circuit schematic

After this inductance has been reduced to the lowest practical limit, the di/dt may have to be reduced by reducing the switching speed by means of the gate resistor. Driving MOS-gated power transistors directly from the IR2110 or similar MGD can result in unnecessarily high switching speeds. The circuit shown in figure 5b produced 4ns turn-off time with 0Ω series gate resistance and generated a negative spike of 90V at pin 5 of the IR2110. A graph of the negative spike and the turn-off time versus series gate resistance is shown in Figure 9.

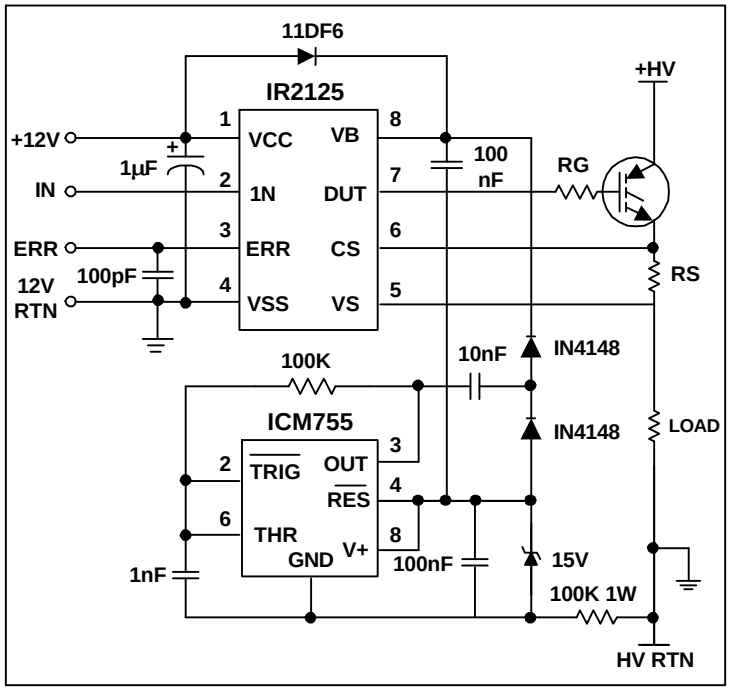


Figure 16. High-side drive provides fast switching, continuous on-tome and protection for the switching device.

Increasing the value of the series gate resistor, the amplitude of the negative spike decreases rapidly, while the turn-off time is a linear function of the series gate resistance. Selecting a resistor value just right from the "knee" in Figure 9 provides a good trade-off between the spike amplitude and the turn-off speed. A 27Ω speed gate resistor was selected for the test circuit which resulted in an 18V spike amplitude and set the turn-off time to 48ns. A parallel diode, with the anode towards the gate, across the gate resistor is also recommended. The diode is reverse biased at turn-on but holds the gate down at turn-off, and during the off state. The reduction in the turn-on speed reduces the spike of reverse recovery, as explained in Section 12 (see also Ref 2). The value of gate resistor should be as low as the layout allows, in terms of overvoltage on the device and negative spikes on the V_S pin.

The layout should also minimize the stray inductance in the charge/discharge loops of the gate drive to reduce oscillations and to improve switching speed and noise immunity, particularly the "dv/dt induced turn-on". To this end, each MOSFET should have a dedicated connection going directly to the pin of the MGD for the return of the gate drive signal. Best results are obtained with a twisted pair connected, on one side, to gate and source, on the other side, to gate drive and gate drive return.

On PC boards parallel tracks should be used. The layout shown in Figure 10 is reduces the stray inductances in the ac path, in the dc path, as well as the stray inductance in the gate drive loop. In this circuit the voltage differential measured between the gate pin of the power MOSFET and the drive pin of the IR2110 during a fast transient was in excess of 2V.

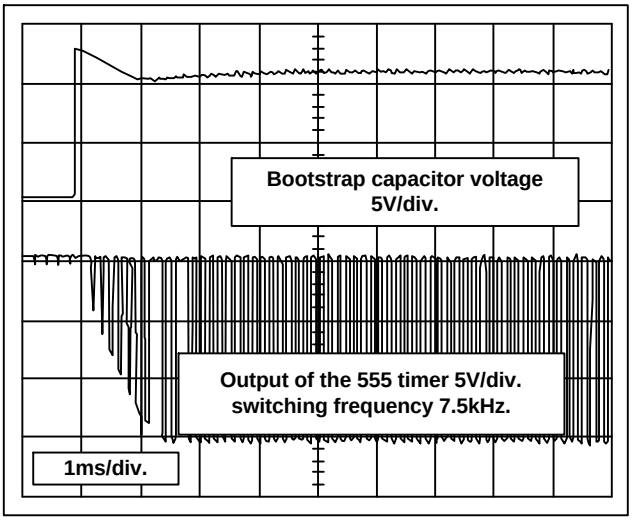


Figure 17. Waveform at start-up.

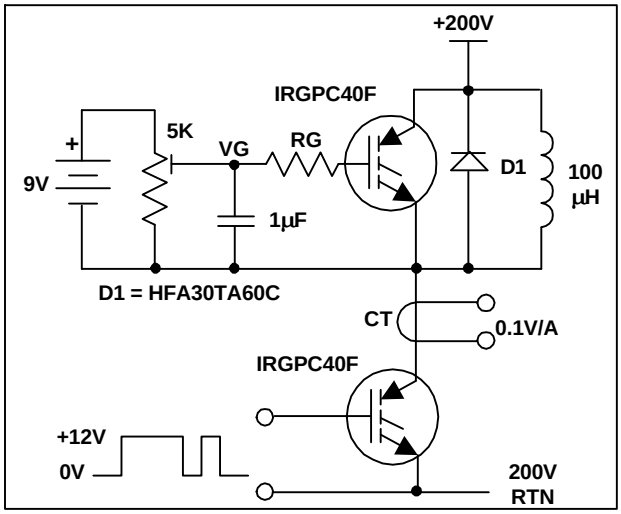


Figure 18. Test circuit

7. HOW TO BOOST GATE DRIVE CURRENT TO DRIVE MODULES

Modules and other paralleled MOS-gated power transistors require significantly more current and lower gate drive impedance than what a typical MGD can provide. The high input impedance power buffer shown in Figure 11 delivers 8A peak output current. It can be mounted close to the power module, thus reducing the inductance of the gate drive loop and improving the immunity to dv/dt induced turn-on. It draws negligible quiescent current and can still be supplied by a bootstrap capacitor. The buffer receives its drive signal from the IR2110 or, preferably, an MGD with lower gate drive capability, and drives an IGBT module which has a total gate charge of 600 nC. Q1 and Q2 are low current drivers for Q3 and Q4 which can be sized to suit the peak output current requirement. When the input signal changes state, R1 limits the current through Q1 and Q2 for the few nanoseconds that both transistors are on. When the input settles to its new state, the driver transistor quickly discharges the gate capacitance of the conducting output transistor forcing it into off-state. Meanwhile the gate of the other output transistor will be charged through R1; the turn-on will be delayed by the RC time constant formed by R1 and the input capacitance of the output transistor.

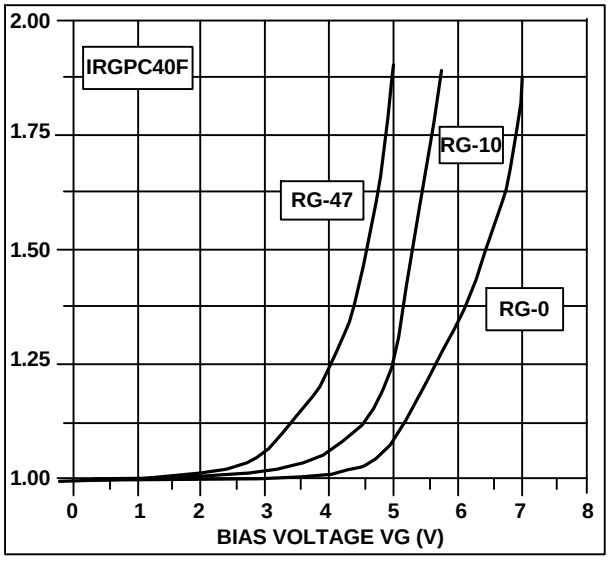


Figure 19. Turn-on losses vs. VG

The typical switching performance while driving an inductive load current of 60A is shown in Figure 12. Turn-on and turn-off delays are 50nS. Rise and fall times are less than 40nS. The buffer was tested with a 0.1µF capacitive load, as shown in Figure 13. The ringing was due to the resonant circuit at the output, formed by the capacitive load and the stray inductances. The current consumption vs. frequency plot is shown in Figure 14. It is possible to use lower on-resistance, lower voltage HEXFETs in the booster stage, but it was found that the large reduction in $R_{DS(on)}$ gave rise to large peak currents which caused a great deal of noise and ringing in the circuit.

A typical use for this buffer is shown in Figure 15. Use good quality 10 µF tantalum or 10 µF electrolytic and 0.l µF ceramic capacitors at the output of the buffer. These decoupling capacitors should be mounted physically close to the output HEXFETs to nullify the effects of stray inductance. They reduce the ringing at the gate during turn-on.

Use short, tightly twisted wires between the output of the buffers and the modules. Use a single point ground at the emitter of the bottom IGBT module. In a bridge configuration, connect the emitters of the bottom IGBT modules to a common point with short heavy wires. Use this point as a common ground.

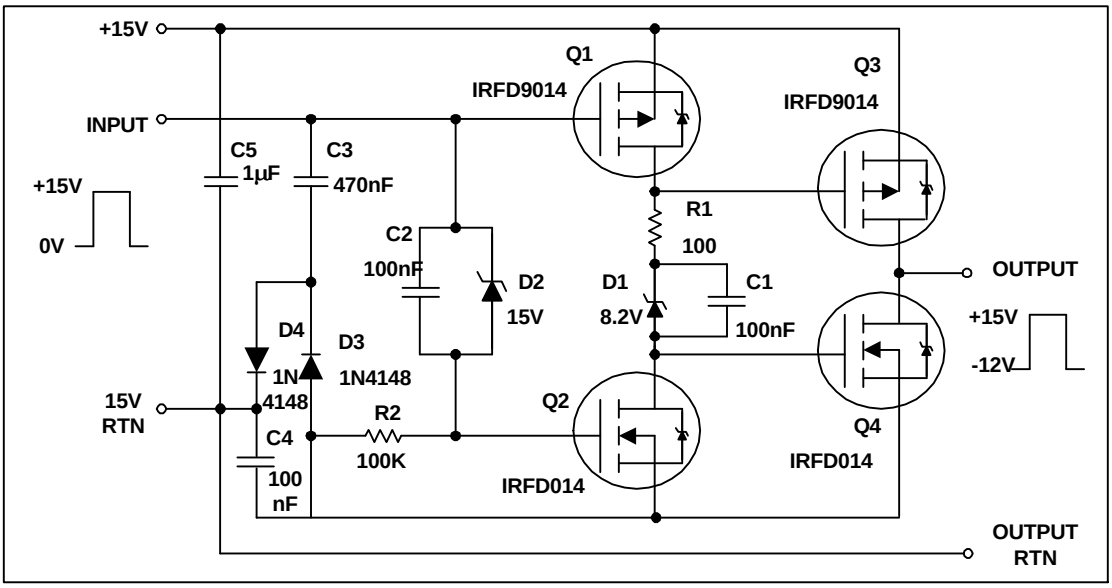


Figure 20. Buffer with negative charge pump

8. HOW TO PROVIDE A CONTINUOUS GATE DRIVE

Some applications, like brushless dc motors, require that the high-side device be on for an indefinite period of time. Under these conditions the charge in the bootstrap capacitor. Isolated supplies are normally used for this purpose.

They add cost and are frequently responsible for spurious turn-on of the power devices due to the coupling of the switching dv/dt through the interwinding capacitance of their transformer. An inexpensive alternative to an isolated supply is the charge pump circuit shown in Figure 16. The IR2125 MGD was selected to demonstrate the cooperation of the charge pump and the bootstrap circuits. The IR2125 also has linear current limiting and time-out shut down capability, providing protection for the MOS-gated device. To provide the low operating current requirement of the IR2125, the charge pump employs a CMOS version of the 555 timer.

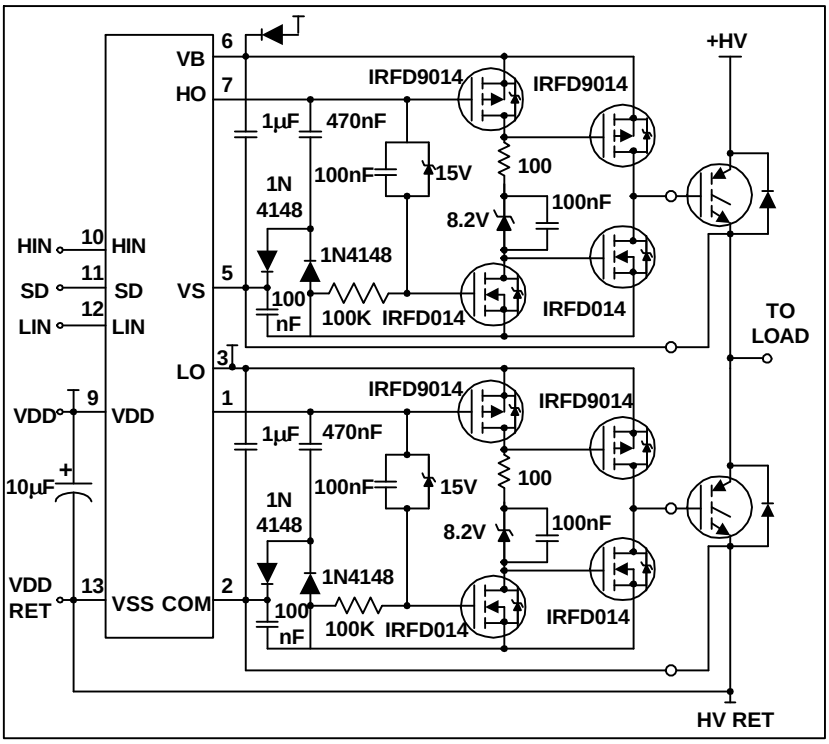


Figure 21. Half-Bridge drive that generates negative bias

When the IGBT is off, the bootstrap capacitor is charged through the bootstrap diode and the load resistor. When the IGBT is on, the 100k resistor connected to ground charges the 100nF capacitor connected between pins 1 and 8 of the 555 timer generating -15V referenced to pin 5 of the IR2125. The charge pump circuit formed by the two lN4148 diodes and the 10nF capacitor which converts the 7.5kHz square wave at pin 3 of the 555 timer to + 15V referenced to V_S and charges the bootstrap capacitor.

Figure 17 shows the circuit waveforms at start-up. As the IGBT turns on, the bootstrap diode disconnects pin 8 of the IR2125 from the +12V power supply, and the voltage across the bootstrap capacitor starts dropping. At the same time the 100k resistor located between pin 1 of the 555 timer and ground starts charging the 100nF capacitor connected to it and generates supply voltage for the CMOS (MAXIM ICL71555IPA) timer.

The output voltage of the charge pump increases with increasing supply voltage. The charge pump maintains the voltage in the bootstrap capacitor, keeping the voltage above the undervoltage threshold level of the IR2125.

The following considerations should be kept in mind in the selection of the components:

- In selecting the zener, consider that he absolute maximum voltage supply voltage for the 555 is 18V

- The 100k lW resistor should be sized according to the maximum supply current at the high side of the IR2125, the minimum operating power supply voltage and the timing requirements

- The supply current at the V_B pin (I_{QBS}) of the IR2125 increases with increasing temperature

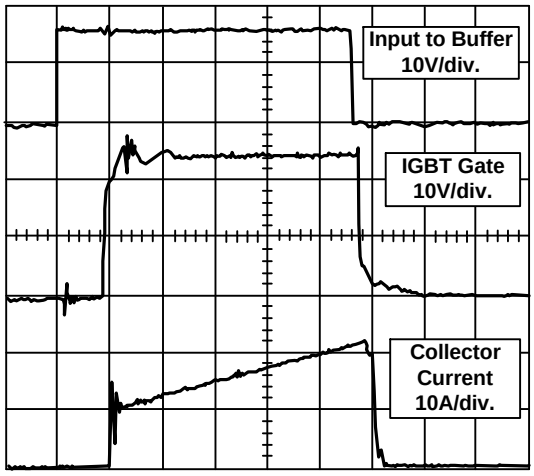


Figure 22. Waveform from negative bias Half-Bridge driver (1ms/div.)

9. HOW TO GENERATE A NEGATIVE GATE BIAS

Inherently neither the MOSFET nor the IGBT requires negative bias on the gate. Setting the gate voltage to zero at turn-off insures proper operation and virtually provides negative bias relative to the threshold voltage of the device. However, there are circumstances when a negative gate drive is necessary:

- The semiconductor manufacturer specifies negative gate bias for the device,
- When the gate voltage can not be held safely below the threshold voltage due to noise generated in the circuit.
- The ultimate in switching speed is desired

Although reference will be made to IGBTs, the information contained is equally applicable to power MOSFETs. The IGBTs made by International Rectifier do not require negative bias. The switching times and energy loss values that are published on the data sheets for both discretes and modules were measured at zero gate voltage turn-off. The problem of “dv/dt induced turn-on” arises when the voltage increases rapidly between the collector-emitter terminals of the IGBT.

During the transient, the gate-collector (Miller) capacitance delivers charge to the gate, increasing the gate voltage. The height and width of the voltage 'blip' at the gate is determined by the ratio of the gate- collector and gate-emitter capacitances, the impedance of the drive circuit connected to the gate, and the applied dv/dt between the collector-emitter terminals.

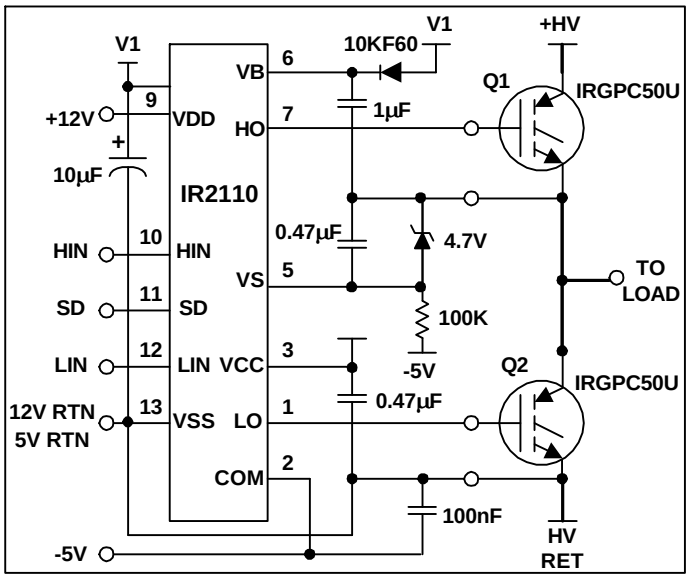


Figure 23. Half-Bridge driver with external negative bias

The following test was conducted to determine the threshold voltage and the effect of the series gate resistance in high dv/dt applications. The test circuit is shown in Figure 18. The positive bias to the upper IGBT was increased until the switching losses in the bottom IGBT indicated excessive shoot-through current. The turn-on loss was measured at 15A inductor current and 6V/ns switching speed. The results are shown in Figure 19.

The threshold voltage levels increasing the turn-on losses are 4V, 5V and 5.6V with 47Ω, 10Ω, and 0Ω series gate resistance, respectively. A parallel diode across the series gate resistor (anode toward the gate) helps clamp the gate low, so the series gate resistor can be sized according to the turn-on requirements. The current 'blip' due to charging the output capacitance (C_{oes}) of the IGBT is frequently mistaken for conduction current. The amplitude of the current 'blip' is approximately 5A for a IRGPC50F IGBT at a dv/dt of 20V/ns. The amplitude of the 'blip' does not change with the applied negative bias.

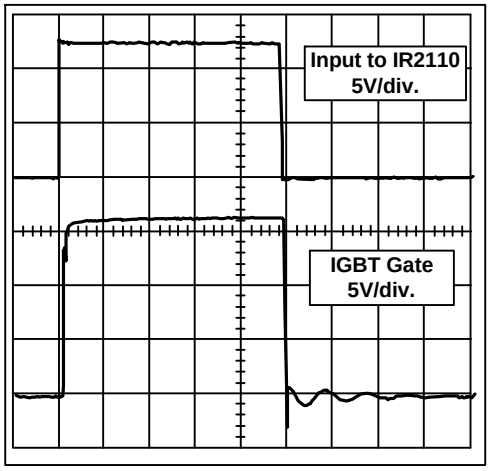


Figure 24. Waveform from circuit shown in Figure 23 (2ms/div)

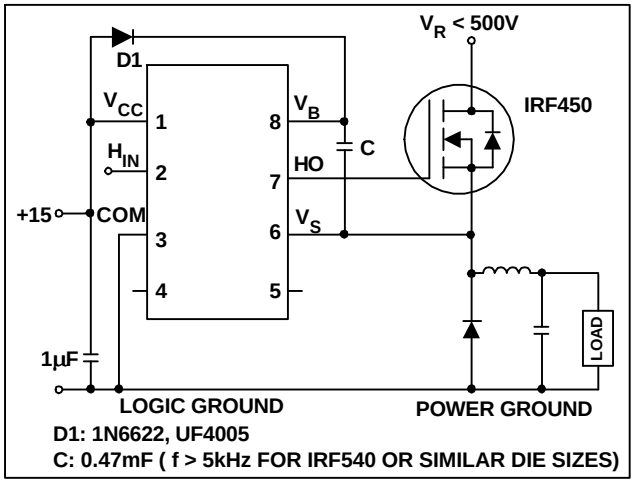


Figure 25. Buck Converter

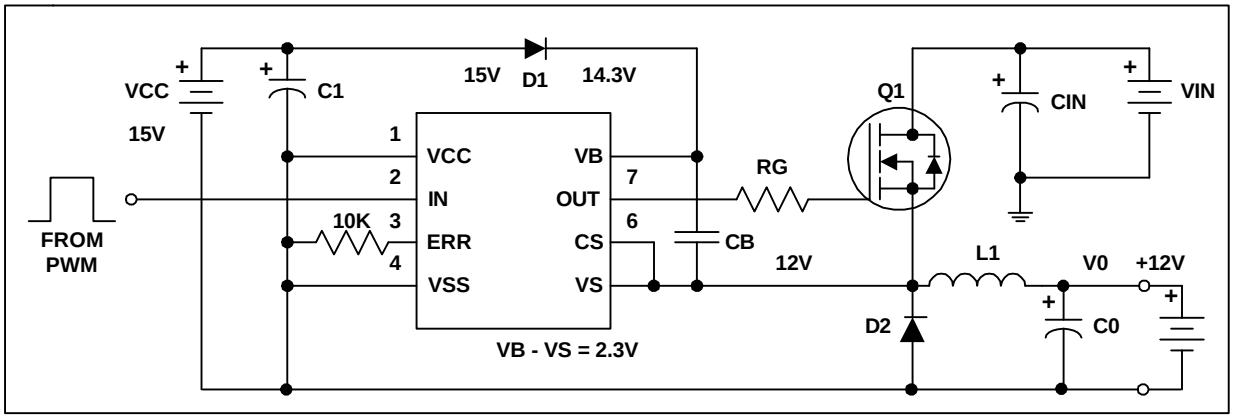


Figure 26. In battery charger applications, the +12V from the output appears at the V_S pin and reduces the voltage across CB at start-up and the undervoltage protection in the IR21XX inhibits the operation.

The basic buffer circuit and the negative charge pump are shown in Figure 20. The buffer circuit employs two p-channel and two n-channel MOSFETs. Resistor R1 between the gates of Q3 and Q4 slows down the turn-on of the output transistor and limits the shoot-through current in the drivers.

D1 reduces the voltage to the gate of Q3 and Q4. D2, C2 and R2 form a level shifter for Q2. C3, C4, D3 and D4 convert the incoming signal to negative DC voltage. After turn-on, the negative voltage settles in a few cycles even at extremely low or high duty cycles (1-99%). The settling time and the stiffness of the negative voltage are affected by the output impedance of the signal source.

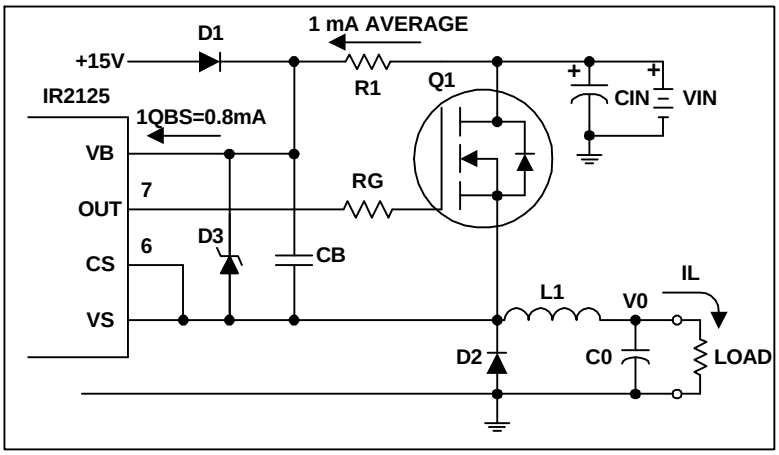


Figure 27. Adding R1 to the circuit, charging current can be derivated from VIN.

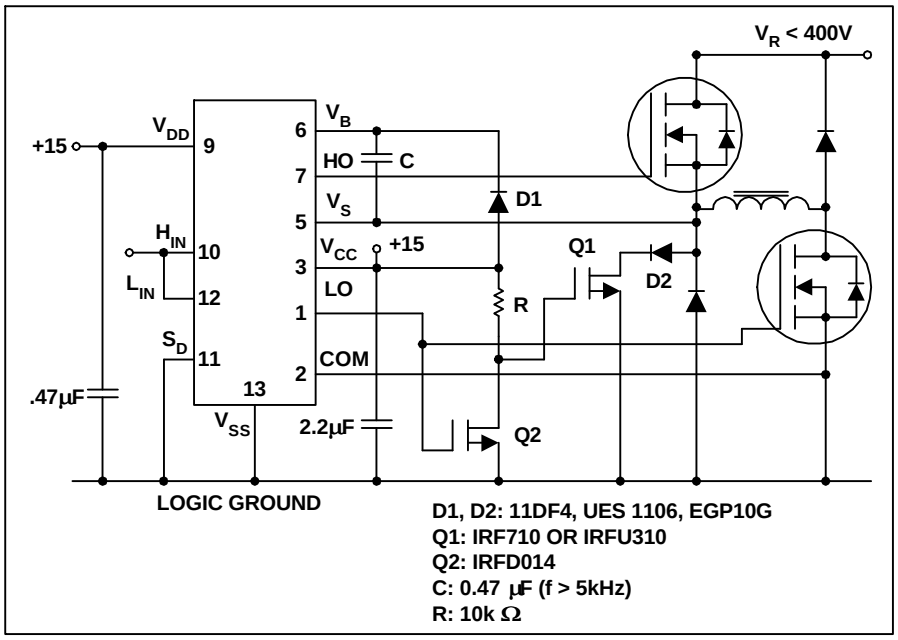


Figure 28. Dual forward converter and switched reluctance motors

The circuit shown in Figure 21 utilizes the high voltage level shifting capability of the IR2110 combined with the drive capability and negative bias of the MOS buffer shown in Figure 20. The circuit was tested with two 270 A IGBT modules with 600 nC of gate charge. The waveforms are shown in Figure 22. The turn-on delay of the circuit is 1 µS, the turn-off delay is 0.2 µS .

The settling time of the negative bias voltage is about 10ms at 5kHz switching frequency at 50% duty cycle. At start-up, the circuit delivers some negative gate voltage even after the first cycle. During power down, the gate voltage remains negative until the reservoir capacitor discharges. A simpler circuit is shown in Figure 23. Input and output waveforms are shown in Figure 24. The negative voltage is provided by an external power supply, while the negative bias voltage for the high-side is generated by a 100k resistor and a zener diode. The negative gate voltages are limited to the maximum applicable offset voltage between the V_{SS}-COM and V_{SS}-VS pins. The total power supply voltage to the IR2110 cannot exceed 20V. The 100k resistor is sufficient for HV=160V, 50% duty cycle operation. Different operating conditions may require different resistor values. The average current through the resistor should be at least 1mA. The power handling capability and maximum operating voltage of the resistor also have to be considered. Since the operating current of the zener diode is small, the special low current ones are preferable in this application.

10. HOW TO DRIVE A BUCK CONVERTER

Figure 25 shows a typical implementation of a buck converter with the high side drive function performed by the IR2117. The diode connected on COM prevents the negative spikes from affecting the operation of the IC and provides an extra measure of noise immunity. As mentioned before, COM *should not* be connected together.

At start-up the bootstrap capacitor is discharged and, in most applications would charge through the inductor and the filter capacitor. The same is true under no-load conditions, when the freewheeling diode may not conduct at all. This alternative path works, as long as the filter capacitor is at least 10 times larger than the bootstrap capacitor. The Q of this resonant circuit should be low enough to insure that the bootstrap capacitor does not get charged beyond the limits of V_{SS} (20V). If this is not so, a zener in parallel with the bootstrap capacitor would take care of possible overvoltages. This is true whether the dc-to-dc converter performs the function of a supply or speed control for a dc motor.

In the following two cases, however, the recharging current for the bootstrap capacitor cannot flow neither in the diode, nor in the load:

1. In a typical battery charger applications, as the one shown in Figure 26, the +12V from the output appears at the V_S pin and reduces the voltage across bootstrap capacitor at start-up and the undervoltage protection in the MGD inhibits the operation.

2. When the regular PWM operation of the buck is interrupted due excessive voltage at the output. This is normally due to a sudden removal of a heavy load at the output which results in higher output voltage than the set value due to the limited speed of the control loop and the stored energy in the Ll inductor. With no load or light load at the output, the filter capacitor can keep the output high for long time while the CB is being discharged at faster rate by the leakage current of the high-side driver.

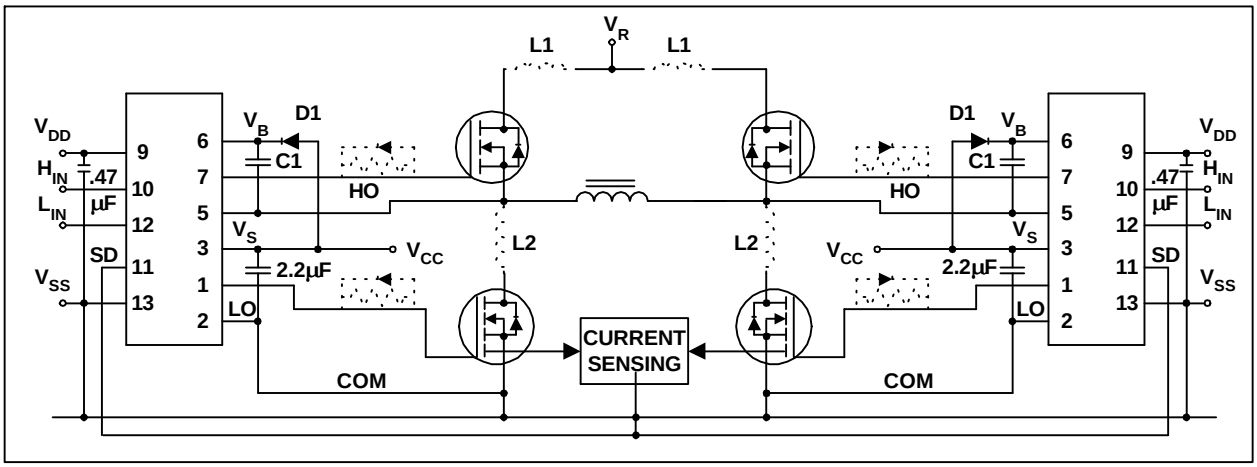


Figure 29. Typical implementation of all H-Bridge with cycle-by-cycle current mode control

As shown in Figure 27, the addition of R1 provides an alternative charging path for the bootstrap capacitor. Because V_{IN} is higher than V_O, some charging current always flows through R1 even if V_S pin is sitting at V_O potential.

To keep CB charged the average current through R1 should be higher than the worst case leakage current. D3 should be a low level zener diode with sharp knee at low currents. The recommended part numbers for 12V and 15V are respectively: lN4110 and lN4107.

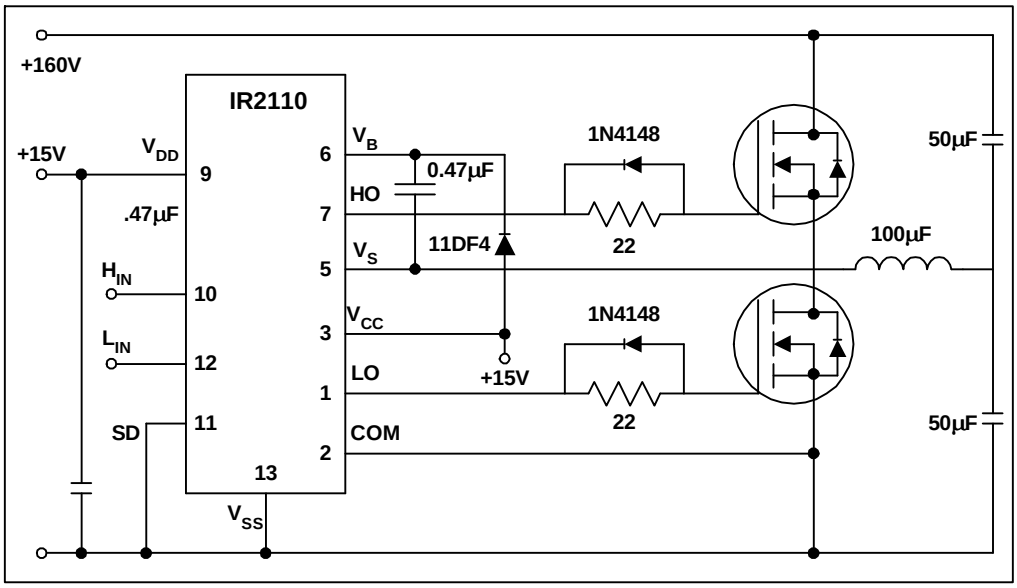


Figure 30a. Test circuit for waveforms shown in Figure 30b. IRF450 operated at approximately 100kHz in a 100 mH inductor.

This technique can also be used in place of a dedicated supply to power the PWM controller, as well as the IR2110 and other auxilliary circuits, if the output voltage of the buck converter is between 10 and 20V.

11. DUAL FORWARD CONVERTER AND SWITCHED RELUCTANCE MOTOR DRIVES

Figure 28 shows a bridge arrangement that is frequently used to drive the windings of a switched reluctance motor or a transformer in a dual forward converter.

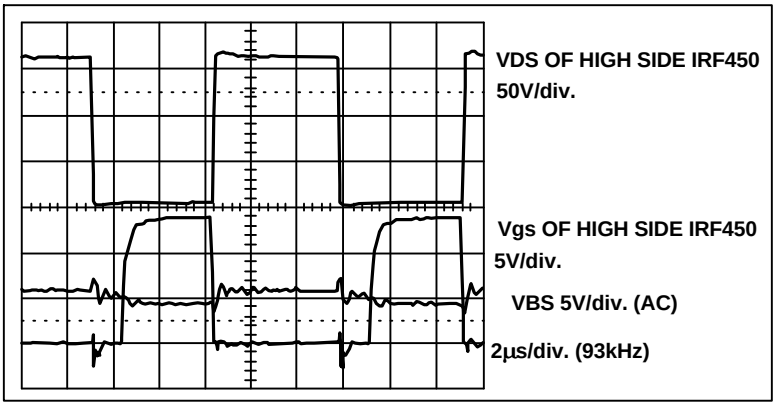


Figure 30b.

The use of the IR2110 requires the addition of four to insure that the bootstrap capacitor is charged at turn on and in subsequent cycles, should the conduction time of the freewheeling diodes become very short.

12. FULL BRIDGE WITH CURRENT MODE CONTROL

Figure 29 shows an H bridge with cycle-by-cycle current control implemented with current sensing devices on the low side in combination with the shutdown pin of the IR2110. The detailed implementation of the current sensing circuit is dependent on the PWM technique used to generate the desired output voltage, the accuracy required, the availability of a negative supply, bandwidth, etc. (Ref. 3, 4 and 5 cover these aspects in greater detail). As explained in Section 2.1, the shutdown function is latched so that the power MOSFETs will remain in the off-state as the load current decays through their internal diodes. The latch is reset at the beginning of next cycle, when the power devices are once again commanded on. As shown in Figures 6 and 7, decoupling capacitors mitigate the negative effects of L_1 . L_2 , on the other hand, must be reduced with a tight layout, as per Figure 10. The turn-on and turn-off propagation delays of the IR2110 are closely matched (worst case mismatch: 10ns), with the turn-on propagation delay 25ns longer than the turn-off. This, by itself, should insure that no conduction overlap of the power devices would occur, even if the on and off input command coincide. As an added safety margin a resistor diode network can be added to the gate, as shown with dashed lines in Figure 29. The purpose of this network is to further delay the turn-on, without affecting the turn-off, thereby inserting some additional dead-time. The resistor-diode network is also useful in reducing the peak of the current spike during the reverse recovery time. As explained in Ref. 2, this has an impact on power losses, as well as dv/dt and EMI. Figure 30 shows the waveforms taken from a test circuit laid out as shown in Figure 10. Operation at 500kHz with the IRF830 HEXFET did not present any problem nor cause any noticeable heating of the IR2110.

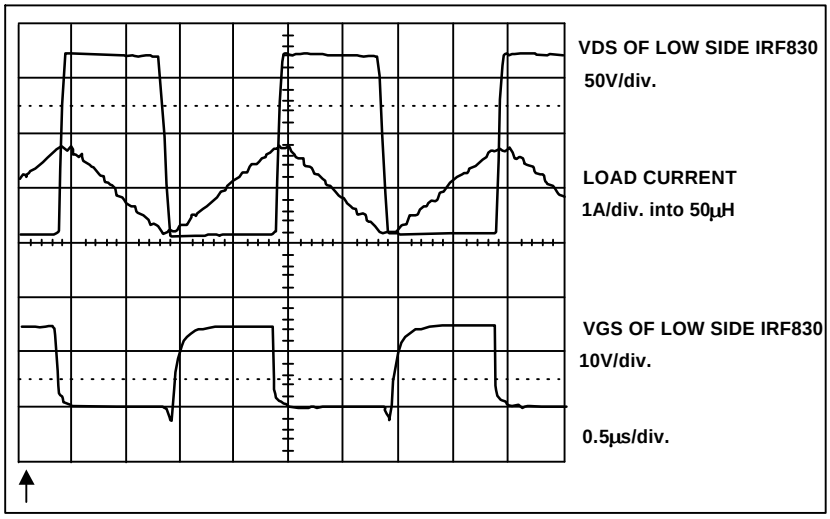


Figure 30c.

13. BRUSHLESS AND INDUCTION MOTOR DRIVES

The implementation of a three-phase bridge for motor drives requires a more careful attention to the layout due to the large di/dt components in the waveforms. In particular, the driver furthest away from the common grounding point will experience the largest voltage differential between COM and the ground reference (Ref. 1).

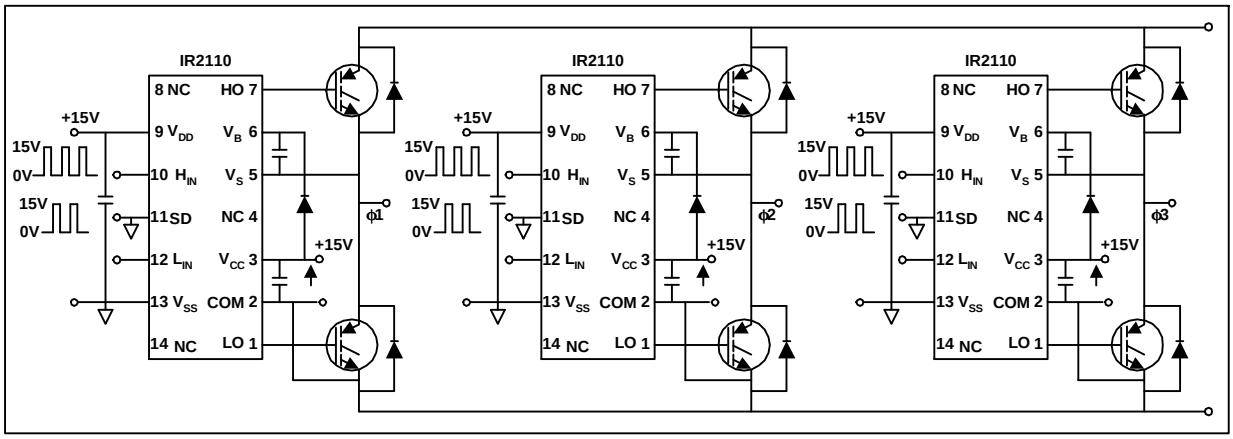


Figure 31. Three-Phase Inverter using three IR2110 devices to drive six IGBTs

In the case of the three-phase drivers, like the IR213x, the guidelines of Sections 5 and 6 should be complemented with the following: Three separate connections should go from the COM pin of the MGD to the three low-side devices. Furthermore, there are several operating conditions that require close scrutiny as potential problem areas.

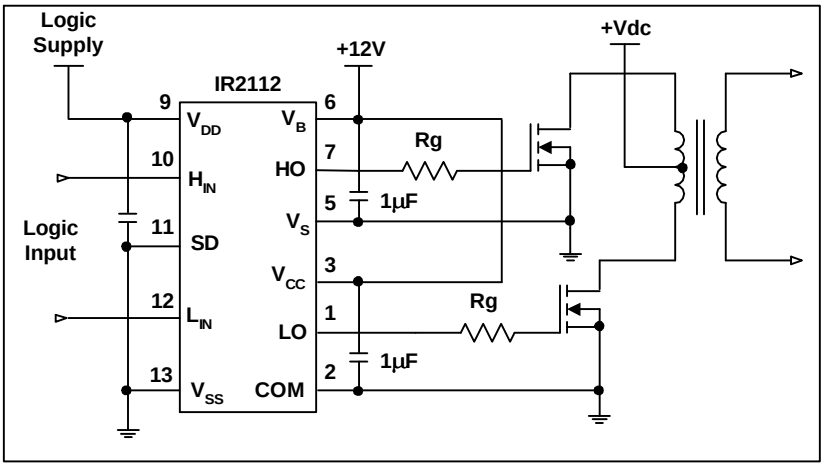


Figure 32. Push Pull Drive Circuit

One such condition could occur when a brushless dc motor is operated with locked rotor for an indefinite period of time with one leg of the bridge being off.
In this condition the bootstrap capacitor could eventually discharge, depending on the voltage seen by V_S during this period of time. As a result the top power device would shut off and would not go on when commanded to do so. In most cases this would not be a cause for malfunction, since the lower device would be commanded on next and the bootstrap capacitor would be charged and ready for next cycle. In general, if the design cannot tolerate this type of operation, it can be avoided in one of four ways:

a. a charge pump could be implemented, as described in Section 8;

b. the control could be arranged to have a very short "normal" duty cycle with a minimum pulse width of a couple of microseconds;

c. if a pole can be inactive for a limited and known period of time, the bootstrap capacitor could be sized to hold up the charge for that time.

d. Isolated supplies could be provided for the high-side, in addition to the bootstrap capacitor.

If the bridge is part of an induction motor drive that use a PWM technique to synthesize a sine wave, each pole goes through prolonged periods of time with zero or very low duty cycle at low frequency. The bootstrap capacitor should be sized to hold enough charge to go through these periods of time without refreshing. In circuits like the one shown in Figure 31, galvanic isolation between the high voltage supply and the logic circuitry is frequently mandated by safety considerations or desirable as a form of damage containment in case of inverter failure.

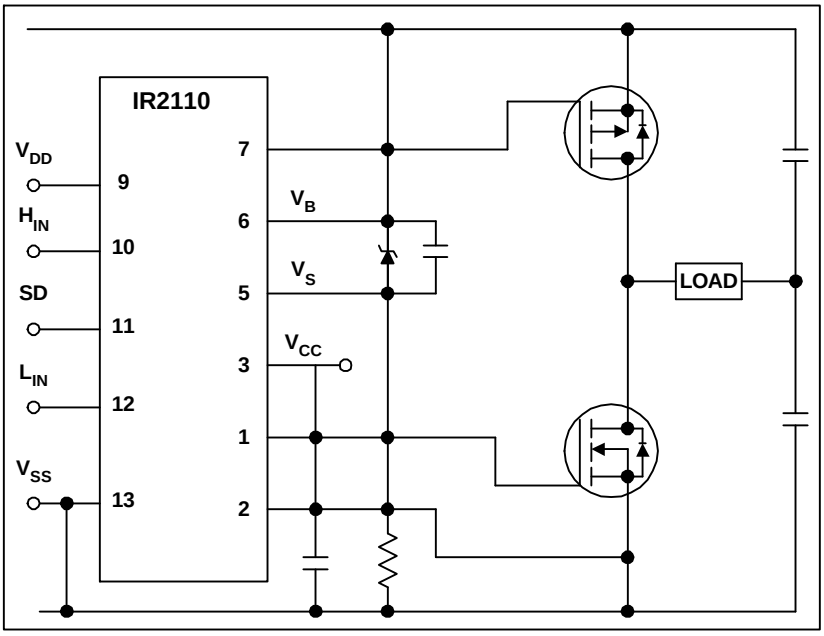


Figure 33. IR2110 driving a high side P-Channel

Optoisolators or pulse transformers are frequently used to perform this function. For drives up to 5 kW, the circuit shown in INT-985 is probably the simplest and most cost-effective way of providing isolation. The use of an MGD shields the optoisolator from the high-voltage dv/dt and reduces their cost while providing a high performance gate drive capability.

14. PUSH-PULL

High-voltage MGDs can still make a very useful contribution in applications that do not capitalize on their key feature, the high voltage level shifting and floating gate drive.

Convenience, noise resilience between V_{SS} and COM and high speed drive capability are appealing features in most power conditioning applications. They can perform the interface and gate drive function with the simple addition of the decoupling capacitors, as shown in Figure 32.

15. HIGH-SIDE P-CHANNEL

MGDs can also drive a P-Channel device as a high side switch, provided that a negative supply referenced to the positive rail is available, as shown in Figure 33. When operated in this mode, the H_{IN} input becomes active low, i.e. a logic 0 at the input turns on the PChannel MOSFET. Whenever V_S (or V_B) are at fixed potential with respect to ground, the power losses mentioned in Section 4.2.d.2 would be zero.

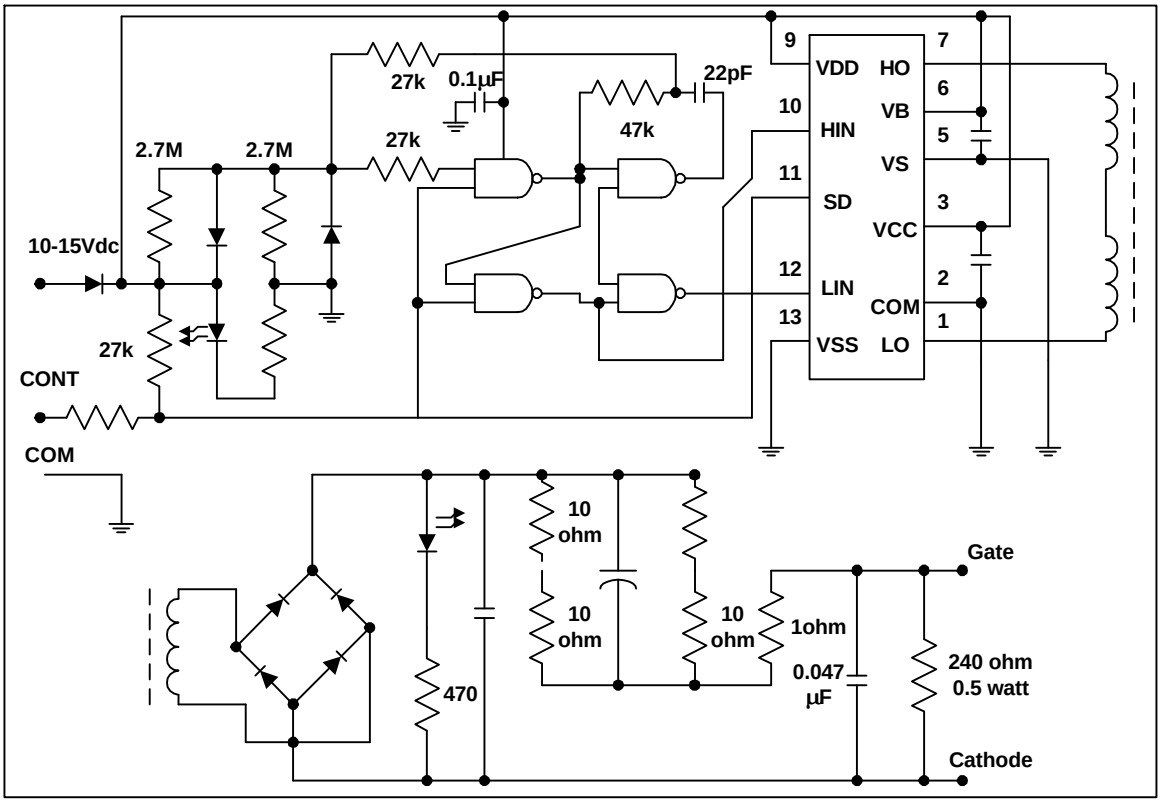


Figure 34. Isolated SCR Gate Drive Circuit

16. THYRISTOR GATE DRIVE

The circuit shown in Figure 34 can provide isolated gate drive to a thyristor, with status feedback. The 2:1 ratio in the gate drive transformer doubles the current available to the gate from what is delivered by the MGD.

17. TROUBLESHOOTING GUIDELINES

To analyze the waveforms of the floating channel of the IR2110 a differential input oscilloscope is required. It is assumed that any voltage differential not referenced to ground is measured in this way.

It is also assumed that obvious checks have been made, for example:

- Pins are correctly connected and power supplies are decoupled.
- The bootstrap charging diode is ultra-fast, rated for the rail voltage.
- The shutdown pin is grounded.
- Logic inputs do not cause simultaneous conduction of devices, unless the topology requires it.

SYMPTOM	POSSIBLE CAUSE
No gate drive pulses	Verify that V_{cc} is above the UV lockout value
Gate drive pulses on lower channel only	Measure voltage across bootstrap capacitor; it should be above the lockout level. If it is not, check why capacitor doesn't get charged. Insure that capacitor is charged at turn-on
Erratic operation of top channel	Verify that V_S doesn't go below COM by more than 5-10V. Verify that high side channel does not go in UV lockout. Verify that dv/dt on V_S with respect to COM does not exceed 50V/ns. If so, switching may need slowing down. Verify that logic inputs are noise-free with respect to V_{SS}. Verify that input logic signals are longer than 50ns.
Excessive ringing on gate drive signal	Reduce inductance of gate drive loop. Use twisted wires, shorten length. If reduction of loop inductance does not bring ringing to acceptable level, add gate resistors.

TABLE 1

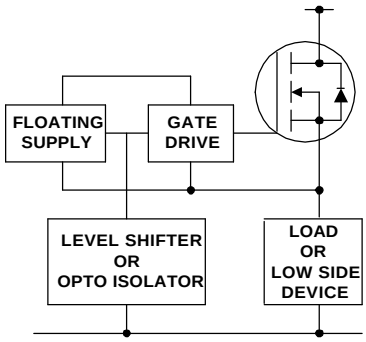
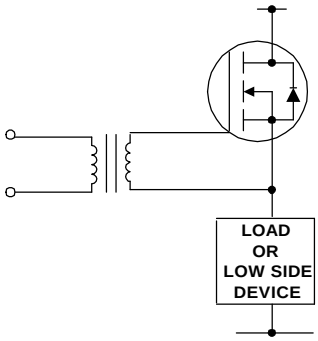
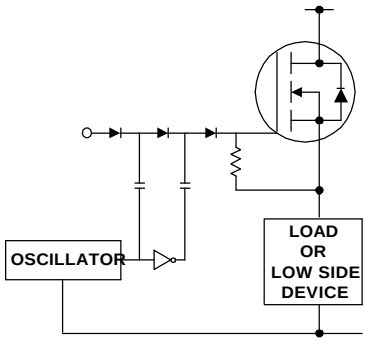
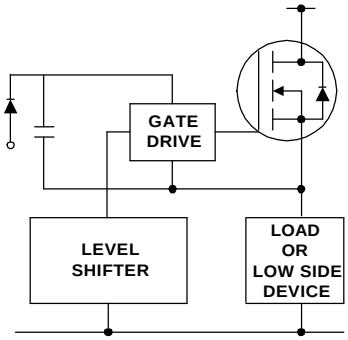
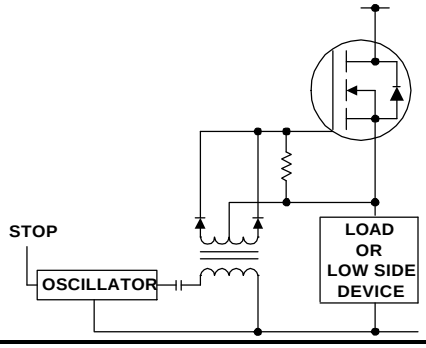
METHOD	BASIC CIRCUIT	KEY FEATURES
FLOATING GATE DRIVE SUPPLY		Full gate control for indefinite periods of time. Cost impact of isolated supply is significant (one required for each high side MOSFET). Level shifting a ground referenced signal can be tricky: Level shifter must sustain full voltage, switch fast with minimal propagation delays and low power consumption. Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive.
PULSE TRANSFORMER		Simple and cost effective but limited in many respects. Operation over wide duty cycles requires complex techniques. Transformer size increases significantly as frequency decreases. Significant parasitics create less than ideal operation with fast switching waveforms.
CHARGE PUMP		Can be used to generate an "over-rail" voltage controlled by a level shifter or to "pump" the gate when MOSFET is turned on. In the first case the problems of a level shifter have to be tackled. In the second case turn on times tend to be too long for switching applications. In either case, gate canb e kept on for an indefinite period of time. Inefficiencies in the voltage multiplication circuit may require more than two stages of pumping.
BOOTSTRAP		Simple and inexpensive with some of the limitations of the pulse transformer: duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. If the capacitor is charged from a high voltage rail, power dissipation can be significant. Requires level shifter, with its associated difficulties.
CARRIER DRIVE		Gives full gate control for an indefinite period of time but is somewhat limited in switching performance. This can be improved with added complexity.

TABLE II			
	Die Size	**Rise Time**	**Fill Time**
Typical switching times for different HEXFET die sizes (Vcc=15V, test circuit as in Figure 9, without gate network)	HEX-2	25ns	17ns
	HEX-3	38ns	23ns
	HEX-4	53ns	34ns
	HEX-5	78ns	54ns
	HEX-6	116ns	74ns

References:

1. "New High Voltage Bridge Driver Simplifies PWM Inverter Design," by D. Grant, B. Pelly. PCIM Conference 1989

2. Application Note AN-967 "PWM Motor Drive with HEXFET III"

3. Application Note AN-961 "Using HEXSense in Current-Mode Control Power Supplies"

4. Application Note AN-959 "An Introduction to the HEXSense"

5. "Dynamic Performance of Current Sensing Power MOSFETs" by D. Grant and R. Pearce, Electronic Letters, Vol. 24 No. 18, Sept 1, 1988