Intelligent Digital Amplifier 4 Channel Controller with Real-Time Feedback for Class-D Audio Amplifier Manufacturers

The D2Audio^{TM} D2-91413 is a fully self-contained 4 channel digital amplifier controller System-On-Chip (SOC). The D2-91413 enables rapid system design for manufacturers of home theater receivers, multi-room distributed audio systems, OEM and Aftermarket Automotive Amplifiers, Powered Subwoofers and Powered Speakers.

The D2-91413 contains a high-performance digital switching controller to play any input source on any output channel.

A configurable audio signal processor provides equalization, volume control, tone control, and compression for each channel, also crossover and power limiting for powered speaker applications

The D2-91413 includes 4-channels I^{2}S/Left-Justified inputs (16 to 24-bit, 16kHz to 192kHz), optional SPDIF receiver (16 to 24-bit).

Boot options include external serial ROM, asynchronous serial, and asynchronous SRC.

Features

• Powerful Digital Audio Management - Reference Design Dependant SRC, Routing, Mixing, Multiple Digital Audio I/O, Tone Control, Parametric EQ, Compression

• Reduced Audio System Cost for manufacturers of Class D Audio amplifiers

• Audio Processing features enable optimized speaker performance and delivers dramatically improved sound quality.

• Minimum Development Cost/Risk/Time-to-Market

• Pure Digital Path

• Superior Dynamic Range

• >110dB SNR, <0.1% THD+N

• ±0.5dB Frequency Response (20Hz - 40kHz)

Complete Class-D Amplifier Controller SOC

• Advanced 4 Channel Digital Switching Controller with Integrated Digital Audio Engine^{TM}

• Flexible Audio Input Sources

• World's First and Only All-Digital, PCM Input, Audio Amplifier Controller with Real-Time Feedback and Power Supply Feed-forward Capability

• Multiple Controller Synchronization

• Support for both Bridge and Non-Bridged Output Topologies

• Stand-Alone or Microcontroller Boot Options (Two-Wire and SPI^{TM})

High-Performance Sound

• Unique performance for each part number

• Superior Dynamic Range

• Up to >115 dB SNR (Open Loop)*

• Up to >118 dB SNR (Closed Loop using CS5381 ADCs)*

• Less than 0.01% THD+N (1W, 1kHz, 8Ω, Open Loop)*

• Less than 0.001% (1W, 1kHz, Load Independent, Closed Loop)*

• ±0.5dB Frequency Response (1W, 20Hz ~ 20kHz, 8Ω, Open Loop)

• ±0.25dB Frequency Response (1W, 20Hz ~ 20kHz, 8Ω, DF Enabled)

Graceful Protection and Recovery

• Complete short-circuit, over-current, and over-voltage fault protection

Pure Digital Path

• Multiple Digital Audio Inputs which support I^{2}S and Left-Justified Formats with Linear PCM (32kHz to 192kHz, 16 to 24-bit)

• Digital Audio Input which supports S/PDIF format with Linear PCM (32kHz to 192kHz, 16 to 24-bit, IEC60958 Compliant)

Device Summary

• D2-91413-LR: Ultra-High-End Performance Solution. 4-Channel PWM Controller with Integrated Digital Audio Engine^{TM} with Digital Feedback (DF) and Digital Power Supply Correction (DPSC), 128-Pin LQFP, RoHS Compliant

System Control Support

• Reference Design Dependant

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D2-91413 Architecture

FIGURE 1. D2-91413 BLOCK DIAGRAM
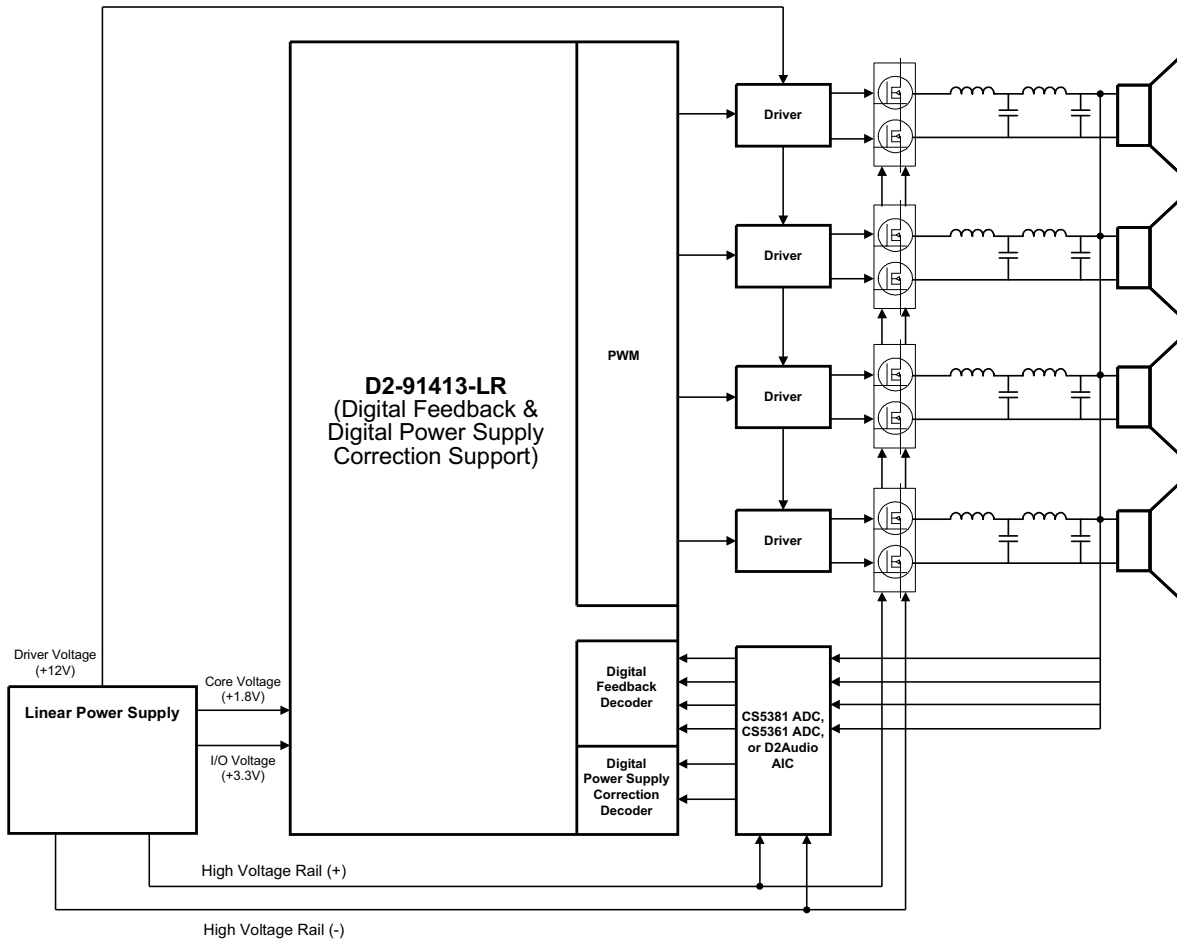
FIGURE 2. D2-91413-LR BLOCK DIAGRAM

D2-91413 Signal Flow

The D2-91413 supports a wide variety of signal flows that are fully programmable and are reference design dependant. D2-91413 use is to only be used as part of a licensed reference design from D2Audio corporation, and furthermore, each reference design has a set signal flow and associated performance level. See corresponding D2Audio Digital Amplifier datasheets for design-specific signal flows.

Specifications

Absolute Maximum Ratings

TABLE 1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	Unit
Supply Voltage RVDD, PWMVDD		-0.3	4.0	V
Supply Voltage CVDD, PLLAVDD, PLLDVDD, OSCVDD		-0.3	2.4	V
Input Voltage, any input but XTALI		-0.3	RVDD+0.3	V
Input Voltage XTALI		-0.3	OSCVDD+0.3	V
Input Current, any pin but supplies		-	±10	mA
Operating Temperature (Ambient)	T_{MAX}	-40	+85	°C
Junction Temperature	T_{JNC}		+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

Pin Characteristics

T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

TABLE 2. PIN CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High Level Input Drive Voltage (Note 1)	V_{IH}	2.0	-	-	V
Low Level Input Drive Voltage (Note 1)	V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (Note 2) I_{OUT} = -Pad Drive	V_{OH}	RVDD - 0.3	-	-	V
Low Level Output Drive Voltage (Note 2) I_{OUT} = +Pad drive	V_{OL}	-	-	0.3	V
High Level Input Drive Voltage (Note 3)	V_{IHX}	0.7	-	OSCVDD	V
Low Level Input Drive Voltage (Note 3)	V_{ILX}	-	-	0.3	V
High Level Output Drive Voltage OSCOUT pin	V_{OHO}	PLLDVDD - 0.3	-	-	V
Low Level Output Drive Voltage OSCOUT pin	V_{OLO}	-	-	0.3	V
Input Leakage Current	I_{IN}	-		±10	µA
Input Capacitance	Cin	-	9	-	pF
Output Capacitance	Cout	-	9	-	pF

NOTES:

1. All input pins except XTALI

2. All digital output pins

3. For XTALI input overdrive operation only

D2-91413

Power Requirements

Typical supply currents measured at T_A = +25°C, PLL at 300MHz, OSC at 27MHz, core running at 150MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

TABLE 3. POWER REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Core Supply Pins	CVDD	1.7	1.8	1.9	V
		0.01	950		mA
Digital I/O Pad Ring Supply Pins	RVDD	3.0	3.3	3.6	V
		0.01	10		mA
PWM I/O Pad Ring Supply Pins	PWMVDD	3.0	3.3	3.6	V
		0.01	5		mA
Analog Supply Pins (PLL)	PLLAVDD	1.7	1.8	1.9	V
		0.01	10		mA
	PLLDVDD	1.7	1.8	1.9	V
		0.01	2		mA
	OSCVDD	1.7	1.8	1.9	V
		0.01	4		mA

Thermal Characteristics

TABLE 4. THERMAL CHARACTERISTICS

PACKAGE TYPE	AIRFLOW	THETA J_A	THETA J_C	UNIT
128-Pin LQFP	0	25.5	2.0*	°C/W
	1 m/s	19.5		
	2 m/s	17.9		

NOTE: Junction to exposed pad

Switching Characteristics - Serial Audio Port

T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

TABLE 5. SERIAL AUDIO PORT TIMING

| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_cSCLK	SCKRx frequency - SCKR0, SCKR1			12.5	MHz
t_wSCLK	SCKRx pulse width (high and low) - SCKR0, SCKR1	40			ns
t_sLRCLK	LRCKRx setup to SCLK rising - LRCKR0, LRCKR1	20			ns
t_hLRCLK	LRCKRx hold from SCLK rising - LRCKR0, LRCKR1	20			ns
t_sSDI	SDINx setup to SCLK rising - SDIN0, SDIN1	20			ns
t_hSDI	SDINx hold from SCLK rising - SDIN0, SDIN1	20			ns
t_dSDO	SDOUTx delay from SCLK falling			20	ns
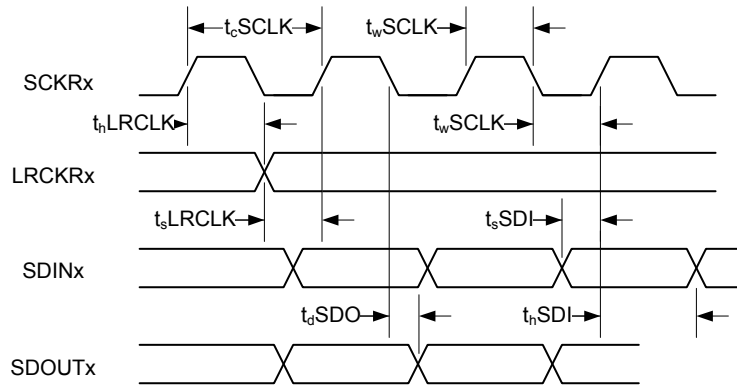
FIGURE 3. SERIAL AUDIO PORT TIMING

SERIAL AUDIO INPUTS (SAI PORTS)

The D2-91413 module contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 192kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^{2}S or Left-Justified data formats.

For I^{2}S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

I^{2}S Format

Left-Justified
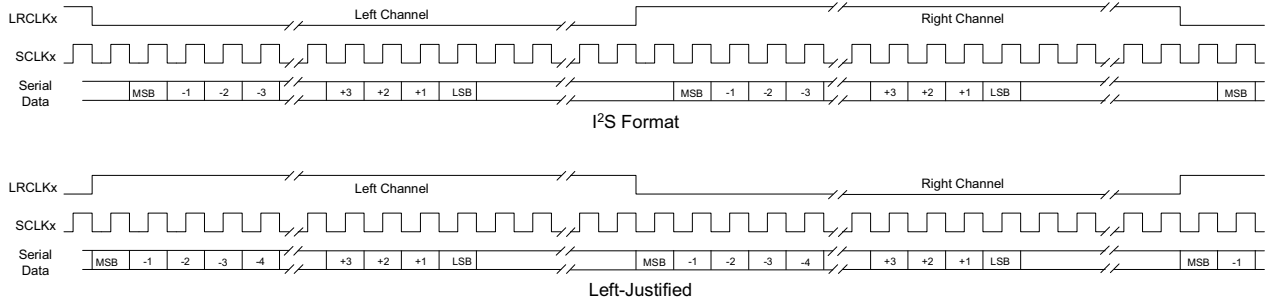
FIGURE 4. SAI PORT DATA FORMATS

Switching Characteristics - 2-Wire Interface

T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

TABLE 6. 2-WIRE INTERFACE PORT TIMING

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
fSCL	SCL frequency		400	kHz
t_{buf}	Bus free time between transmissions	4.7		µs
t_{wlow}SCLx	SCL clock low	4.7		µs
t_{whigh}SCLx	SCL clock high	4.0		µs
t_sSTA	Setup time for a (repeated) Start	4.7		µs
t_hSTA	Start condition Hold time	4.0		µs
t_hSDAx	SDA hold from SCL falling (see note)	0		µs
t_sSDAx	SDA setup time to SCL rising	250		ns
t_dSDAx	SDA output delay time from SCL falling		3.5	µs
t_r	Rise time of both SDA and SCL		1	µs
t_f	Fall time of both SDA and SCL		300	ns
t_sSTO	Setup time for a Stop condition	4.7		µs

NOTE: Data must be held sufficient time to bridge the 300ns transition time of SCL

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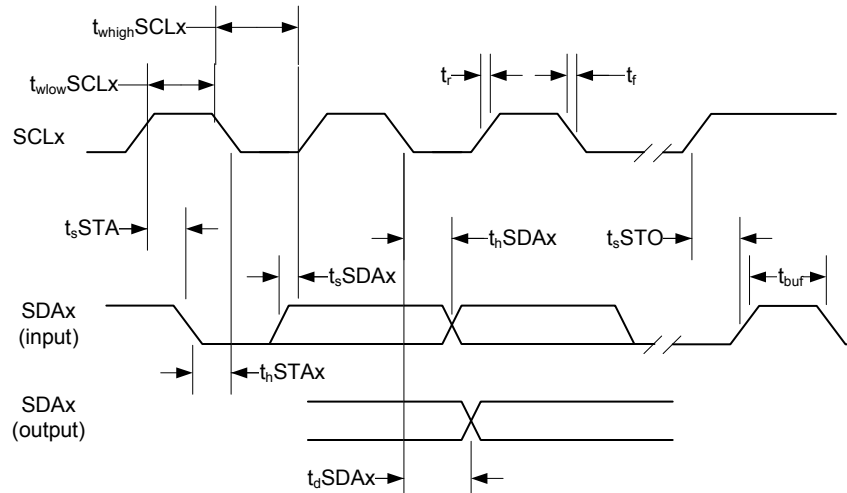
FIGURE 5. 2-WIRE INTERFACE TIMING

Switching Characteristics - SPI^{TM} Interface

T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

TABLE 7. SPI PORT TIMING

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
fSCK	SCK frequency		1	MHz
t_V	MOSI valid from clock edge		2	ns
t_S	MISO setup to clock edge	2		ns
t_H	MISO hold from clock edge	2		ns
t_{WI}	nSS minimum width	3		3 system clocks + 2ns
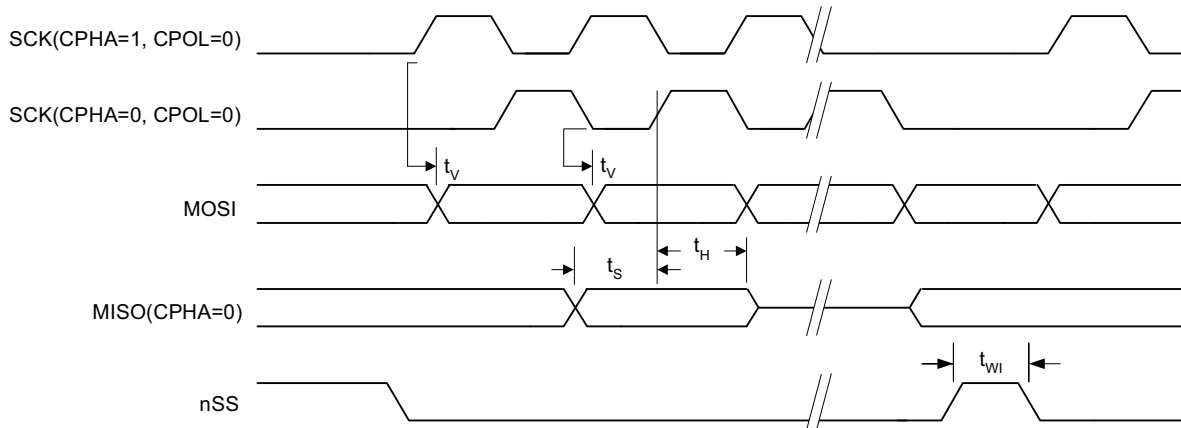
FIGURE 6. SPI TIMING

D2-91413-LR Package Pinout
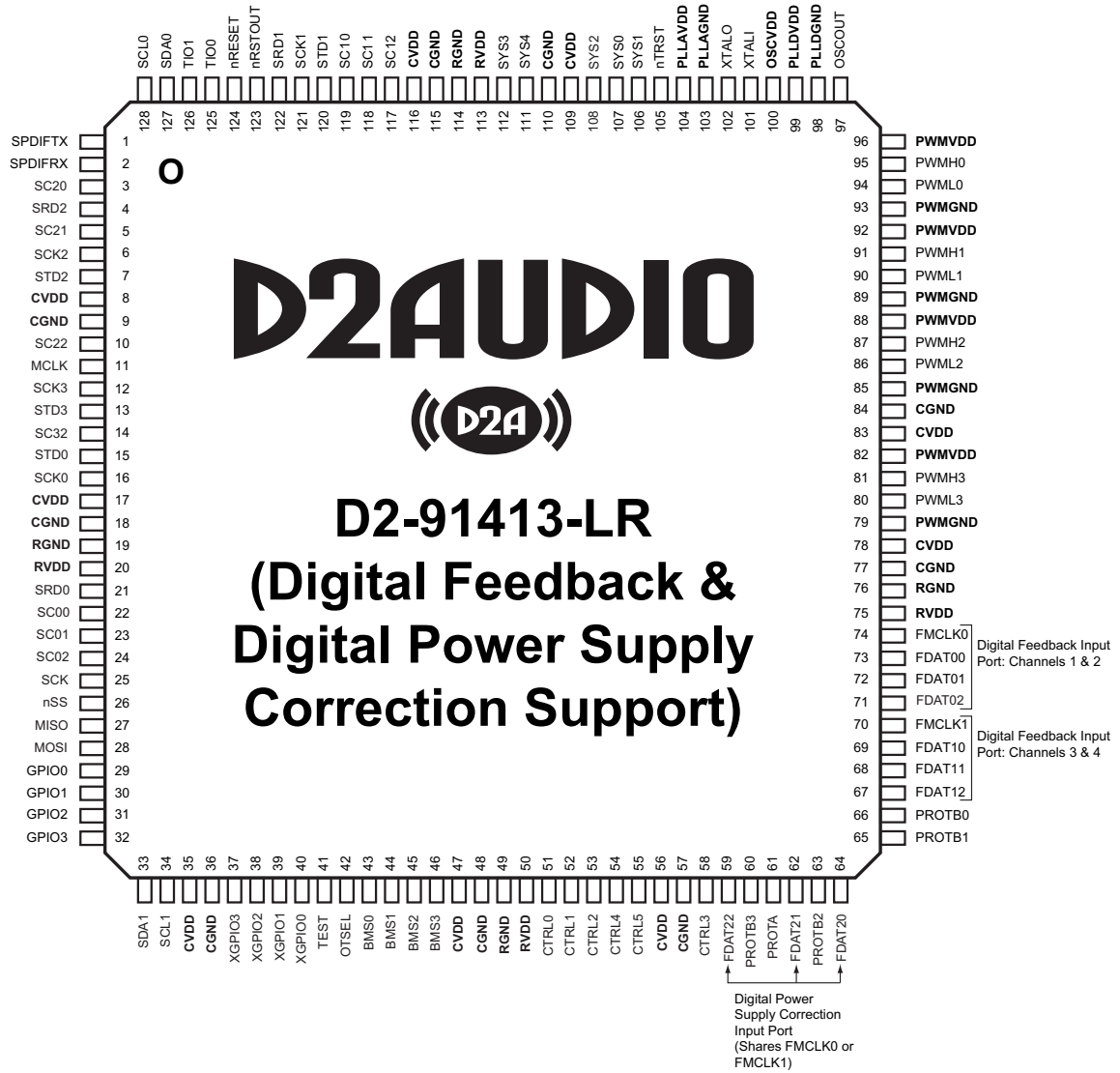
FIGURE 7. D2-91413-LR PINOUT

D2-91413-LR Pin Definitions

TABLE 8. PIN DEFINITIONS

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
SERIAL AUDIO PINS (SAI/SAO)			
11	MCLK	Output	Master clock.
3	SC20	I/O	Serial Audio Bit Clock Receiver 0 (SCKR0)
5	SC21	I/O	Serial Audio Left/Right Clock Receiver 0 (LRCKR0)
4	SRD2	Input	Serial Audio Data In 0 (SDIN0)
6	SCK2	I/O	Serial Audio Bit Clock Receiver 1 (SCKR1)
10	SC22	I/O	Serial Audio Left/Right Clock Receiver 1 (LRCKR1)
7	STD2	Input	Serial Audio Data In 1 (SDIN1)
12	SCK3	I/O	Serial Audio Bit Clock Transmitter (SCKT)

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TABLE 8. PIN DEFINITIONS (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
14	SC32	I/O	Serial Audio Left/Right Clock Transmitter (LRCKRT)
13	STD3	Output	Serial Audio Data Output (SDO)
S/PDIF PINS			
1	SPDIFTX	Output	S/PDIF data output
2	SPDIFRX	Input	S/PDIF data input
PWM PINS			
95	PWMH0	Output	Channel 0 PWM high side output
94	PWML0	Output	Channel 0 PWM low side output
91	PWMH1	Output	Channel 1 PWM high side output
90	PWML1	Output	Channel 1 PWM low side output
87	PWMH2	Output	Channel 2 PWM high side output
86	PWML2	Output	Channel 2 PWM low side output
81	PWMH3	Output	Channel 3 PWM high side output
80	PWML3	Output	Channel 3 PWM low side output
42	OTSEL	Input	Output topology select input
2-WIRE SERIAL PINS			
128	SCL0	I/O	Two wire port 0 serial clock
127	SDA0	I/O	Two wire port 0 serial data
34	SCL1	I/O	Two wire port 1 serial clock
33	SDA1	I/O	Two wire port 1 serial data
SPI PINS			
26	nSS	I/O	SPI slave select IO
25	SCK	I/O	SPI clock IO
27	MISO	Input	SPI master input
28	MOSI	Output	SPI master output
GPIO PINS			
32, 31, 30, 29	GPIO[3:0]	I/O	General purpose I/O
37, 38, 39, 40	XGPIO[3:0]	I/O	General purpose I/O
RESET AND TEST PINS			
124	nRESET	Input	Reset - active low
105	nTRST	Input	Test Reset - active low
123	nRSTOUT	Output	Reset output- active low output
41	TEST	Input	Hardware test pin
CRYSTAL OSCILLATOR AND PLL PINS			
97	OSCOUT	Output	Oscillator output to slave device
101	XTALI	Input	Crystal Oscillator input
102	XTALO	Output	Crystal Oscillator output
AUDIO INTERFACE CHANNEL (AIC) PINS			
74	FMCLK0	Output	Analog Interface Channel Master Clock 0 (Used for Digital Feedback Input Port: Channels 1 and 2)

TABLE 8. PIN DEFINITIONS (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
71, 72, 73	FDAT0[2:0]	Input	Analog Interface Channel Data 0 (Used for Digital Feedback Input Port: Channels 1 and 2)
70	FMCLK1	Output	Analog Interface Control Master Clock 1 (Used for Digital Feedback Input Port: Channels 3 and 4)
67, 68, 69	FDAT1[2:0]	Input	Analog Interface Channel Data 1 (Used for Digital Feedback Input Port: Channels 3 and 4)
59, 62, 64	FDAT2[2:0]	Input	Analog Interface Channel Data 1 (Used for Digital Power Supply Correction Input Port)
SERIAL AUDIO INTERFACE PINS			
16	SCK0	I/O	Serial Audio Interface 0 serial clock port
121	SCK1	I/O	Serial Audio Interface 1 serial clock port
24, 23, 22	SC0[2:0]	I/O	Serial Audio Interface 0 serial control ports
117, 118, 119	SC1[2:0]	I/O	Serial Audio Interface 1 serial control ports
21	SRD0	I/O	Serial Audio Interface 0 serial receive data ports
122	SRD1	I/O	Serial Audio Interface 1 serial receive data ports
15	STD0	I/O	Serial Audio Interface 0 serial transmit data
120	STD1	I/O	Serial Audio Interface 1 serial transmit data ports
SYSTEM CONTROL PINS			
46, 45, 44, 43	BMS[3:0]	Input	Boot mode select
51	CTRL0	I/O	Power supply pump control, high side or GPIO.
52	CTRL1	I/O	Power supply pump control, low side or GPIO
53	CTRL2	I/O	PWM sync
58	CTRL3	I/O	Power supply sync
54	CTRL4	I/O	Power temperature protection
55	CTRL5	I/O	Power over-current protection
107	SYS0	I/O	Reserved for factory test
106	SYS1	Input	
108	SYS2	Input	
112	SYS3	Input	
111	SYS4	Output	
TIMER (TIO) PINS			
126, 125	TIO[1:0]	I/O	Timer I/O ports
PWM PROTECTION PINS			
61	PROTA	I/O	PWM Temperature status input, or GPIO
60, 63, 65, 66	PROTB	I/O	PWM Over Current Protection inputs, or GPIO.
59, 62, 64	PROTC	I/O	PWM Shoot Through Current inputs or GPIO.
POWER PINS			
104	PLLAVDD	Power	PLL Analog power
103	PLLAGND	Ground	PLL Analog ground
99	PLLDVDD	Power	PLL Digital power
98	PLLDGND	Ground	PLL Digital ground

TABLE 8. PIN DEFINITIONS (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
100	OSCVDD	Power	Oscillator power
116, 109, 83, 78, 56, 47, 35, 17, 8	CVDD	Power	Core power - 9 pins
115, 110, 84, 77, 57, 48, 36, 18, 9	CGND	Ground	Core ground - 9 pins
96, 92, 88, 82	PWMVDD	Power	PWM output pin power - 4 pins
93, 89, 85, 79	PWMGND	Ground	PWM output pin ground - 4 pins
113, 75, 50, 20	RVDD	Power	Digital pad ring power - 4 pins
114, 76, 49, 19	RGND	Ground	Digital pad ring ground- 4 pins

Pin Descriptions

Pins are 100% firmware and Reference Design dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

SERIAL AUDIO (SAI/SAO) PINS

MCLK   Master Clock Output

Master Clock output for external ADC/DAC components with 16mA drive strength. Pin drives low on reset.

SC20   SAI Receiver Bit Clock 1

SAI Receiver 0 bit clock is an output when D2-91413 is a master, or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC21   SAI Receiver Left/Right Clock 0

SAI Receiver 0 left/right audio frame clock is an output when D2-91413 is a master or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 8mA drive strength.

SRD2   SAI Receiver Serial Data Input 0

SAI Receiver 0 data input.

SCK2   SAI Receiver Bit Clock 1

SAI Receiver 1 bit clock is an output when D2-91413 is a master, or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC22   SAI Receiver Left/Right Clock 1

SAI Receiver 1 left/right audio frame clock is an output when D2-91413 is a master or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 4mA drive strength.

STD2   SAI Receiver Serial Data Input 1

SAI Receiver 1 data input.

SCK3   SAI Transmitter Bit Clock

SAI Transmitter bit clock is an output when D2-91413 is a master, or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 8mA drive strength. Input has hysteresis.

SC32   SAI Receiver Left/Right Clock

SAI Transmitter left/right audio frame clock is an output when D2-91413 is a master or an input when D2-91413 is a slave. Defaults to an input on reset. Output has 8mA drive strength.

STD3   SAI Receiver Serial Data Output

SAI Transmitter data output with 8mA drive strength.

SPDIF PINS

SPDIFRX   S/PDIF Data Input

This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to proper logic levels.

SPDIFTX   S/PDIF Data Output

This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz with 4mA drive strength.

PWM PINS

PWMxH   PWM High Side Driver Outputs

PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

PWMxL   PWM Low Side Driver Outputs

PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL   Output Topology Select Input

Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

2-WIRE SERIAL PINS

SCL0   Serial Clock 0

Two-Wire Serial clock port 0, open drain driver with 8mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA0   Serial Data 0

Two-Wire Serial data port 0, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

SCL1   Serial Clock 1

Two-Wire Serial clock port 1, open drain driver with 8mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA1   Serial Data 1

Two-Wire Serial data port 1, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

SPI PINS

nSS   Slave Select

SPI slave select IO. May be used as GPIO with 4mA driver. Resets to input.

SCK   SPI Clock

SPI clock IO with hysteresis input. May be used as GPIO with 4mA driver. Resets to input.

MISO   Master In Slave Out

SPI master input, slave output data signal. May be used as GPIO with 4mA driver. Resets to input.

MOSI   Master Out Slave In

SPI master output, slave input data signal. May be used as GPIO with 4mA driver. Resets to input.

RESET AND TEST PINS

nRESET   System Reset Input

Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nTRST   Test Reset Input

Active low reset input. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

nRSTOUT   System Reset Output

Active low reset output with 16mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST   Test Mode Input

Hardware test mode control. For D2Audio use only. Must be tied low.

CRYSTAL OSCILLATOR PINS

OSCOUT   Oscillator Output

Analog oscillator output to slave D2-91413 devices. OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin.

XTALI   Crystal Oscillator Input

Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-91413 systems, the OSCOUT from the master D2-91413 would drive the XTALI pin.

XTALO   Crystal Oscillator Output

Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.

GPIO PINS

GPIO[3:0]   General Purpose I/O

Bidirectional GPIO ports with 16mA driver. Resets to input ports.

XGPIO[3:0]   Extra General Purpose I/O

Bidirectional GPIO ports with 16mA driver. Resets to input ports.

TIMER (TIO) PINS

TIO[1:0]   Timer

Timer I/O ports with 16mA driver. May be configured as GPIO.

PWM PROTECTION PINS

PROTA   PWM Protection A Input

PWM protection A input with 4mA driver and hysteresis input. May be configured as GPIO.

PROTB[3:0]   PWM Protection B Inputs

PWM protection B inputs with 4mA drivers and hysteresis inputs. May be configured as GPIO.

PROTC[2:0]   PWM Protection C Inputs

PWM protection C inputs with 4mA drivers and hysteresis inputs. May be configured as GPIO.

AUDIO INTERFACE CHANNEL (AIC)

FMCLK0   AIC Channel 0 Master Clock

Analog Interface Channel Master Clock 0, with 16mA driver and hysteresis receiver.

FDAT0[2:0]   AIC Channel 0 Data

Analog Interface Channel Data 0 inputs.

FMCLK1   AIC Channel 1 Master Clock

Analog Interface Control Master Clock 1, with 16mA driver and hysteresis receiver.

FDAT1[2:0]   AIC Channel 1 Data

Analog Interface Channel Data 0 inputs.

SERIAL AUDIO INTERFACE PINS

SCK0   Serial Clock 0

Serial Audio Interface 0 serial clock port with 8mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SCK1   Serial Clock 1

Serial Audio Interface 1 serial clock port with 8mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC0[2:0]   Serial Control 0

Serial Audio Interface 0 serial control ports with 8mA driver. Resets to input port. May be configured as GPIO. SC00 input has hysteresis.

SC1[2:0]   Serial Control 1

Serial Audio Interface 1 serial control ports with 8mA driver. Resets to input port. May be configured as GPIO. SC10 input has hysteresis.

SRD0   Serial Receive Data 0

Serial Audio Interface 0 serial receive data ports with 4mA driver. Resets to input port. May be configured as GPIO.

SRD1   Serial Receive Data 1

Serial Audio Interface 1 serial receive data ports with 4mA driver. Resets to input port. May be configured as GPIO.

STD0   Serial Transmit Data 0

Serial Audio Interface 0 serial transmit data ports with 8mA driver. Resets to input port. May be configured as GPIO.

STD1   Serial Transmit Data 1

Serial Audio Interface 1 serial transmit data ports with 8mA driver. Resets to input port. May be configured as GPIO.

CONTROL PINS

CTRL0   Power Supply Pump High

High side power supply pump output with 16mA driver. May be used as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

CTRL1   Power Supply Pump Low

Low side power supply pump output with 16mA driver. May be used as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

CTRL2   Power Supply Sync

Switching power supply synchronization signal with 16mA driver. May be used as GPIO. Resets to input port.

CTRL3   PWM Synchronization

PWM synchronization port with 16mA drive. Used in multi-D2-91413 configurations to synchronize the PWM

controllers. The master D2-91413 will drive synchronization data to the slave D2-91413(s), thus the pin will be an output on the master D2-91413 and an input on the slave D2-91413(s). Pin floats on reset.

CTRL4   Power Supply Temperature Protection

Power supply timer protection input. May be used as GPIO with 4mA driver. Resets to input port.

CTRL5   Power Supply Current Protection

Power supply timer protection input. May be used as GPIO with 4mA driver. Resets to input port.

SYS[4:0]   System Pins

Reserved for factory test. Tie high with 10kΩ resistor.

BOOT MODE SELECT PINS

BMS[3:0]   Boot Mode Select Inputs

External boot mode select inputs. On nRESET deassertion, these pins specify the boot mode selection.

POWER PINS

PLLAVDD/PLLAGND   PLL Analog Power and Ground

PLL analog supply/return. This 1.8V supply is used for the jitter-critical sections of the PLL.

PLLDVDD/PLLDGND   PLL Digital Power and Ground

 PLL digital supply/return. This 1.8V supply is used for the "dirty" sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD   Oscillator Power

Oscillator supply. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND   Core Power and Ground

Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 9 core supply pad pairs internally connected around the pad ring.

PWMVDD/PWMGND   PWM Driver Power and Ground

PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

RVDD/RGND   Pad Ring Power and Ground

Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 4 ring supply pairs internally connected around the pad ring.
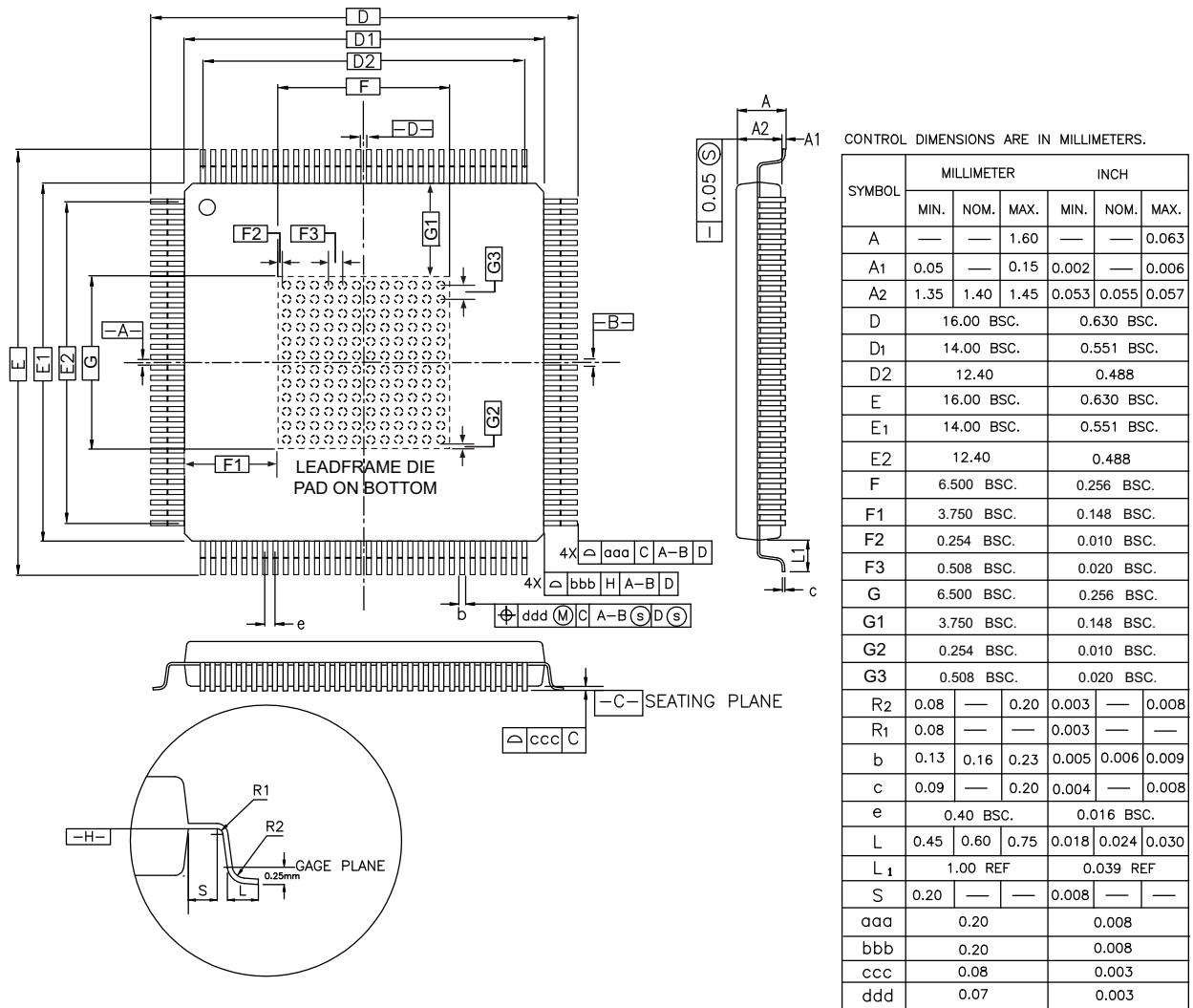
Package Physical Dimensions

FIGURE 8. D2-91413 PACKAGE DIMENSIONS

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.40			0.488		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.40			0.488		
F	6.500 BSC.			0.256 BSC.		
F1	3.750 BSC.			0.148 BSC.		
F2	0.254 BSC.			0.010 BSC.		
F3	0.508 BSC.			0.020 BSC.		
G	6.500 BSC.			0.256 BSC.		
G1	3.750 BSC.			0.148 BSC.		
G2	0.254 BSC.			0.010 BSC.		
G3	0.508 BSC.			0.020 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	—	0.20	0.004	—	0.008
e	0.40 BSC.			0.016 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTE: The D2-91413 EP-LQFP 128-pin package contains thermal vias that improve heat dissipation and thermal performance. To take advantage of this important feature, see the D2Audio Application Note D2-AN-12-1.0.1.

D2-91413 Digital Feedback And Power Supply Correction

Special Data Input Formats

D2-91413 supports -8 to +8 undecimated data format common to many commercially available ADCs. The protocol and timing relationships are shown in Figure 9:
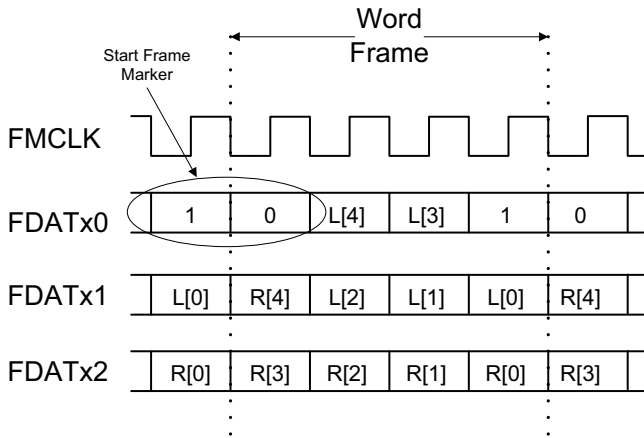

FIGURE 9. SPECIAL DATA INPUT TIMING

To support digital feedback and/or power supply correction, the D2-91413 must interface to an ADC that generates raw modulator outputs. ADCs can generate this output by tieing the MODE0 and MODE1 pins to logic VDD and toggling the HPF pin. To allow a self-start, it is recommended to place the ADC in master mode by tieing the M/S pin to logic VDD and connecting the LRCK pin to the HPF pin.

The special modulator mode does not use I^{2}S to output the digital audio signal. Instead, the modulator data are encoded on the LRCLK, SCLK, and SDOUT pins. Follow the pin mapping in the table below to connect an ADC to the D2-91413:

TABLE 9. ADC TO D2-91413 PIN MAPPING

ADC OUTPUT SIGNALS	D2-91413 POWER SUPPLY CORRECTION SIGNALS	D2-91413 DIGITAL FEEDBACK SIGNALS
LRCLK	PDAT0	FDAT00 FDAT10
SCLK	PDAT1	FDAT01 FDAT11
SDOUT	PDAT2	FDAT02 FDAT12

D2-91413 Reset and Boot Modes

Reset

D2-91413 has a two reset inputs - the nRESET and nTRST input pins. The nRESET input pin is effectively a power-on system reset. All internal state logic, except internal test hardware, is initialized by nRESET. While reset is active the system is held in the reset condition. The reset condition is

defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled. The nTRST input resets internal factory test hardware only.

To assure proper system initialization, the nTRST input pin must be driven low along with nRESET.

TABLE 10. POWER ON RESET TIMING DETAILS

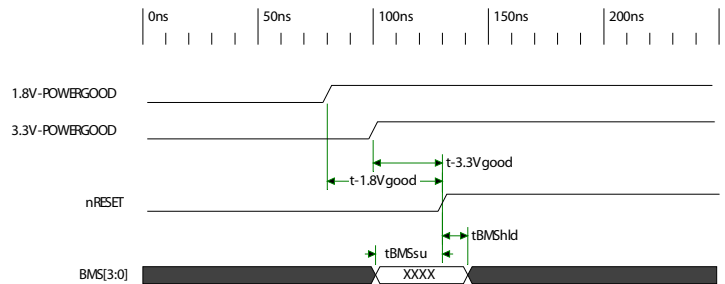| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t-1.8Vgood	Valid 1.8V power before nRESET release		10		ns
t-3.3Vgood	Valid 3.3V power before nRESET release		10		ns
tBMSsu	Boot Mode Select (BMS[3:0]) setup		1		ns
tBMShld	Boot Mode Select (BMS[3:0]) hold		0		ns

FIGURE 10. POWER ON RESET TIMING

Boot Modes

The boot mode is determined by the BMS[3:0] pin inputs. The BMS[3:0] pin state is latched on the deassertion of system reset. It is expected that the application board will have pull-ups in the BMS[3:0] pins, so that the desired boot mode is selected by default. The following table defines the boot modes.

TABLE 11. BOOT MODES

MODE	BMS[3:0]	M/S	INTERFACE SPEED	DESCRIPTION
0	0000			RESERVED
1	0001	M	400kb/s	ROM on 2-wire 0 port
2	0010	M	TBD	SPI ROM on SPI port
3	0011	S	per Master	SPI slave
7	0111	S	384Kb/s	Fast Asynchronous slave boot (ex: D2-91413 to D2-91413)
8	1000			RESERVED
9	1001			RESERVED
A	1010			RESERVED
B	1011			RESERVED

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TABLE 11. BOOT MODES (Continued)

MODE	BMS[3:0]	M/S	INTERFACE SPEED	DESCRIPTION
C	1100	S	per Master	2-wire port 1 slave boot from micro, address = 1000101x
D	1101			RESERVED
E	1110			RESERVED
F	1111			RESERVED

The Interface Speed specification is the speed at which the interface is configured to operate by the boot code. For the selection where the interface speed is "per Master", the interface must operate within the requirements of the selected interface specification. For example, the EEPROM boot speed with 2-wire interface is 400KHz.

TABLE 12. EXTERNAL HOST BOOT TIMING DETAILS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tBMSsu	Boot Mode Select (BMS[3:0]) setup	10			ns
tBMShld	Boot Mode Select (BMS[3:0]) hold	0			ns
tEXTbootRDY	2-Wire external source ready to boot	2400000			ns
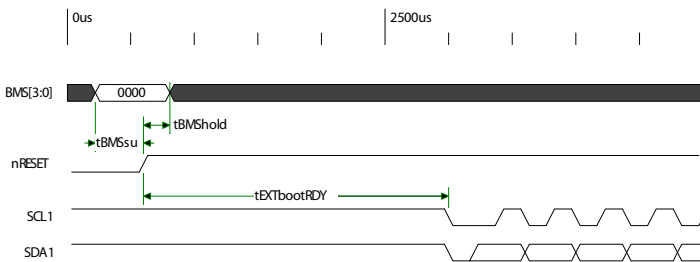
FIGURE 11. EXTERNAL HOST BOOT TIMING

TABLE 13. 2-WIRE EEPROM BOOT TIMING DETAILS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tEEboot	2-Wire EE boot delay		2650000		ns
tBMSsu	Boot Mode Select (BMS[3:0]) setup		10		ns
tBMShld	Boot Mode Select (BMS[3:0]) hold		0		ns

FIGURE 12. 2-WIRE EEPROM BOOT TIMING

IC Part Ordering

TABLE 14. ORDERING PART NUMBERS

PART NUMBER	DESCRIPTION
D2-91413-LR	Advanced PWM Controller with Integrated Digital Audio Engine, 4 channels, 128-pin package, LQFP, RoHS Compliant (Pb-Free)

Document Revision History

10/8/08 REVISION FN6791.0	
Converted to Intersil format. Removed all references to D2-91433. Assigned file number FN6784. Rev 0 - first release with this file number.	
2/26/09 REVISION FN6791.1	
Logo updates; updated trademark data; removed old internal document revision history; corrected fn67xx document number reference.	

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