A scalable approach to Class-D design challenges

by Jun Honda, Senior Staff Engineer, Class D Audio, International Rectifier Corp.

Designers of high-performance audio equipment from home theatre to active speakers are finding Class-D topology an attractive option for its space-saving benefits. Unfortunately, those designers are not familiar with the new PWM-based switching amplifier concept used in Class D because their experience is rooted in the linear-based topology of Class-AB amplifier design.

The challenges are related to the switching operation of the power transistor, which is either switched hard on or fully off. A finely tuned and well-protected PWM switching stage will perform reliably, but a design that embodies small errors or non-ideal aspects can easily result in catastrophic failure of the prototype. After the amplifier has self-destructed, the reasons for its failure can be difficult to detect. Hence correcting the error potentially adds a great deal of time and cost to the project.

To accelerate the design of robust Class-D amplifiers, four major building blocks – error amplifier, PWM comparator, gate-driver stage, and overload-protection functions – must be integrated into a single-chip solution (**Figure 1**). By combining these functions, the IRS2092 Class-D amplifier from International Rectifier can be quickly optimized to enhance performance and flexibility in the end product.

ERROR AMPLIFIER WITH NOISE ISOLATION

The major figures of merit for an audio amplifier are noise and total harmonic distortion (THD). In a Class-D amplifier, these are due to imperfections such as finite switching time, over/under-shoots, and power supply fluctuations. Their mitigation is largely determined by the error amplifier performance, which compares the output audio signal with the input audio signal to correct these imperfections in the output stage.

The noisy environment of a Class-D amplifier calls for characteristics unlike those required in a Class-A or Class-A/B design, and makes finding a suitable op amp a complex and time-consuming process. The IRS2092 integrates an optimized operational amplifier with high

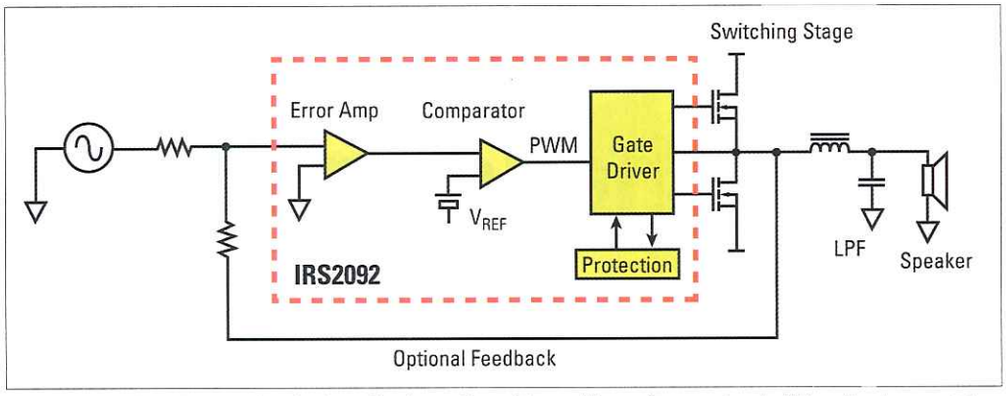

Figure 1. To accelerate the design of robust Class-D amplifiers, four major building blocks must be integrated into a single-chip solution.

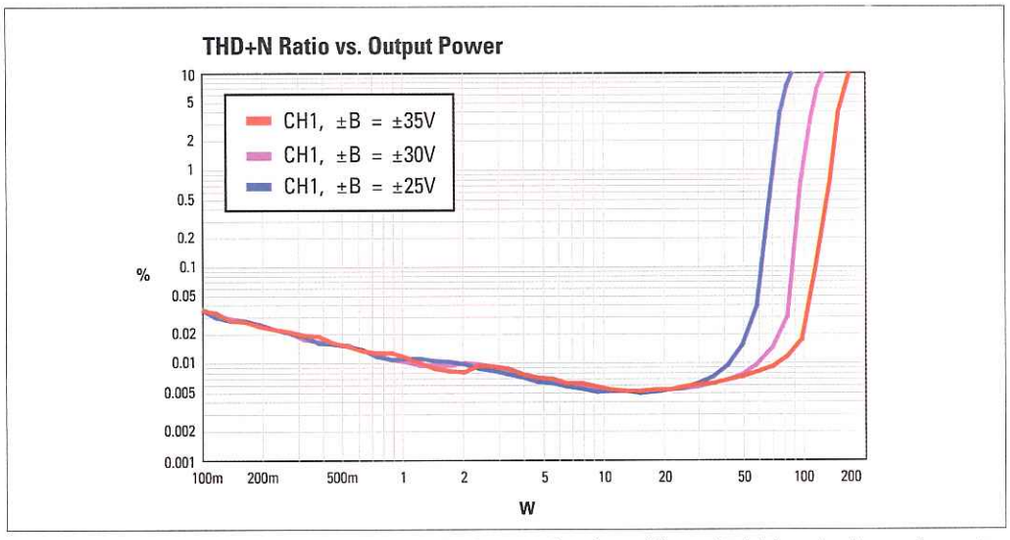

Figure 2. The IRS2092 integrates an optimized operational amplifier with high noise immunity and 5MHz bandwidth, resulting in 0.005 percent THD.

noise immunity and 5MHz bandwidth, resulting in 0.005 percent THD in the design example shown in **Figure 2**.

The Class-D topology requires the front- and back-ends to be physically close to one another. In a discrete solution, the designer must determine how to isolate the noise-sensitive input analog part from the harmful switching noise of the loud output stage.

In a monolithic solution, the toughest challenge involves achieving adequate electrical isolation between the two circuits. The IRS2092 uses a proprietary junction isolation method to guarantee noise isolation.

PWM COMPARATOR AND LEVEL SHIFTING

Once the error amplifier processes the input audio signal such that the output has the proportional shape of the input signal, the comparator converts this analog signal into a pulse-width modulated (PWM) signal. The PWM comparator transforms the analog signal to PWM with a short propagation delay, thereby allowing greater flexibility to optimize the feedback loop design.

The next challenge is to transfer the PWM signal from the quiet error-amplifier territory into the noisy switching stage. A high-voltage level shifter transfers the digital signal to a different floating potential, passing on the PWM signal accurately regardless of any voltage difference in each side, just like an ideal differential amplifier.

GATE DRIVE AND MOSFET SWITCHING STAGE

The gate-drive stage receives the PWM signal from the comparator – which is referenced to the ground potential – and level-shifts down to the gate-drive signals referenced to each source of the high-side and low-side MOSFETs. At the gate-drive stage, deadtime is inserted in between each ON state to prevent simultaneous ON states in the high- and low-side MOSFETs.

Precise gate control is the key to attaining good audio performance. The gate driver must feature low pulse-width distortion, with close matching between high- and low-side gate driver stages. Both of these attributes are critical to allow deadtime to be minimized in order to promote linearity in the amplifier's performance.

Deadtime insertion is regarded as the most critical part of the switching stage design in a Class-D amplifier. By accommodating the limited switching transition time of the MOSFET, deadtime prevents shoot-through and thereby ensures safe operation. However, it also produces nonlinearity leading to unwanted distortion. Designers are often forced to trade-off THD performance against safety margin. The built-in deadtime allows the designer to choose the deadtime duration according to the MOSFET selected. In contrast to an external deadtime design, integrated deadtime insertion with guaranteed duration saves the designers from having to estimate the worst-case scenario.

OVERLOAD PROTECTION

Since power dissipation in the MOSFET is proportional to the square of the load current, protection circuitry usually monitors the load current to prevent MOSFET failure in the event of an overload condition. An external shunt resistor is commonly used for load current detection, but aspects such as resistor selection and noise filtering are critical. This can add time, cost, and physical size to the overall solution.

The protection circuit is also required to support the redress of additional switching noise generated due to stray inductance in the critical current loop path in the power stage.

In the integrated building block IC, built-in overload protection is determined by the on-resistance of the MOSFET. Integrated circuitry monitors the output current and shuts down the PWM if a predetermined threshold is exceeded. Additionally, the large positive temperature coefficient of the MOSFET on-resistance reduces the over-current threshold with the junction temperature, thereby enhancing the safety of the amplifier.

By integrating these four essential functions, the plug-in Class-D amplifier solution can implement the critically important protected PWM switching stage. IRS2092's high level of integration solves many design challenges, but there are also flexible features allowing engineers to customize functionality to suit specific design needs.

Scaling the amplifier to different output power levels or a different number of channels is also achieved easily by selecting the appropriate external MOSFET pair and adjusting the deadtime and the overload protection threshold accordingly. The use of external MOSFETs also allows engineers to optimize EMI and efficiency to suit application requirements. Finally, as ready scalability also allows sharing of a common base design among several products, it delivers ongoing cost and time-to-market savings as end-products evolve. ■