A SWITCH MODE TRANSISTOR POWER AMPLIFIER FOR SONAR TRANSDUCERS

JOHN B. ORZALLI

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ABSTRACT

The operation of power transistors in a switch mode circuit is considered for application as a power amplifier, at 3.5 KCS, to drive sonar transducers. A method of reducing the undesired effects of resonant loading is investigated, and a method of obtaining reduced power output through pulse width modulation is considered. The effects of transistor rise, storage, and fall time is evaluated. Transistor and circuit characteristics are reviewed as a basic for design.

The design and testing of an experimental, two transistor, switch mode amplifier which delivers 166 watts of fundamental power is described. The feasibility of switch mode application is evaluated for amplifiers capable of power output in excess of one kilowatt.

The work for this thesis was done at Raytheon Company, Airborne Sonar Section, Waltham, Massachusetts, during the period 4 January 1960 through 10 March 1960, and at the U. S. Naval Postgraduate School from 15 March through 5 April 1960.

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TABLE OF SYMBOLS AND ABBREVIATIONS

α (α_n)	Direct current forward transfer ratio, common base configuration. α_i same with functions of collector and emitter interchanged.
α_ε	High frequency current amplification factor, common emitter
α_o	Direct current forward current transfer ratio, common base, low collector voltage
C	Capacitance
db	decibels
DC	Direct current
h_{FE}	DC current amplification factor, common emitter
Ibl	Initial base current
Ib2	Base current flowing just prior to switching
Ib3	Projected base current when switching to the off state.
Ic	Collector current
Icbo	Collector cut off current
KCS	Kilocycles per second
L	Inductance
M	Multiplication factor
ma	milliampere
mh	millihenry
ms	millisecond
PWM	Pulse width modulation
R	Resistance
Rie	DC base input impedance, common emitter configuration
Re	Resistance, emitter to ground
tf	fall time
tj	junction temperature

to	ambient temperature
tr	rise time
ts	storage time
μf	micro farad
μsec	micro second
ω_i	inverted angular cut off frequency with the function of the collector and emitter interchanged
$\omega_{\alpha E}$	angular cutoff frequency, common emitter
ω_{α}	angular cutoff frequency, common base

CHAPTER I

INTRODUCTION

A. Objectives

The application of solid state devices in sonar equipment has advanced rapidly in the past three years. The advantage of transistors with regards to physical size of the units, and their associated circuitry, over the same characteristics of vacuum tube application, makes transistors or other solid state devices, preferable in circuits within their capabilities. Sonar equipment in particular, offers a fertile field of solid state application.

The development of airborne sonar, with its inherent light weight requirements, lends itself readily to transistorized equipment. The array transducer of surface, and subsurface sonars, appears to be ideally suited to multiple drive units, which might well increase overall power output, with a decrease in size, weight, and source power requirements, when compared with conventional tube circuits.

The trend towards lower frequency sonars also permits easier application of transistors, as the present high power transistors are somewhat frequency limited.

The particular problem considered in this paper concerns the utilization of transistors, in a power amplifier circuit, to drive a sonar transducer. In order to take full advantage of transistor capabilities, the circuit chosen for study is the "switch mode" amplifier. Pertinent transistor characteristics, circuit configurations, and design problems, are discussed to provide a logical development of the final circuit evolved.

CHAPTER II

TRANSISTOR CHARACTERISTICS

A. Power Transistors

Power transistors, as any other circuit device, have several electrical limits which determine the operation of the unit. In order to better understand the problems of constructing a power transistor amplifier, these limits will be discussed, and the relative merits of several different amplifier configurations, and modes of operation will be evaluated.

The germanium power transistor, capable of currents in excess of one ampere, came into being during 1955. The development of the germanium power transistor appears to have reached a performance peak with units such as the 2N174, rated at 15 amperes and a maximum collector voltage of 80. During 1959, high voltage, high current, silicon transistors have become available. While silicon power transistors are not readily available from commercial suppliers at this date, units such as the Westinghouse 1016D are in production and can be obtained with considerable lead time. (See Appendix V for 1016D characteristics).

B. Power Output

Power output is determined by the maximum amount of power the transistor can dissipate, providing certain voltage limitations are not exceeded. The internal dissipation limit is set by the maximum junction temperature that still permits transistor action. While the maximum junction temperature for any solid state device can be theoretically determined from the physical properties of the materials used, it is usually determined by controlled temperature experiments conducted by the transistor manufacturer. [1]

The engineer has meager means of determining the junction temperature directly, so a figure relating the junction temperature to measureable quantities is generally given by the manufacturer. This figure is called the "Thermal resistance, junction to case", or "Thermal resistance, junction to mounting base", and is given in units of temperature per unit of power dissipated. Junction temperature is therefore determined indirectly by multiplying the "thermal resistance" value given, by the internal power dissipated, and adding the result to the ambient.

Transient junction temperature response is discussed in current literature, [2] but for the applications considered herein, the thermal rise time of the junction is sufficiently short (i.e. approximately 30 ms.), so that calculations involving power dissipation will be made on a steady state basis, assuming an infinite heat sink. [3]

Referring to Appendix V, the 2N174 has a maximum thermal resistance of 0.8 degrees Centigrade per watt. Its maximum continuous junction temperature is 95 degrees Centigrade. Assuming the transistor is mounted on an infinite heat sink, and the ambient temperature at 25 degrees Centigrade, the unit should be capable of dissipating 87.5 watts. $(\frac{95 - 25}{0.8} = 87.5)$. In actual practice, the assumed ambient temperature would be closer to 55 degrees centigrade, and the method of mounting the transistor to the heat sink could contribute an additional thermal resistance of 0.2 [4] degrees centigrade per watt. For this condition the maximum dissipation for the 2N174 would be 40 watts.

Once the maximum thermal dissipation for a particular type of mounting is known, and the ambient temperature limits given, the maximum power output to the load may be determined.

C. Thermal Runaway

Thermal runaway occurs in transistors from the effects of an uncontrolled increase in leakage current caused by an elevated junction temperature. That portion of the leakage current (Icbo) flowing through the emitter will be amplified by the transistor and result in an increased collector current. This increase in collector current causes a further rise in the junction temperature which starts the cycle over again. With this action going on in the transistor, the collector current increases until limited by the external circuit, or the unit fails completely.

In treating the problem of thermal runaway, the stability factor of the circuit is considered. That portion of the Icbo flowing in the base is not amplified by the transistor, so does not contribute to thermal runaway. The stability factor is defined as the ratio of the increase in collector current to the increase in Icbo, and may vary from unity (i.e. all Icbo flows through the base) to the h_{FE} of the transistor (i.e. all Icbo flows through the emitter). Methods of computing the stability factor of a circuit are given by many of the transistor texts. [5, 6]

D. Voltage Limitations

The voltage at which a transistor breaks down is a function of both the individual transistor characteristics, and the circuit employed. In order to understand the dependency on the circuit, the three basic modes of voltage breakdown will be discussed. None of these breakdown phenomena is by itself destructive. It is the power, and resulting heat developed by the high current flow under breakdown conditions, that gives rise to a permanent degradation of the transistor characteristics.

E. Avalanche Breakdown

Avalanche breakdown is the failure of the collector to base junction, and is in no way dependent on transistor action [7] . This mechanism of breakdown is the same means by which a "zener"[1] diode reaches and maintains a constant potential with the application of a reverse current. The additional carriers that lead to the breakdown are formed by collisions between the rapidly accelerated minority carriers and the valence electrons of the germanium atoms in the crystal network.

The ratio between the actual current at any voltage, and the current that would flow if there had been no increase from electron collision is defined as the multiplication factor, M. This factor is unity at low voltage, and reaches infinity at the avalanche breakdown voltage.

F. Alpha Equals Unity Breakdown

The M, defined above, multiplies the alpha of the transistor as well as the leakage current. Therefore, the alpha of the transistor at low voltage is taken as a reference, α_o . The alpha at any other higher voltage will be $M\alpha_o$, where M is an increasing function of the voltage applied. The DC common emitter amplification factor h_{FE}, is also a function of M by the relation:

II-1 $$h_{FE} = \frac{\alpha_o M}{1-\alpha_o M}$$

At some voltage considerably less than the avalance breakdown voltage, the factor M will be such that $M\alpha_o$ is unity, ($\alpha = 1$). This results in an infinite h_{FE}, or a common emitter breakdown.

[1] The action of a "zener" diode is comparable to the Townsend effect of a gas tube, and not a true Zener effect, which is the stripping of the valence electrons. [8]

G. Punch Through Breakdown

When a negative voltage is applied to the collector of PNP transistor, the holes in the P-type collector will be attracted to that negative potential. This attraction of the carriers away from the junction creates a depletion layer in which there are no free carriers. In an alloyed junction transistor such as the 2N174, the base region has a much higher resistivity than does the collector; therefore, as voltage is increased, the expansion of the depletion layer will occur mainly in the base region. At some elevated voltage, this depletion layer will extend entirely through the base region, and come into contact with the emitter junction. When this occurs, there will be no recombination in the base region as it is free of carriers. A short circuit now exists from collector to emitter. When punch through occurs, the base signal loses all ability to control the action within the transistor. This is in contrast to the $\alpha = 1$ phenomenon, in which the base is still capable of control until avalanche breakdown is reached.

H. Frequency Dependent Parameters

The three parameters of primary importance in considering a switch mode power amplifier are rise time (tr), storage time (ts), and fall time (tf). The usual method of determining these parameters involves the use of the frequency dependent parameters to arrive at an equivalent circuit for the transistor. An analysis of this method is carried out by Golahny [9] . The equations derived are reproduced below in [T-2, 3, 4.

Fundamentally the three parameters may be described as follows:

a . tr: The time required for the collector current to reach 90% of its final value in response to a step input. For a transistor in the common emitter configuration, the equation for tr is:

II-2 $$t_r = \frac{1}{\omega_{\alpha\mathcal{E}}} \ln \left[\frac{I_{b1}}{I_{b1} - 0.9\, \frac{I_{c\,max}}{\alpha_{\mathcal{E}}}} \right]$$

Examination of equation II-2 indicates that increasing Ibl would decrease the rise time.

b. ts: The excess concentration of minority carriers at the collector-base junction during saturation causes a delay between the removal of the drive signal and collector current drop. After the drive is removed, the excess carriers will drift into the collector region, and maintain collector current flow until their concentration reaches equilibrium, and current flow goes to zero during fall time.

II-3 $$t_s = \frac{\omega_n + \omega_1}{\omega_n \omega_1 (1 - \alpha_n \alpha_1)} \ln \left[\frac{I_{b1} - I_{b2}}{\frac{I_c (1 - \alpha_n)}{\alpha_n} - I_{b2}} \right]$$

Considering the relative magnitudes of the quantities contained in the brackets of equation II-3, one solution to obtain a decrease in storage time is available by decreasing Ib2 to a value just sufficient to hold the transistor in saturation.

c. tf: The time required for the collector current to reach 10% of its initial value.

II-4 $$t_f = \frac{1}{\omega_{\alpha\mathcal{E}}} \ln \left[\frac{I_{c\,max} - \alpha_{\mathcal{E}} I_{b3}}{0.1\, I_{c\,max} - \alpha_{\mathcal{E}} I_{b3}} \right]$$

A method of decreasing the fall time would be most easily accomplished by increasing Ib3.

CHAPTER III

CRITERION FOR SELECTION OF THE SWITCH MODE AMPLIFIER

A. Power Amplifiers

Considering the fundamental power and voltage limits of transistors, only two modes of operation have been considered applicable to sonar transducer drive units. The first application involves the use of transistors in class B linear circuity, the second would employ transistors in the switch mode.

In December, 1959, both methods were investigated by the Submarine Signal Division of Raytheon Company. [10] This particular study was undertaken to determine the most desirable circuit capable of delivering one kilowatt of power to a section of a large sub-surface sonar transducer. An additional requirement in this application was the capability of reduced power output to 30db below one kilowatt in six steps.

The results of this study led to a selection of the class B linear type of driver. The main reasons given for the selection of the Class B linear drive over switch mode were as follows:

1. Reduced power output is obtained through reduced signal drive to the amplifier.
2. The resonant load presented to the power amplifier offers no particular problem to continuous class B operation.

B. Circuit Characteristics

The above listed advantages seem sufficient to choose linear operation in preference to switch mode of operation, as either of the above advantages is immediately lost in switch mode. Other considerations detract from the desirability of linear operation. Maximum internal

dissipation could be reached before the transistors deliver their full capability. In this application this point is especially pertinent as maximum dissipation occurs at reduced signal drive. Appendix I contains a detailed explanation of linear dissipation.

As the power amplifier is pulsed in sonar applications, the resonant characteristics of the load still presents problems of initial voltage or current transients, dependent on whether the load is series or parallel tuned. Unless the signal drive is controlled to insure that each pulse commences as a sine wave, i.e. current or voltage drive is zero at time zero, for each pulse, initial transients are as possible as with a switched amplifier. An alternate solution is to derate the transistor in order to keep any undesired transients from destroying the units. It is interesting to note that the manufacturer's recommendation (see Appendix V) for the 2N174 suggest the use of a 12 volt supply where high voltage transients are to be encountered, although the 2N174 is rated as an 80 volt transistor.

Switch mode operation offers some distinctive advantages over any type of sinusoidal operation. The major advantage of switch mode lies in its high efficiency.

C. Output Power

A simplified comparison between switch mode and class B linear operation will now be given to point out the major advantage of the former method. Basis for the figures obtained in the example will be found in Appendix I. Pertinent excerpts from manufacturer's engineering sheets for the 2N174 are contained in Appendix V.

In class B operation, the voltage applied to the off transistor is twice the supply voltage, so that our chosen supply voltage is 40. The load to each transistor is therefore 2.66 ohms to obtain 15 amps of collector current. The saturation resistance, the "off" state leakage current, and the signal drive power will be omitted from the calculations as their effects are negligible. The linear amplifier can deliver 300 watts of fundamental power, ($\frac{\text{Emax Imax}}{2}$ = Power out). With two transistors delivering 300 watts of useful power, 85 watts must be dissipated internally.

For the same two transistors operated in the switch mode, the power output would be (40x15) 600 watts. Of this 600 watts, 80%, or 485 watts is contained in the fundamental frequency of the square wave obtained. The internal dissipation of the transistors will be calculated on the tr and tf, plus the "on" and "off" state losses, which will be considerably lower than the 85 watts obtained in the linear amplifier. The switch mode transistors offer a 62% theoretical increase in power output, with a considerable decrease in internal dissipation.

The reader will no doubt wonder at this point why two transistors are used in push-pull switching rather than one, which if switched at maximum rating would deliver the same power, i.e. 80 volts x 15 amperes x $\frac{1}{2}$ = 600 watts. Were it not for the limitations imposed by the frequency dependent parameters and the increased size of the output transformer required to handle the resultant unbalanced direct current, single ended operation would be highly attractive.

Even neglecting the secondary internal power losses in the linear amplifier, each transistor is required to dissipate 42.5 watts of power. This would set an absolute ambient temperature maximum. Utilizing the assumptions made on page 3:

$$\text{III-1} \qquad T_{o\,max} = 95^{\circ}C - (42.5 \text{ watts} \times 1.0^{\circ}C/\text{watt})$$

$$= 52.5^{\circ}C$$

The results of equation III-1 indicates linear operations at maximum limits is not permitted if one is to meet the requirements of present military specification. [11]

CHAPTER IV

CIRCUIT PROBLEMS IN SWITCH MODE APPLICATION

A. General

It has been shown that the switch mode amplifier offers an advantage over the linear amplifier with regards to two primary considerations. On the decision to take advantage of these two factors, three major problems confront the designer. In order of importance considered by the writer, the problems are as follows:

1. Resonant loads, such as sonar transducers, prohibit square wave voltage and current, as would be obtained from a switch mode amplifier.
2. Reduced power output must be available from the circuit utilized.
3. Power transistors are low frequency devices that might require some sort of signal drive wave shaping.

B. Amplifier Load

Work done by Kirkland [12] involves the use of switch mode amplifiers in which either current or voltage waveform is kept square, while the opposite of the chosen square waveform is allowed to vary with the load. This approach immediately loses the advantage of having both square current and voltage, in that internal dissipation for the switched transistor is about the same as the sinusoidal application.

An alternate approach, and the one chosen for the work presented herein, is the use of a crossover network to provide a frequency independent load to the amplifier. In considering a crossover network for this application, the simple L-section, constant resistance type was chosen. [13]

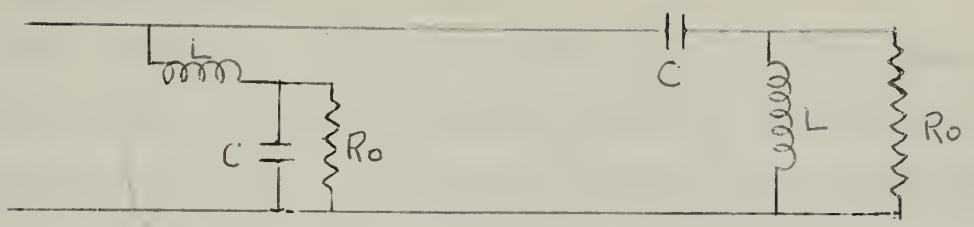
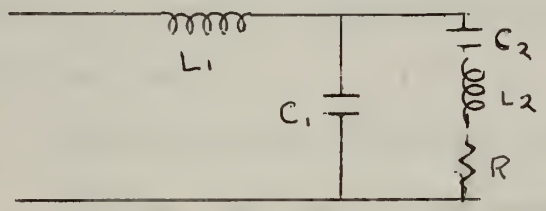


Figure 1. Constant Resistance Crossover Network

The component values for the network of Fig. 1 may be found in most design handbooks [14] , and the calculations involved present no particular problem once the Ro is specified. It is of interest to compare the low frequency side of Fig. 1 with the general schematic of a series tuned ceramic transducer element. [15]



$$\sqrt{L_1 C_1} = \sqrt{L_2 C_2}$$

Figure 2. General Schematic of a Series Tuned Ceramic Transducer

The similiarity is obvious, and while no further investigations were made, the implication is such, that it was considered appropriate to look upon the entire low frequency L-section, with termination, as a first approximation of a transducer.

By placing the high frequency arm of the network on the primary side of the coupling transformer, the possibility of including the leakage reactance of the transformer in the calculation of the series inductance in the low frequency arm, is within the realm of application.

The theoretical attenuation for this type of network is given as 12 db [16] per octave. Square wave frequency analysis yields only odd harmonics (see Appendix II), so that fundamental power losses in the high frequency termination should be less than seven per cent, if the crossover frequency is at 7 KC.

C. Reduced Power Output

The advantages to be gained from switch mode operation demand that the transistor be operated so that the ratio of AC to DC current is high. Reduced power requires a reduced power supply, or pulse width modulation. To illustrate the effects of pulse width modulation, a frequency analysis of a wave so modulated is carried out in Appendix II. Problems involved in reducing the voltage of the power supply indicate that a less "brute force" method would be a low level pre-amplifier to obtain the desired pulse width modulation.

D. Response Time Compensation

Equations II-2, II-3, and II-4 indicate the required compensation to reduce tr, ts, and tf. Reduction of these quantities appear to be desirable for two reasons:

1. The approximate trapezoidal output resulting from excessive response time leads to increased internal dissipation, with no increase in power output.
2. The current flowing in the collector of the "off" transistor during ts and tf lowers the $\alpha = 1$ voltage. In a push-pull switch circuit, this could be quite detrimental, as the collector voltage to the "off" transistor rises to twice the supply voltage.

Dependent on the type of drive source available, either of two methods may be used to obtain the desired base signal. A resistance-capacitance lead network will accomplish the job where a constant voltage source is available. (Fig. 3a) For a constant current source, a resistance-inductance network is required. (Fig. 3b)

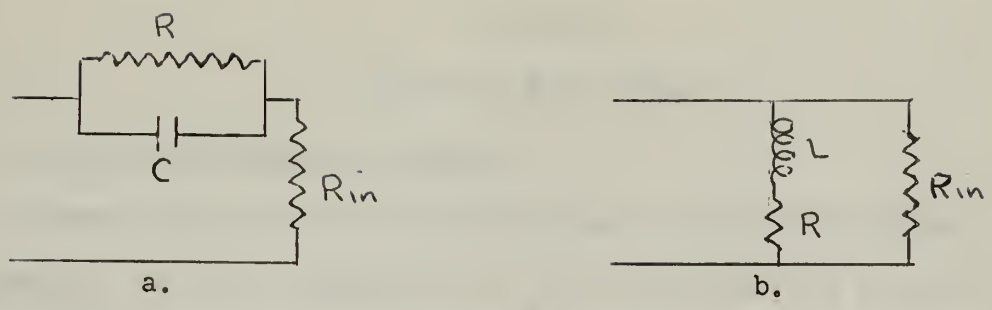


Figure 3. Lead Networks

The Rin shown in Fig. 3 represents the input impedance to the base of the transistor. When this value is known, and the desired overshoot on the Ibl is selected, the other values may be readily calculated.

By purposely raising the low frequency response of the coupling transformer, sufficient "droop" on the output waveform could be obtained to give the desired drive characteristics.

CHAPTER V

THE SWITCH MODE AMPLIFIER

A. Pulse Width Modulation Circuit

Several methods of pulse width modulation were investigated. Assuming a low level sinusoidal drive is available, the simplest solution appears to be an extension of the principles involved in an overdriven amplifier which is commonly used to obtain square waves. By varying the reverse bias to the base of a switching transistor, pulse width may be varied from full "square" wave to the point where there is insufficient drive to saturate the transistor. Of course there is a degradation in the rise time of the output as the pulse width is reduced. It is of interest to note that transistors are ideally suited for this application since switching transistors are readily available that will saturate with considerable less than one volt drive.

Two Fairchild 2N697 transistors were connected in a push-pull circuit, and variable bias was applied through the center tap of the input transformer to test the feasibility of the method. While 2N697's are switching transistors, (Appendix V) their use in the circuit was determined primarily on an availability basis rather than their characteristics. Fig. 4 is a schematic of the test circuit.

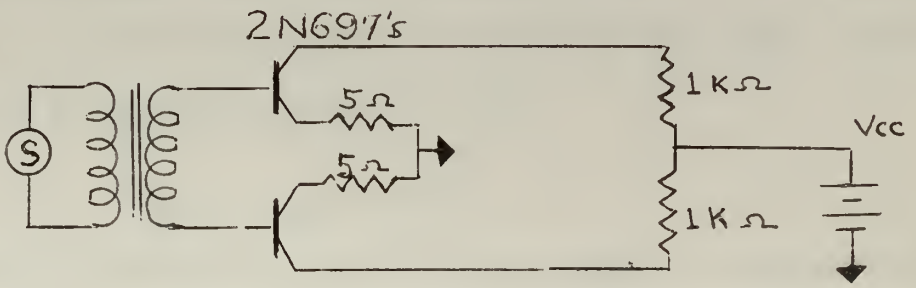


Figure 4. Preliminary Pulse Width Modulation Circuit

Photographic results of this test are contained in Appendix III, Fig. 1, 2. Fig. 1a, and 1c shows the general shape of the output obtained from collector to collector. Fig. 1b shows the details of the crossover section (porch) of the wave. Fig. 2 gives the details of the "square" wave obtained.

All tests were conducted at 3.5 KCS (period 386 μsec). Porch width was variable from 0 to 100 μsec. With no porch, the tr for one half the peak amplitude was 10 μsec, with maximum porch width, the tr was 30 μsec.

The results of those preliminary tests indicated that the desired modulation could be obtained. Subsequent tests with increased loads indicated that considerable degradation of tr could be expected as the power requirements are increased. In addition, increasing the signal drive, to reduce the tr, leads to a base to emitter breakdown on the reverse biased transistor in the push-pull circuit.

The next step in the design of the modulation circuit was to compute the power required from the drive transistors. Data available from previous work done at Raytheon [12] included a measurement of the input resistance for 13, 2N174 transistors. This data was utilized to compute a mean value of the input resistance. Taking the minimum value of h_{FE} given by the manufacturer, and using .25 ohm emitter resistors, the results provided a mean input resistance of 7.55 ohms. A standard deviation of 1.96 ohms was also obtained from this data. Equation V-1 was used in computing the above values.

V-1 $$Rin = Rie + h_{FE} R_e$$

To simplify calculations, seven ohms was chosen to represent the input impedance to the 2N174s in the proposed circuit. Working from the manufacturer's data, a 10 ampere collector current would require a 500 ma

base drive. Allowing for no other losses, the minimum drive power required should be 1.75 watts.

A two stage circuit was designed for the next test. Direct coupling was employed using PNP, 2N329A's working directly into the bases of the NPN, 2N697's. This arrangement has two distinct advantages over transformer or capacitive coupling.

1. No coupling elements are required.
2. A separate biasing circuit is not required in the second stage. Negative bias is not required, and the small positive bias required for square wave output may be obtained by biasing for a small collector current in the first stage.

At this point in the design, considerable time was expended in the choice of a coupling circuit to be used between the 2N697 drive transistors, and the bases of the 2N174 output stage. Direct coupling was desired, but was finally rejected on two significant considerations.

1. Reverse bias to the off transistor of the power output stage is not available.
2. The method of obtaining bias for the second stage could result in a quiescent collector current. This collector current, if present in the output stage, would cause both the output transistors to operate in the active region. The only load presented would be that of the DC resistance of the output transformer and the .28 ohm emitter resistors. Destruction of the output transistors under these conditions could easily occur.

Capacitive coupling was rejected on the basis of the first reason given above, and in addition, the stability factor in the output stage would be h_{FE}, as no DC path would exist from base to emitter. Transformer coupling eliminates all of the objections raised for the other two methods.

The circuit of Figure 5 was constructed, and tests conducted. The small emitter resistors used in both stages serve, not only as stabilizing elements, but eliminates input characteristic differences between the individual transistors. Changes in h_{FE} and Rin tend to give unsymetrical "square" waves from the push-pull circuit if the emitter resistors are omitted. The tests conducted utilizing the load of Fig. 5b proved highly satisfactory. Rise times of only 20 μsec were obtainable with porch widths of 200 μsec, (See Appendix III,Fig. 8, 9). On the basis of these tests a special transformer was ordered.

While awaiting the delivery of the transformer, several different transformers immediately available in the laboratory were tried in the configuration of Fig. 5b. Each trial required a separate calculation to determine the termination necessary on the secondary winding to present a 300 ohm load to the transistors. Unfortunately, none of the transformers tested during this trial and error period proved capable of passing the desired waveshape without considerable distortion. During this testing of random transformers, some of the results indicated the possibility of utilizing the transformer design, instead of a lead network, for drive wave shaping. The long lead time required for special transformers precluded this type of application from being included in the overall design.

In the circuit under test, the reader might question the use of only one termination on the secondary of the transformer. As one of the transistors in the output stage is off, the input impedance reflected by that unit is the equivalent of a reverse biased diode, and can be considered infinite with respect to the input impedance of the transistor that is on.

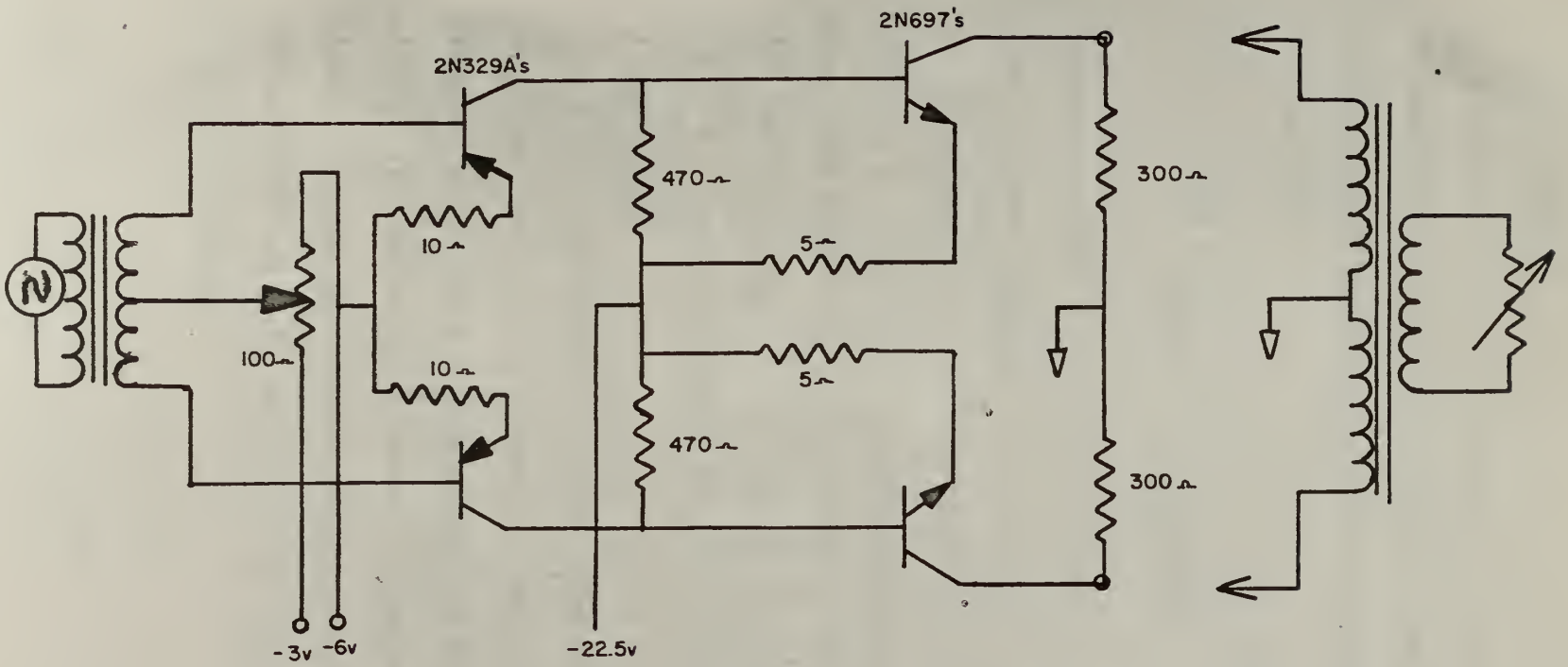


FIGURE 5 PULSE WIDTH MODULATION CIRCUIT

B. Lead Network

Utilizing the general schematic of Fig. 3b, a LaPlace transformation was used to obtain the drive current through Rin in response to a step voltage input. The results of this transformation is summarized in equation V-2.[2]

V-2 $$i(t) = \frac{1}{R + Rin} + \frac{R}{Rin(Rin + R)} e^{\frac{t(Rin+R)}{Rin\,RC}}$$

With equation V-2, one may select the desired overshoot of Ibl, and given the input impedance of the circuit to be used, compute the component values required. The time constant of the circuit used need not be critical, as long as the transient will decay in half a period of the square wave assumed. The values chosen for experimentation should yield a 50% overshoot, and a decay time (5 time constants) of 50.0 μsecs. i. e. R = 3.5 ohms, C = 4 μf, Rin set at 7 ohms for one transistor.

C. Termination

A decision to utilize a 300 ohm terminating load was based on verbal information available at Raytheon concerning the characteristics of the transducer units for the AN/BQQ-1 application. [10] Straightforward computations for the crossover network component values were made using the handbook formulas and a chosen crossover frequency of 6 KCS. Results of these computations yield values for the components of the schematic shown in Fig. 1 as follows:

Ro = 300 ohms

L = 11.3 mh

C = 0.062 uf

[2]. Saturated transistors are a nearly perfect constant voltage source. As evidenced by the inclusion of a R-L lead network in the photographs contained in Appendix V, this fact was not discovered by the writer until late in the experimental stages of the project.

If it is desired to reflect the high frequency section of the cross-over network to the primary side of the transformer, either the impedance ratio specified, or the turns ratio of the transformer may be used in accordance with equations V-3.

$$C(\text{reflected}) = (N_2/N_1)^2\, C = (Z_2/Z_1)\, C = C' \qquad \text{V-3}$$

$$L(\text{reflected}) = (N_1/N_2)^2\, L = (Z_1/Z_2)\, L = L'$$

$$Ro(\text{reflected}) = (N_1/N_2)^2\, Ro = (Z_1/Z_2)\, Ro = Ro'$$

The theoretical calculations were verified with the test circuit of Fig. 6.[3]

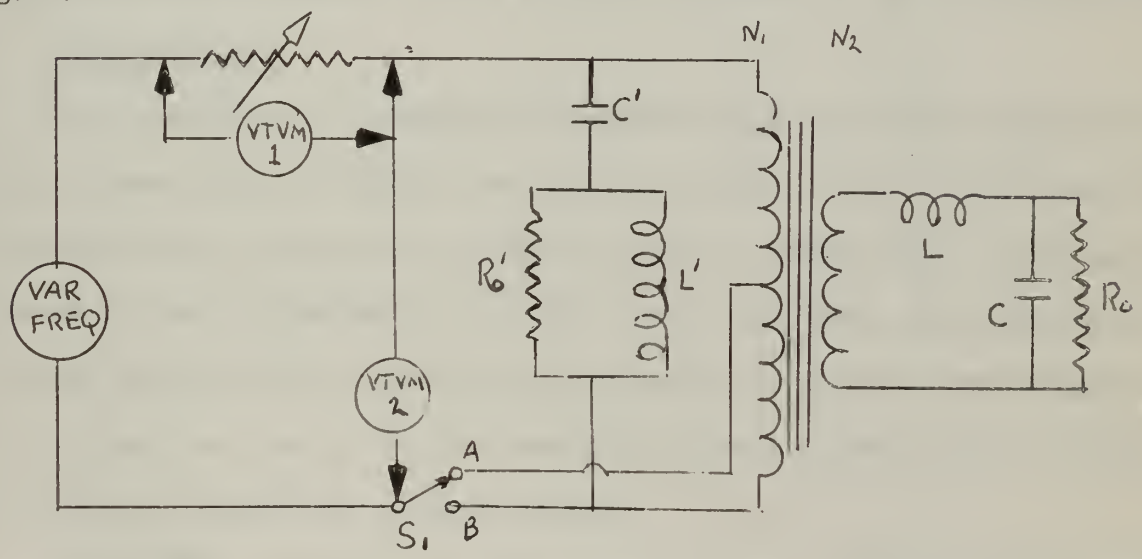


Figure 6. Input Impedance Test Circuit

Magnitude of the input impedance may be measured with the test circuit of Fig. 6 in the following manner.

1. Connect S1 to either terminal A or B.
2. Set R to a convenient multiple, say 10 times, the expected input impedance.
3. Set the oscillator output to give midscale deflection on VTVM 1 at each frequency used.

[3] Several attempts were made to measure the input impedance of the circuit with a bridge. The impedance values to be measured are less than 4.5 ohms, which gave considerable difficulty with the bridges available.

4. Set VTVM 2 on a lower scale, (1/10 that of VTVM1).

5. Compute input impedance directly from the ratio determined by the R setting and the VTVM readings.

While the above method will not give phase angle, it can be assumed that the input impedance is resistive if the magnitude of the impedance does not change over a considerable frequency range. All tests conducted with this method on the actual circuits indicated that the load was constant at all frequencies from 3.5 KCS to 20 KCS. An extension of this method of measurement was made to determine the DC primary resistance of the transformers used.

D. Circuit Tests

The first tests of the amplifier and PWM circuit were made employing resistive loads in the collector leads of the 2N174's. Fig. 7 illustrates the first test circuit used. The choice of load for these initial tests was predicated on the non-availability of an output transformer, and a desire to evaluate the PWM circuit working into the load for which it was designed. In addition, the results of this test would give a control factor to later tests with a transformer coupled output.

The results of the first test revealed no basic faults with the theory of design. Practical problems which arose from these tests were corrected by increasing the power capability of the PWM circuit by the insertion of 2N158 and 2N1050 transistors for the 2N329A and 2N697 respectively. The final results obtained from these tests are illustrated in the collector to collector waveforms obtained. (Appendix III, Fig. 3 - 7). The "rounding" of the tops of the waveforms indicated is attributed to power supply deficiencies. Later experimentation proved conclusively that transients in the power supply can cause considerable distortion in the output wave forms.

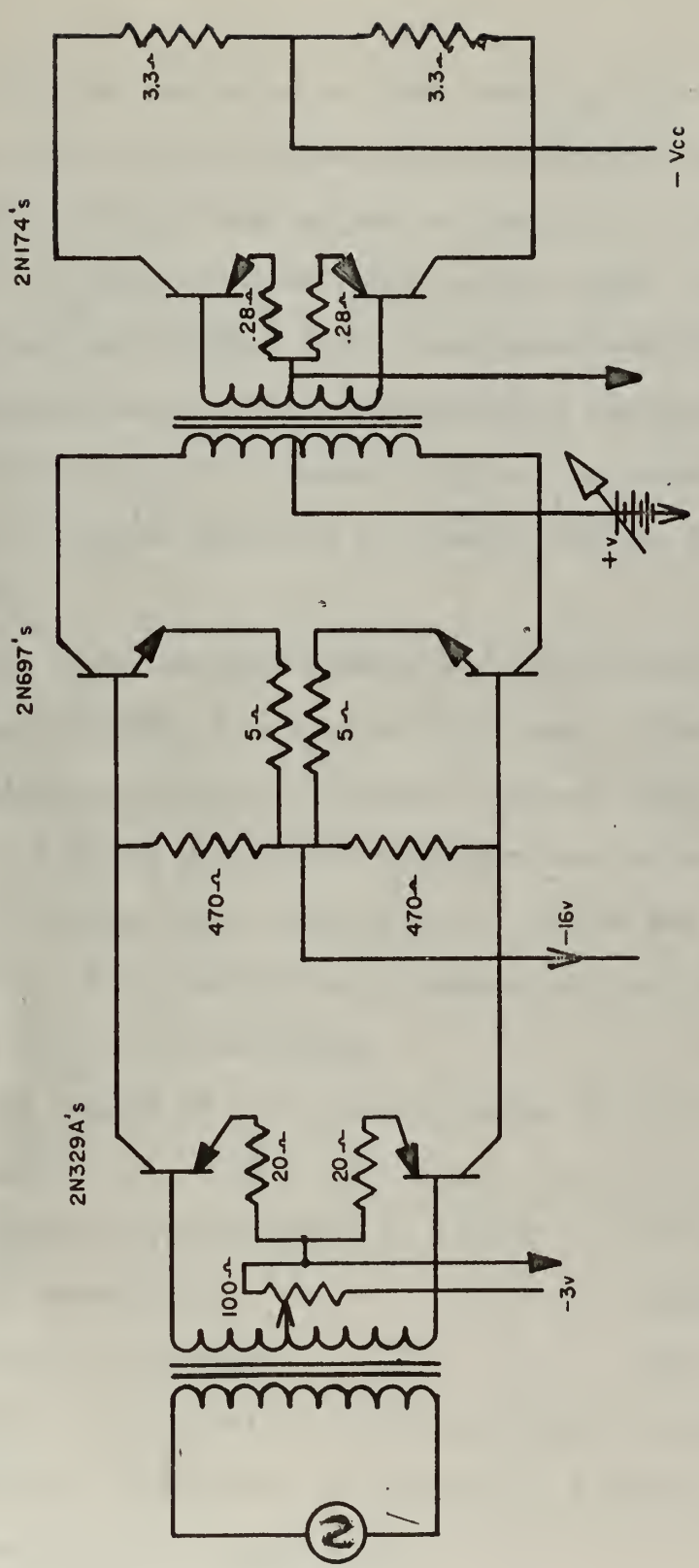


FIGURE 7 TEST CIRCUIT NO. 1

The final evaluation was made using the circuit of Fig. 8. Photographs of the breadboard, and test equipment associated with the schematic of Fig. 8 may be found in Appendix V. The values indicated in Fig. 8 are those associated with the final tests, and the reader is advised that two different input transformers, and two different output transformers were utilized in the complete evaluation. Referring to Figures 3 through 17 of Appendix III, one may observe the waveforms obtained at various points in the circuit, and see the effects of the PWM control.

The distortion introduced in Fig. 14 of Appendix III was the result of inserting 1N344 diodes in the base leads of the 2N174's in an attempt to nullify the overshoot obtained at reduced pulse widths. The slight overshoot on the collector to collector waveform of Fig. 10 is the result of a power supply transient, and not from any reactive component in the load. This overshoot was eliminated entirely in tests made subsequent to the time of the photograph.

The results of the terminating tests on the circuit are summarized as follows:

Fundamental power output at 3.5 KCS	166 watts
DC. Power input	368 watts
Overall efficiency	45%

As the efficiency for this circuit seems low when compared with the theorectical calculations of Chapter III, some basic considerations will help to justify the figure given.

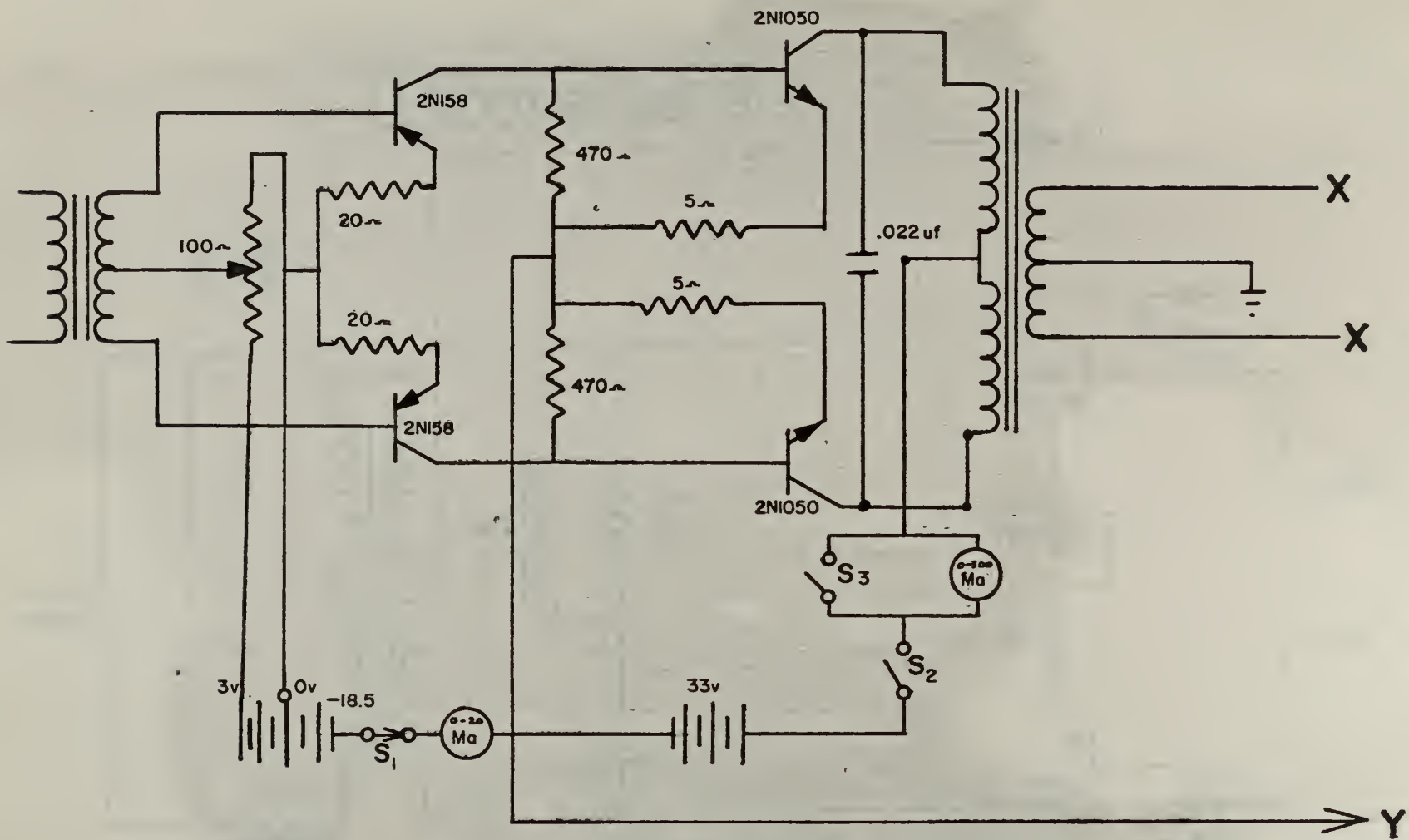


FIGURE 8 FINAL TEST CIRCUIT

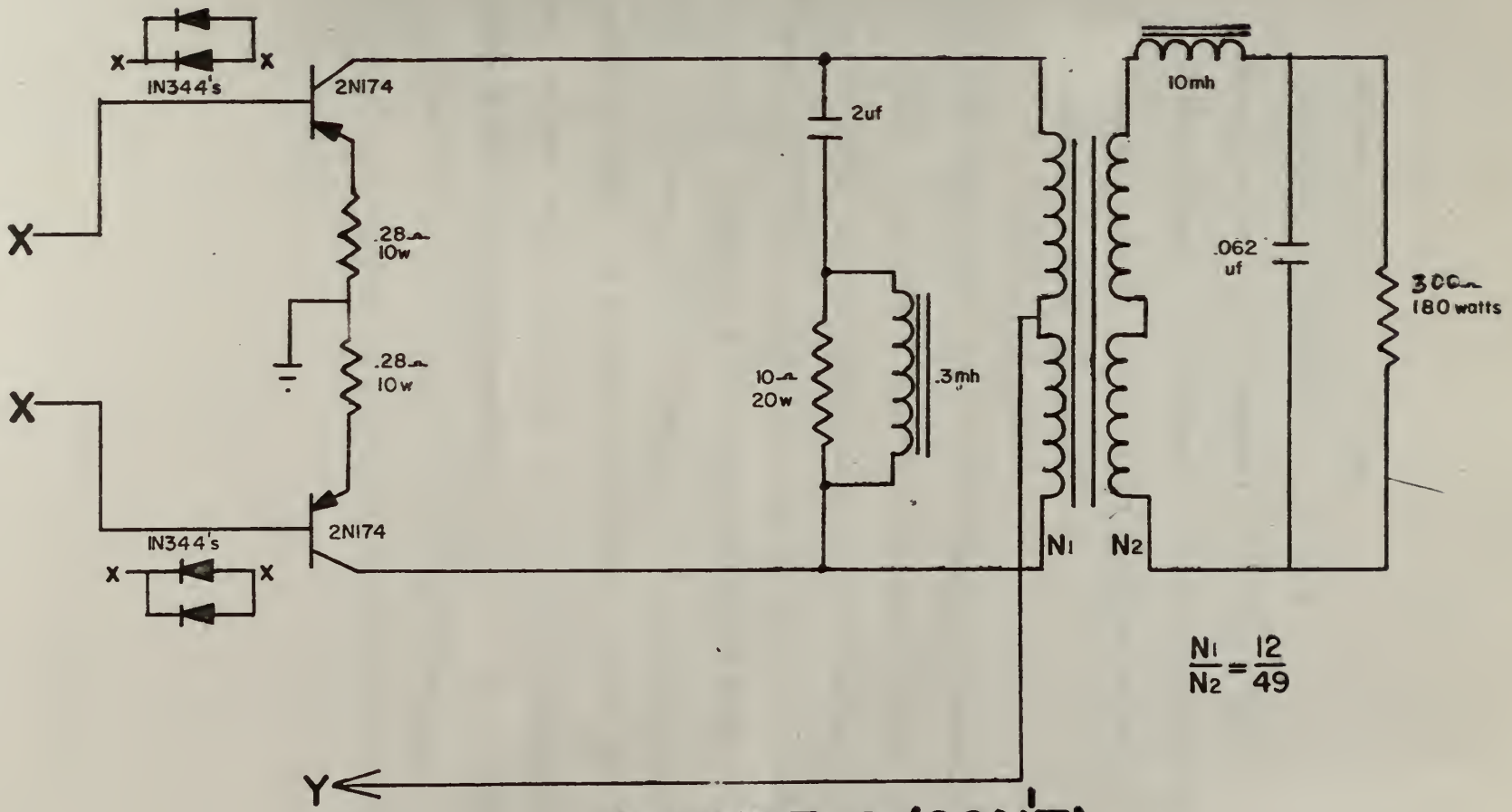


FIGURE 8 (CON'T)

Emitter resistors - 0.28 ohms	
Transformer DC resistance - 0.19 ohms	
Supply current (10.8 amperes)^2 x (0.28 + 0.19)	55 watts
Assumed power in the harmonics of the "square wave"	42 watts
Fundamental power lost in the HF section of the crossover network (measured)	27 watts
Known power losses	124 watts

The known power losses added to the fundamental power give a total of 292 watts. No attempt to apportion the balance of 76 watts between the dissipation in the transistors, and the core losses of the transformer. A DONNER #2102 wave analyzer was used to obtain the fundamental power calculated. Pulses of 3 to 5 seconds duration were used to obtain readings on the wave analyzer. Throughout the experiment a "finger test" failed to detect any noticable temperature rise in either the transistor case, or stud mount. There was no detectable difference in the output obtained with the RC lead network included in the circuit. A power reduction of 3.2 db was obtained through the use of PWM. With a well regulated power supply, no transient voltage spikes could be detected in the circuit.

CHAPTER VI

CONCLUSIONS

A. Pulse Width Modulation

The concept of PWM to obtain reduced power output is feasible. If power output is to be reduced by several db, more than two stages will be required in the control circuit. Reductions in the order of 30db do not appear to be feasible regardless of the number of stages employed, as the width of the pulse required would be less than the total of the rise and fall times of the transistors.

B. Response Time Improvement

Improvements resulting from the use of load networks could not be measured relative to the results obtained without compensating devices. The rise times observed throughout the experiment were less than those given by the manufacturer. On the basis of the experimental evidence it is concluded that the 2N174 does not require compensating networks if operated at 3.5 KCS or lower.

C. Load Termination

The use of a crossover network permits switching operation into reactive loads. All aspects of switching theory may be applied directly to the circuit with a resistive load assumed. In addition, by inserting the high frequency section of the network in the primary side of the output transformer, the undesirable effects of transformer primary leakage inductance may be eliminated. Application of 2N174 transistors in an amplifier capable of power in excess of one kilowatt does not appear feasible in this circuit configuration. The low impedance required to draw sufficient current would rapidly approach the DC resistance of the primary winding of the coupling transformer.

D. Suggestions For Further Application

The inclusion of a crossover network in present linear amplifiers would eliminate initial voltage transients and the need for timing circuitry in pulsed applications.

With units such as the Westinghouse 1016D, an amplifier capable of one kilowatt fundamental output power would require a maximum of four transistors, and quite possibly two transistors of this type would be sufficient if the power supply capability was not a determining factor. Substituting 2N1016D's directly into the circuit of Fig. 8 and raising the supply voltage to 60 volts would yield an amplifier capable of 530 watts of fundamental output.

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3. Loc. Cit., Clevite Transistor Products, pp 1.

4. Ibid., pp 2.

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8. Ibid., p. 2

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13. W. L. Everitt and G.E. Anner, Communications Engineering, McGraw-Hill Book Co., Inc., pp. 289-291, 1956.

14. F. Langford Smith, Radiotron Designer's Handbook, RCA Tube Div.,p.185,'53

15. Kinsler and Frey, Fundamentals of Accoustics, John Wiley and Sons, p. 473, 1950.

16. Loc. Cit. F. Langford-Smith, p. 184.

In addition to the preceeding specified references, the following papers were useful and pertinent.

17. H.W. Henkels, T.P. Norwalk, High Power Silicon Transistors, Westinghouse Electric Corp., Semiconductor Dept., pp. 1-10.

18. Clevite Transistor Products, Application Bulletin No. 2. Collector Breakdown Failure in Power Transistors, Waltham, Mass. (No date or Author given)

APPENDIX I

AMPLIFIER EFFICIENCY

Sinusoidal Amplifier

Normalizing the output of a sine wave amplifier the power output can be expressed:

$$Po = x\,(1-x)$$

where $x = a \sin wt$: a = excitation

$$Po = a \sin st\,(1 - a \sin wt)$$
$$= a \sin wt - a^2 \sin^2 st$$

Average power output = $\frac{a^2}{2}$

Average power input = $\frac{2}{\pi}$

Defining Efficiency as Po(avg)/Pin (avg) = $\frac{a^2}{2} \Big/ \frac{2a}{\pi} = \frac{\pi}{4}\,a$

This gives efficiency directly proportional to the excitation, a, and a maximum efficiency of $\pi/4 = 78.54\%$

Also note that dissipation is a function of excitation, and maximum dissipation does not occur at maximum excitation.

i.e.

Power Dissipated (Pd) = $a\left(\frac{2}{\pi} - \frac{a^2}{2}\right) = a\left(\frac{4 - a}{2\pi}\right)$

Solving for Pd max.

$$dPd/da = \left(\frac{4 - \pi a}{2\pi}\right) - a/2 = o \text{ when } a = \frac{2}{\pi}$$

Square Wave Amplifier

Assuming a perfect amplifier, the power dissipated is zero, while the efficiency is determined from the analysis of the wave form in terms of fundamental and harmonic power.

$Po = P_f$ and + $P_{harmonic}$.

$$e(t) = \frac{4E}{\pi} (\sin wt + 1/3 \sin 3 wt + 1/5 \sin 3 wt + \ldots)$$

Normalizing

$$\text{Power} = \frac{8}{\pi^2} (1 + 1/9 + 1/25 + \ldots\ldots)$$

$$= \frac{8}{\pi^2} (1 + K)$$

$$P_{fund} = \frac{8}{\pi^2} = .808 \quad P_{harmonics} = \frac{8K}{\pi^2} = .192$$

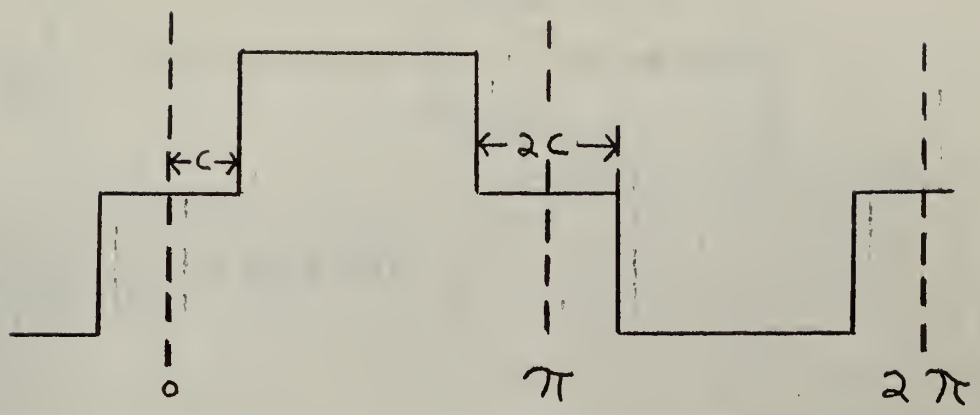
Summary

The table below summarizes the characteristics of the amplifiers considered.

Mode	a	Input	Output	Dissipation	Efficiency
Square Wave	1	1	.808	.192	80.8
Sin Wave	1	.636	.500	.136	78.5
Sin Wave	.636	.404	.202	.202	50.0

APPENDIX

SYNTHESIS OF OUTPUT WAVEFORM



DEFINE THE WAVEFORM AS FOLLOWS:

AMPLITUDE = 1

$f(t) = 0$ 0 to c

$= 1$ c to $\pi - c$

$= 0$ $\pi - c$ to $\pi + c$

$= -1$ $\pi + c$ to $2\pi - c$

$= 0$ $2\pi - c$ to 2π

Applying Fourier Series techniques

$$f(t) = \tfrac{1}{2}a_0 + \sum_{n=1}^{\infty} (a_n \cos nwt + b_n \sin nwt)$$

By a choice of axis, the odd function resulting, leads to an elimination of all a_n terms of the series.

b_n is defined:

$$b_n = \int_0^{2\pi} f(t) \sin nwt \, d(wt)$$

Substituting for the given Waveform:

$$b_n = \frac{1}{\pi}\left\{\int_{c}^{\pi - c} \sin n(wt)d(wt) - \int_{\pi + c}^{2\pi - c} \sin nwt\, d(wt)\right\}$$

$$= \frac{2}{\pi}\int_{c}^{\pi - c} \sin nwt\, d(wt)$$

$$= -\frac{2}{\pi n}\left[\cos nwt\right]_{c}^{\pi - c}$$

$$= -\frac{2}{\pi n}\left[\cos n(\pi - c) - \cos nc\right] =$$

$\frac{4}{\pi n}$ cos N c for n odd; o for n even

$\therefore$

$$f(t) = \frac{4}{\pi}\sum_{n=1}^{\infty} \frac{\cos}{n} nc \sin nwt \quad (n \text{ odd})$$

Note that the above function reduces to the familiar series of a square wave with c = 0

APPENDIX III

CIRCUIT WAVEFORMS

Appropriate comments relating each of the oscilloscope photographs are found in the corresponding position on the page facing the illustrations.

Collector to collector waveforms obtained from the test circuit shown in Figure 4, page 16 of the text.

Fig. 1

Collector to collector waveforms obtained from the test circuit shown in Fig. 4, page 16 of the text.

Fig. 2

Load waveform obtained from the test circuit shown in Fig. 5b, page 20 of the text. Transformer used is the transformer shown in Fig. 8 (Final test circuit) page 26 of the text.

Fig. 3

Collector to collector voltage waveform obtained from the test circuit shown in Fig. 7. (Test circuit No. 1) page 24 of the text.

Fig. 4

APPENDIX III
CIRCUIT WAVEFORMS

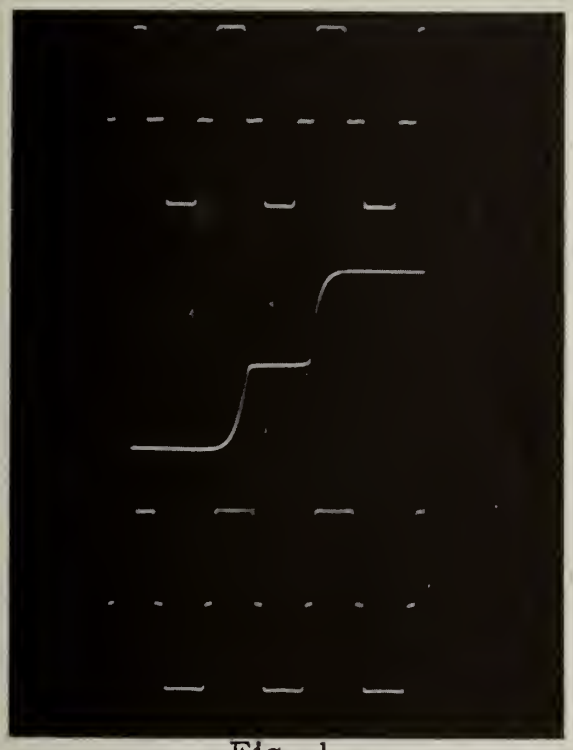


Fig. 1

3.5 kc 3.8-v peak

Fig. 2

3.5 kc 3.8-v peak

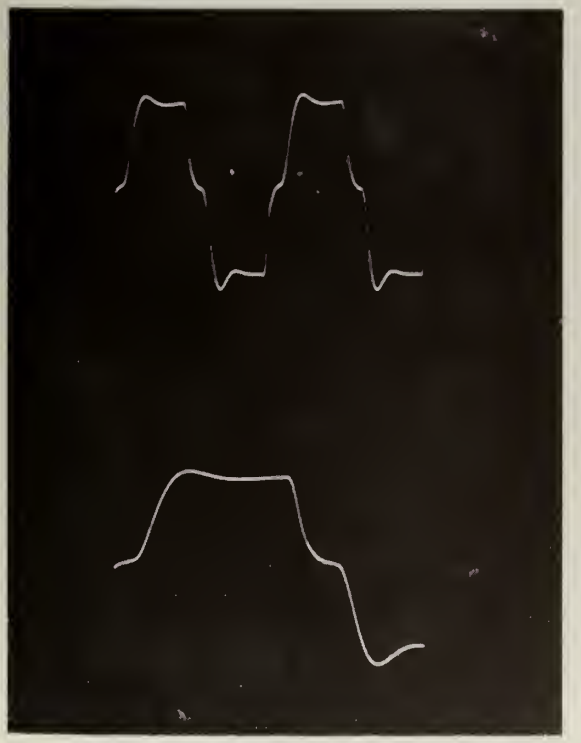


Fig. 3

(a) 50 μ sec/cm .2 volts/cm
(b) 20 μ sec/cm .2 volts/cm

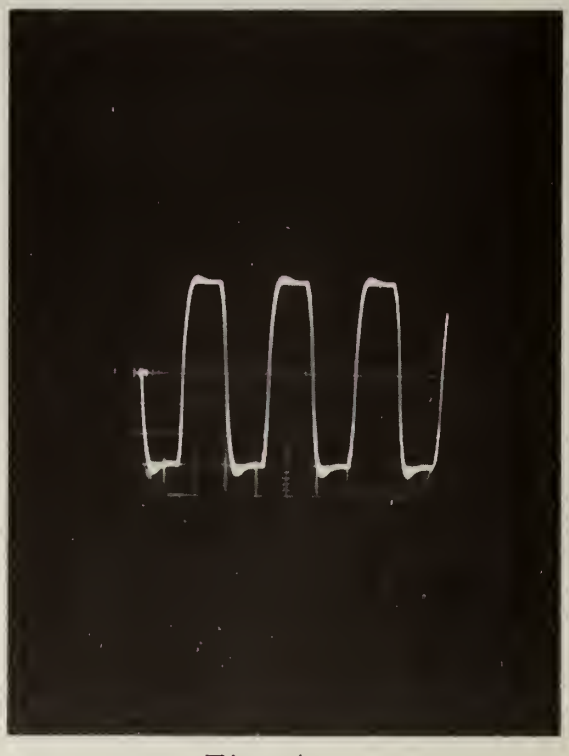


Fig. 4

100 μ sec/cm 5 volts/cm

Fig. 5, 6, and 7 were obtained from the test circuit shown in Fig. 7, Test Circuit No. 1, page 24 of the text.

Base-to-Base drive waveform for the 2N174 output transistors. Full drive.

Fig. 5

Collector to collector waveform. 2N174. Power supply at 20 volts.

Fig. 6

Collector to collector 2N174 waveform. Reduced drive. 20 volt power supply.

Fig. 7

Waveforms obtained from Fig. 5a page of 20 the text.
a. collector-to-collector of the 2N329A's.

b. collector-to-collector of the 2N697's

Fig. 8

Fig. 5

50μsec/cm 2 volts/cm

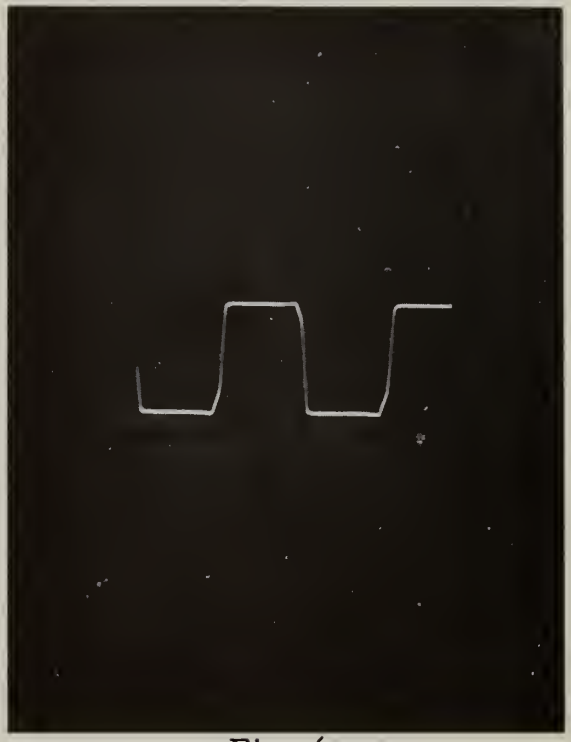


Fig. 6

50μsec/cm 10 volts/cm

Fig. 7

50μsec/cm 10 volts/cm

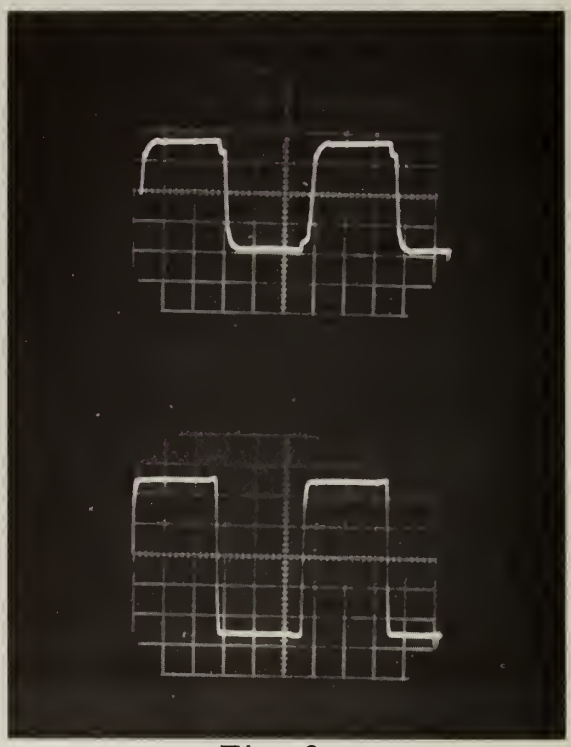


Fig. 8

(a) 50μsec/cm 1 volt/cm
(b) 50μsec/cm 10 volts/cm

Waveforms obtained from the Pulse Width Modulation circuit shown in Fig. 5a, page 20 of the text.

a. collector-to-collector of the 2N329A's.

b. collector-to-collector of the 2N697's.

Fig. 9

Waveforms obtained from the Final Test Circuit, Fig. 8, page 27 of the text.

a. collector-to-collector of the 2N174's. Overshoot obtained attributed to power supply transients.

b. "fundamental" output across the 300 ohm terminating resistor.

Fig. 10

Waveform obtained from Final test circuit. Fig. 8, page 27 of the text.

a. collector-to-collector waveform, 2N174's, reduced drive.

b. "Fundamental" output waveform across 300 phm terminating resistor, reduced drive.

Fig. 11

Waveform obtained from Final Test Circuit. Fig. 8, page 26 of the text.

a. collector-to-collector waveform. 2N158's, full drive.

b. base-to-base waveform, 2N174's, full drive.

Fig. 12

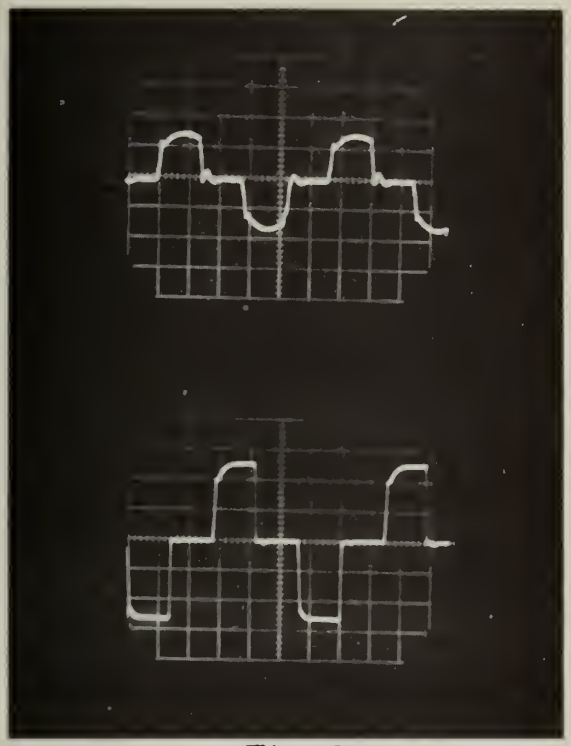


Fig. 9

(a) 50μsec/cm 1 volt/cm
(b) 50μsec/cm 10 volts/cm

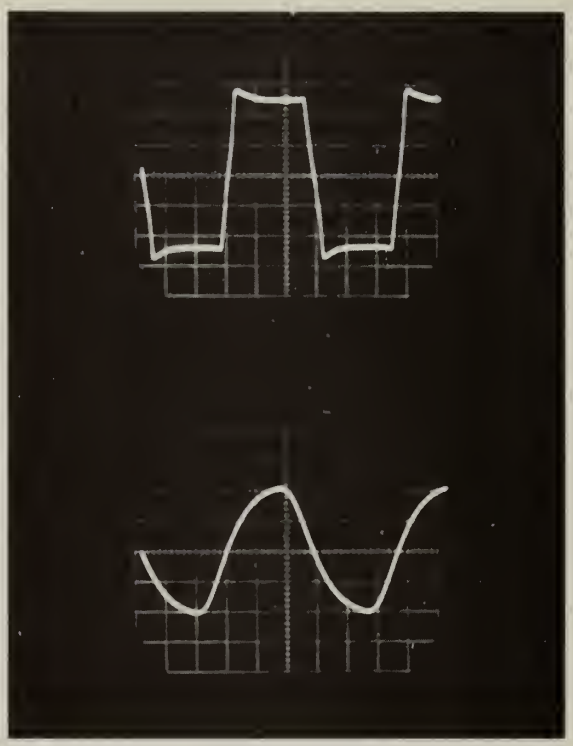


Fig. 10

(a) 50μsec/cm 20 volts/cm
(b) 50μsec/cm 100 volts/cm

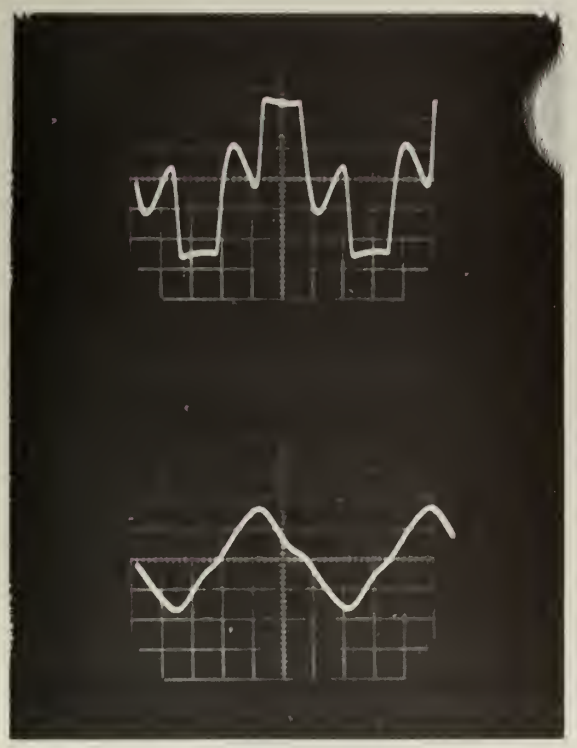


Fig. 11

(a) 50μsec/cm 20 volts/cm
(b) 50μsec/cm 100 volts/cm

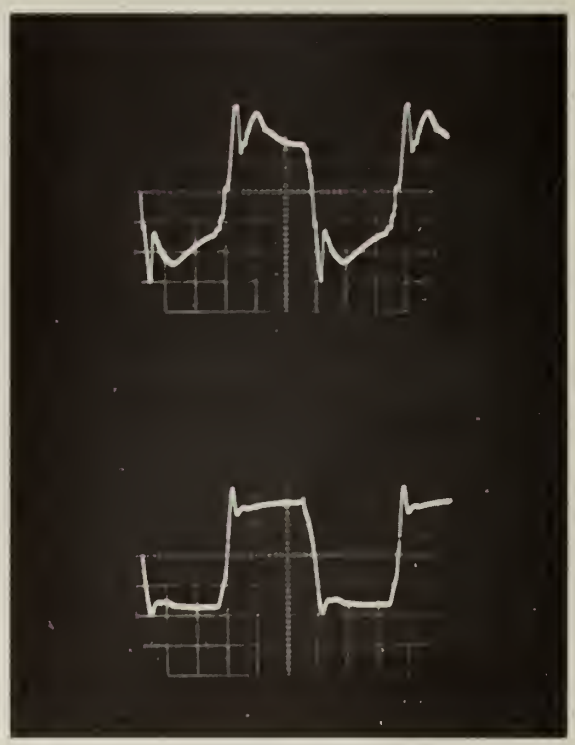


Fig. 12

(a) & (b)
50μsec/cm 2 volts/cm

All waveforms described were obtained from the test circuit of Fig. 8, page 26,27 of the text. (Final test circuit.)

a. Base-to-base, 2N174's, reduced drive.

b. Base-to-base, 2N1050's, reduced drive.

Fig. 13

Base-to-base, 2N174's with diode inserted in an attempt to minimize the overshoot obtained in Appendix III, Fig. 11.

a. full drive.

b. reduced drive.

Fig. 14

2N158 base-to-base.

a. full drive

b. reduced drive

Fig. 15

Output across the dissipating resistor contained in the high frequency side of the output cross-over network.

a. full drive

b. reduced drive.

Fig. 16

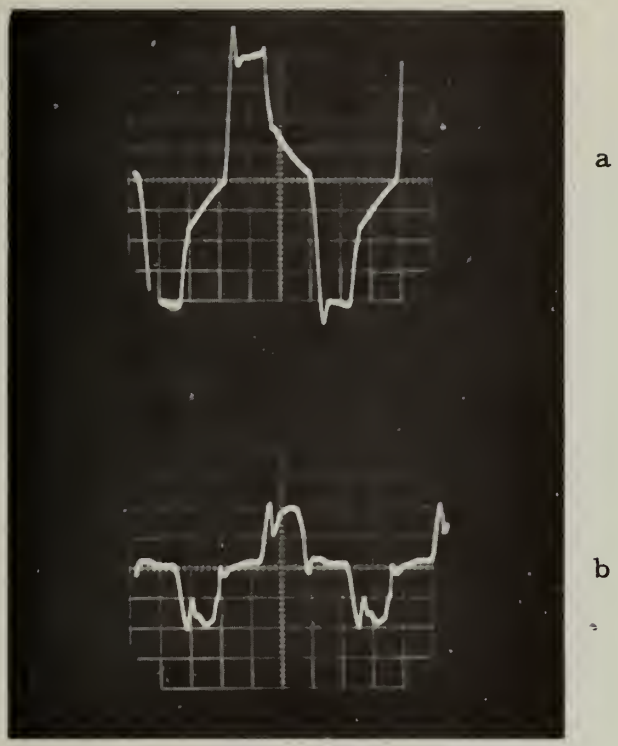


Fig. 13

(a) & (b) 50μ sec/cm 2 volts/cm

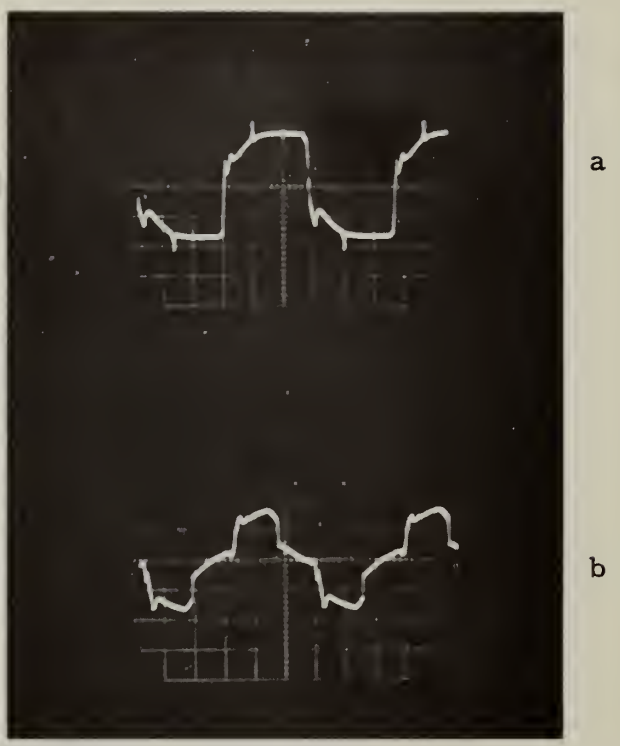


Fig. 14

(a) & (b) 50μsec/cm 2 volts/cm

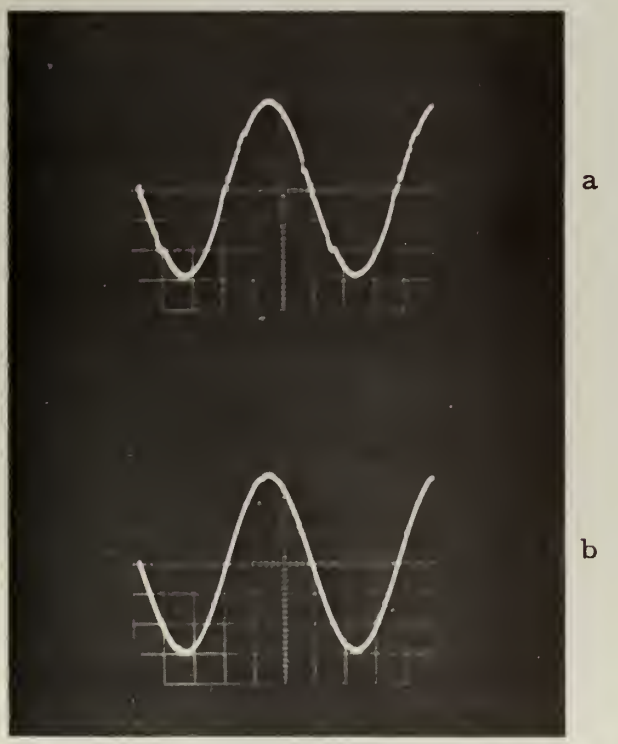


Fig. 15

(a) & (b) 50μ sec/cm 2 volts/cm

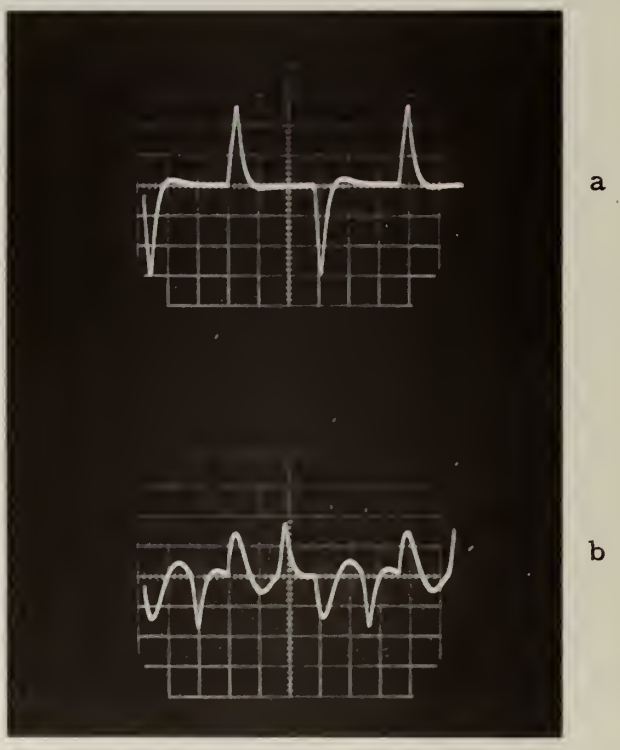


Fig. 16

(a) & (b) 50μsec/cm 20 volts/cm

Collector-to-collector voltage waveform of the 2N174 transistors shown in Fig. 8, page 27 of the text. This photograph shows the detail of the "crossover", and rise time.

Fig. 17

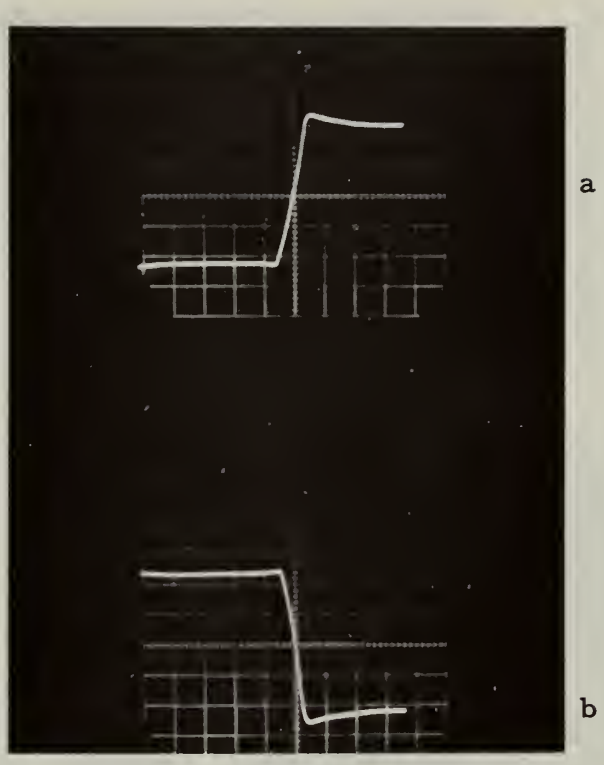


Fig. 17

20 μ sec/cm 20 volts/cm

APPENDIX IV

TEST EQUIPMENT AND CIRCUIT

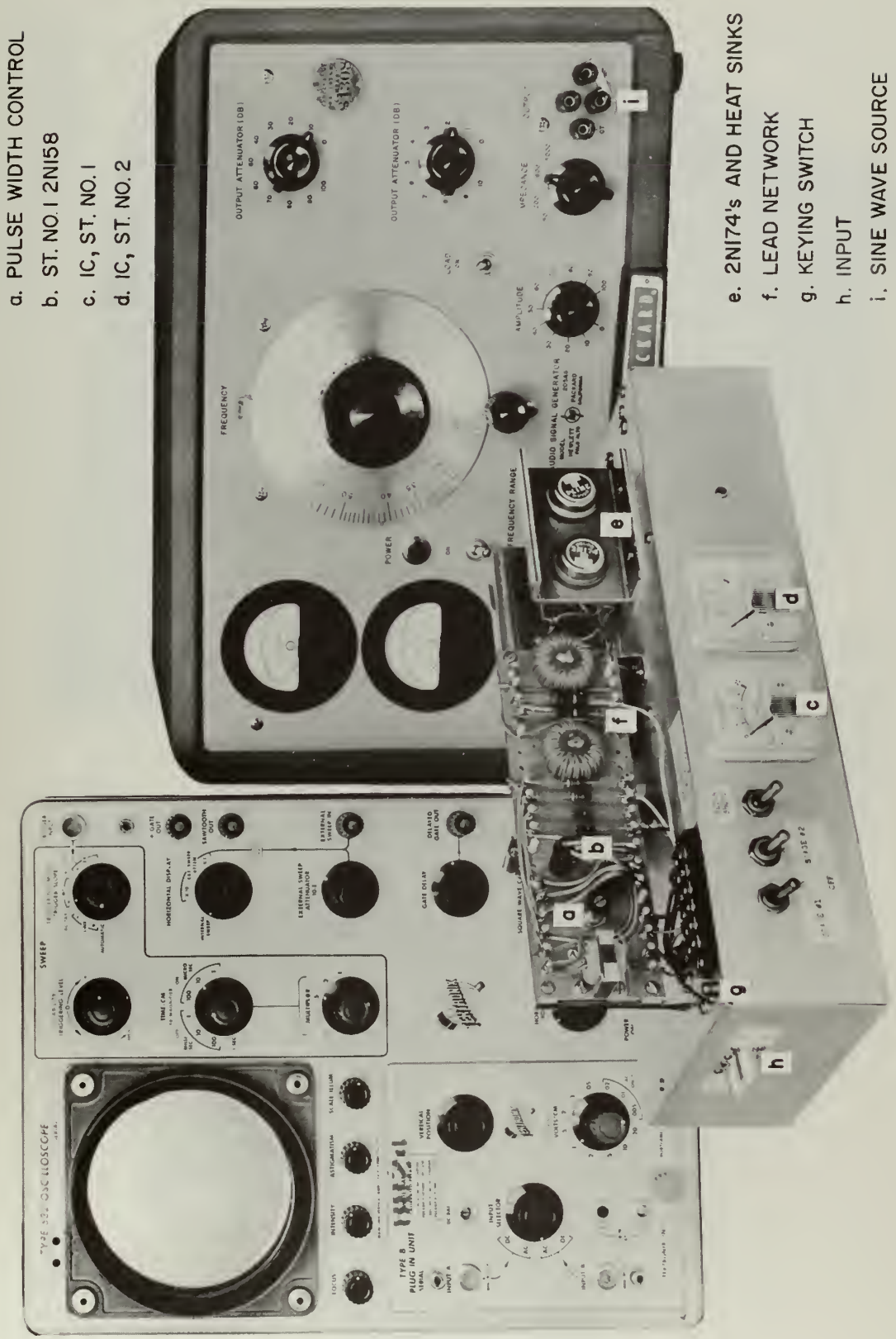


FIGURE I BREADBOARD AND TEST EQUIPMENT

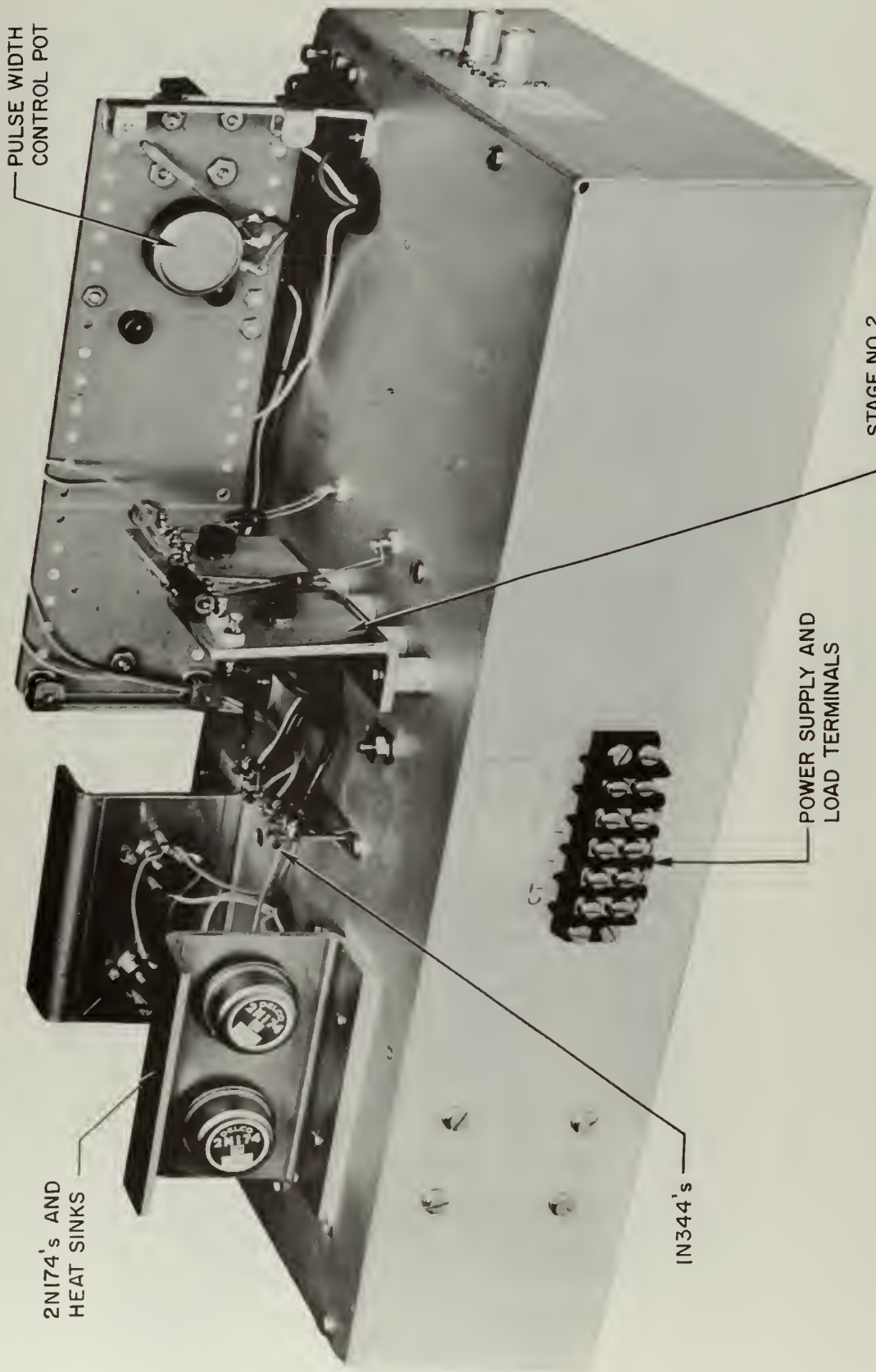


FIGURE 2 BREADBOARD, BACK VIEW

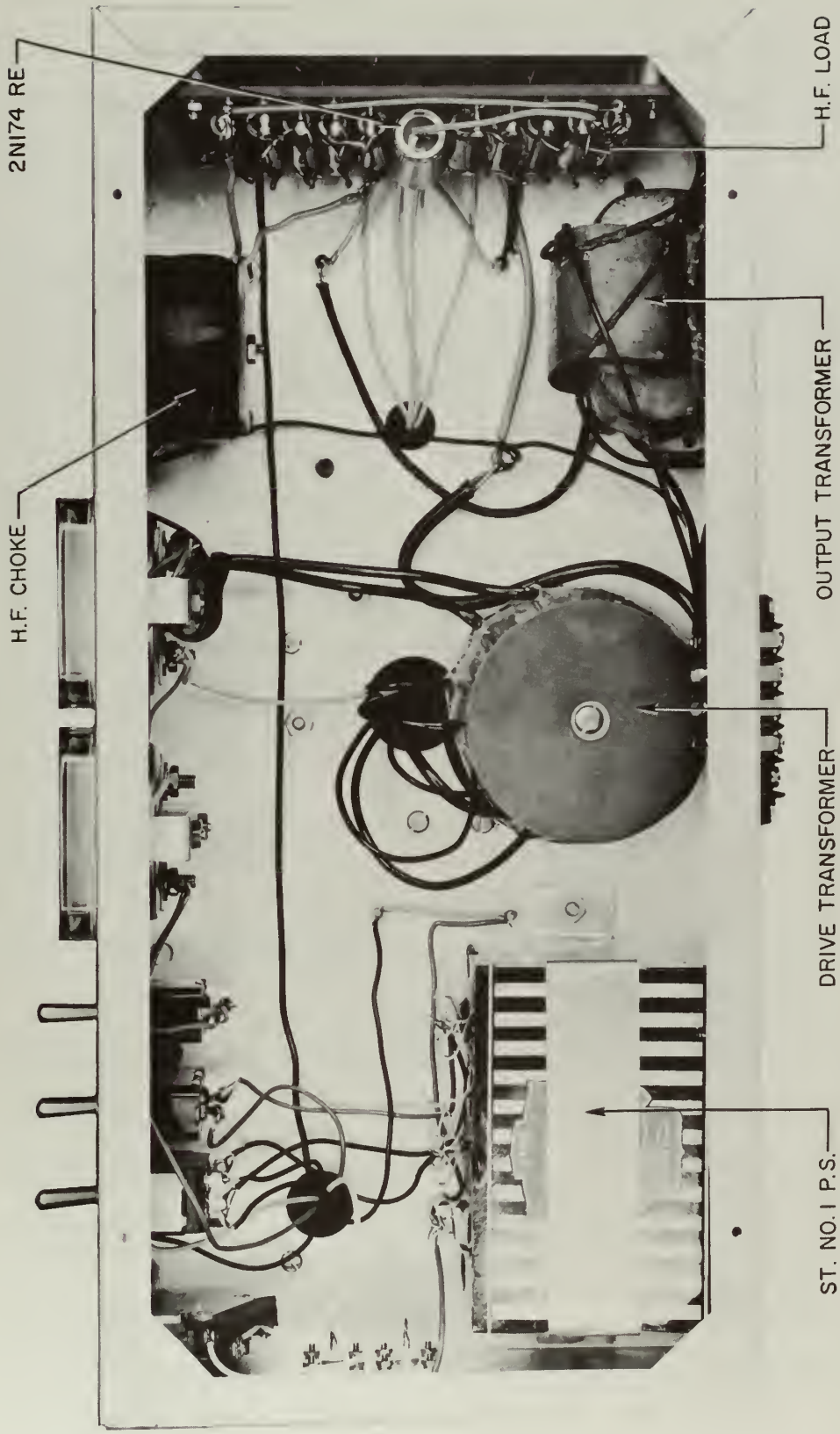


FIGURE 3 BREADBOARD, BOTTOM VIEW

APPENDIX V

TRANSISTOR ENGINEERING DATA

The information contained in this Appendix was taken directly from the Engineering Data Sheets supplied by the transistor manufacturers indicated.

DELCO 2N174

General Description: The improved Delco Radio 2N174 is a P-N-P germanium power transistor designed for general use with a 28 volt power supply and for use with a 12 volt power supply in applications where high voltage transients are encountered.

Absolute maximum ratings

Collector diode voltage Vcb (Veb = -1.5 volts)	80 volts
Emitter diode voltage Vebo	60 colts
Emitter current(continuous)	15 amperes
Base current(continuous)	4 amperes
Maximum junction temperature	
Continuous	95°C
Intermittent	100°C

Electrical Characteristics Temperature at 25°C

	Typical	Maximum
Collector diode current (Vcbo,-80)	2 ma	8 ma
Current gain h_{FE}(Vce,-2;Ic,12a)	20	
Saturation voltage (Ib = 2a, Ic = 12a)	.3 volts	.9 volts
Common emitter current amplification cutoff frequency f αe. (Ic = 5 a)	10 KCS	
Rise time (Ic = 12a)	15 usec	
Fall time (Ic = 0)	15 usec	
Thermal resistance (junction to mounting base)	.5	.8°C/watt

Fairchild 2N697

General Description: As a saturating switch, total switching times are a fraction of a μsec at 500ma. Gain bandwidth product is typically 100 megacycles. .... As a power output stage, it delivers 1.5 watts at 20 megacycles..... All production units are stabalized by extended 300°C. storage. The Fairchild mesa structure minimizes the effects of thermal and mechanical shock. Units have withstood impacts greater than 20,000 g for 3 ms.....

Absolute maximum ratings

Collector to emitter voltage (Vce)	40 volts
Collector to base voltage (Vcbo)	60 volts
Emitter to base voltage (Vebo)	5 volts
Electrical Characteristics (25°C)	
Current gain (h_{FE})	75 (typical)
Saturation voltage (Vbe)	1 volt
Total dissipation at case temperature of 100°C	1 watt
Saturation resistance (approx.)	10 ohms

Texas Instruments 2N1050

General Description: The Tl 2N1050 is an NPN diffused junction silicon transistor capable of 40 watts dissipation at 25°C with infinite heat sink.....

Maximum ratings

Collector voltage referred to base or emitter at 25°C	120 volts
Junction temperature (maximum range)	-65°C to = 200°C
Electrical Characteristics (25°C)	
Current gain (h_{FE})	30-90
Saturation resistance, (Ic = 200 ma)	15 ohms
Saturation voltage (Vbe), (Ic = 500 ma)	10 volts

Westinghouse 2N1016D

General Description: The Westinghouse WX1016 is a NPN fused silicon power transistor intended for high power switching and amplifier applications. The voltage and current ratings of this transistor, together with its very low saturation resistance, enable it to handle high switching powers with a minimum of losses.

Absolute maximum ratings

Collector to emitter diode voltage (Veb = -1.5 volts)	200 volts
Emitter diode voltage (Vebo) (Ic = 0)	25 volts
Emitter current(continuous)	5 amperes
Base current(continuous)	5 amperes
Maximum junction temperature	150°C

Electrical Characteristics (25°C)

Collector diode current (Vce = 200, Vbe = -1.5)	20 ma
Current Gain $h_{FE(min)}$	10
Common emitter current amplification cut off frequency (based on f α e = f α b/hfe)	30 KCS
Saturation voltage (Ic = 5 amperes)	2.5 volts
Thermal resistance (junction to case)	2.7°C/watt