Class-D Audio II Evaluation Board (HIP4080AEVAL2)

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Introduction

Historically, audio amplifiers have been configured as Class A, B or A/B and the art of design is well-known. Also well known is the poor efficiency of these types compared to that of Class-D amplifiers. Motor drive and power supply designers have been using Class-D (switching) amplifiers for many years because use of linear amplifiers would incur excessive power loss, except when driving tiny loads. When evaluating Class-D amplifiers in the audio bandwidth, Intersil has made available the HIP4080AEVAL2 Evaluation Board as a tool that enables the audio designer to immediately evaluate the Class-D topology. This Application Note will refer to this evaluation platform periodically (See also datasheet File Number 4018).

Whereas the theoretical best efficiency for Class-B amplifiers is 78%, the practical upper limit is more nearly 70% when driving a purely resistive load. But when driving real speaker loads which can have power factor angles of 60 degrees or more, efficiency can deteriorate to 55% or less. Class-D amplifiers, however, can attain efficiencies of 90%, and with careful component choices can exceed 95% efficiency. Moreover, the power factor of the load doesn't affect the on-state power losses in the MOSFET switches normally used in these amplifiers. Using Class-D techniques, amplifiers capable of delivering several hundred watts to the load can be designed using small, inexpensive, stamped heat sinks.

To review how poorly the efficiency of Class-B amplifiers can be, Figure 1 shows the ideal efficiency of a Class-B amplifier. The solid curve shows the ideal efficiency as a function of the power factor angle of the load current with respect to the applied load voltage. The dotted curve assumes that the peak output voltage will be 90% of the DC bus voltage level, which reflects a more realistic maximum efficiency level for various stray resistances in the output circuit.

The efficiency plots in Figure 1 do not include any losses due to bias current of the Class-B amplifier, used to minimize crossover distortion, which occurs as one of the transistors in the totem pole turns off and the other turns on. The bias power loss is the product of the bias current and the total bus voltage impressed across the output transistors and will further degrade Class-B efficiency shown in Figure 1.

Efficiency of Class-D amplifiers opens the possibility for powerful, small, light amplifiers with good sound quality to be designed today. The HIP4080A and related Intersil Intelligent Power Products ICs greatly simplify Class-D designs.

Class-D Efficiency

Class-D efficiency is largely determined by the ratio of the load resistance to the total DC loop resistance which is the sum of the $r_{DS(ON)}$ of the MOSFETs, wire resistances (including the output filter) and current sense resistor if used, and the load resistance. For highest efficiency, the MOSFET $r_{DS(ON)}$ resistances, shunt and filter resistances should be small compared to the load resistance. In audio Class-D applications, MOSFETs are used instead of IGBTs and Bipolar transistors because the switching frequencies required to keep distortion low at 20kHz signal frequencies can exceed 150kHz and neither Bipolar Power Transistors or IGBTs Switch efficiently at such high frequencies.

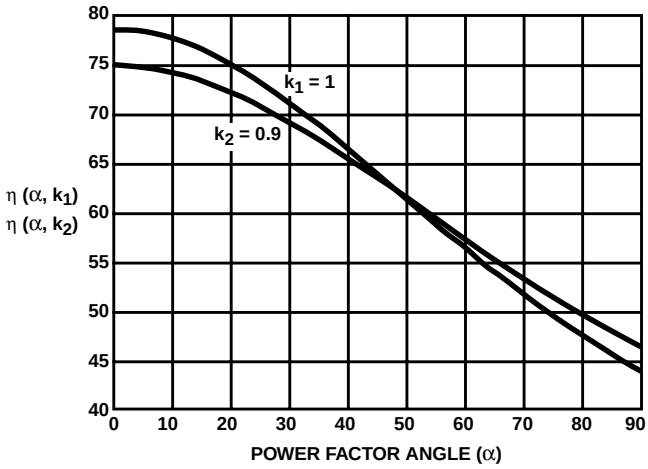

FIGURE 1. IDEAL/REALISTIC CLASS-B EFFICIENCY

For load current to flow in the Class-D bridge, two switches must be on simultaneously. The current flows through these, the stray and filter resistances, and the load. The instantaneous load current is related to the bus voltage as follows, where R_X includes all stray and filter resistances:

$$V_{BUS} = I_{LOAD}(2 \bullet r_{DSON} + R_X + R_{LOAD}) \quad \text{(EQ. 1)}$$

The RMS load current is related to the peak value of the load current and hence the DC bus voltage, due to the sinusoidal nature of the load current, as follows:

$$I_{RMS} = \frac{V_{BUS}}{\sqrt{2} \bullet (2 \bullet r_{DSON} + R_{LOAD} + R_X)} \quad \text{(EQ. 2)}$$

The power delivered to the load is the product of the square of the RMS load current and the load resistance, as Equation 3 shows:

$$P_{LOAD} = I_{RMS}^2 \bullet R_{LOAD} \quad \text{(EQ. 3)}$$

or, in terms of the bus voltage as Equation 4 shows:

$$P_{LOAD} = \frac{1}{2} \bullet \frac{V_{BUS}^2}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)^2} \bullet R_{LOAD} \quad \text{(EQ. 4)}$$

The total power is the product of the square of the RMS load current and the sum of the load, filter, stray wiring and $r_{DS(ON)}$ resistances of the two series MOSFETs as shown in Equation 5. The resistance, R_X, is the sum of all stray circuit resistances connecting the bridge with the load, including the resistances of the filter inductors, if any.

$$P_{TOTAL} = \frac{\frac{1}{2} \bullet V_{BUS}^2}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \quad \text{(EQ. 5)}$$

If switching losses could be ignored, Class-D efficiency is simply the ratio of the load resistance to the total power circuit resistance as viewed from the Bus supply as shown in Equation 6.

$$\eta = \frac{R_{LOAD}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \quad \text{(EQ. 6)}$$

With switching losses included, the total power dissipation and efficiency can be described as shown in Equation 7 and Equation 8 respectively, which are fully developed in the Appendix.

$$P_{TOTAL} = \frac{\frac{V_{BUS}^2}{2}}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)} \cdots \quad \text{(EQ. 7)}$$

$$+ f_{PWM} \bullet V_{BUS} \bullet \left[2 \bullet \frac{\left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \bullet \frac{2}{\pi} \right)^2}{I_{RATE}} \cdots \right.$$

$$\left. + I_{RATE} \bullet t_{RR}^2 \right]$$

$$\eta = \frac{\frac{R_{LOAD}}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)}}{1 + f_{PWM} \bullet \left[\frac{16 \bullet V_{BUS}}{\pi^2 \bullet I_{RATE} \bullet (2 \bullet r_{DSON} + R_{LOAD} + R_X)} \cdots \right.} \quad \text{(EQ. 8)}$$

$$\left. + 2 \bullet I_{RATE} \bullet \frac{t_{RR}^2}{V_{BUS}} \bullet (2 \bullet r_{DSON} + R_{LOAD} + R_X) \right]$$

For example, using the RFP22N10 MOSFET with a 4Ω load, a bus voltage of 36V, at a switching frequency of 240kHz, a commutation rate of 100A/µs, and a reverse recovery time, t_{RR}, of 100ns as shown below, would yield an operating efficiency of 84.1% given the conditions below.

$$R_{LOAD} = 4 \bullet \Omega \quad r_{DSON} = 0.08\Omega \quad V_{BUS} = 36 \bullet V$$

$$I_{RATE} = 100 \bullet \frac{AMP}{\mu s} \quad t_{RR} = 100 \bullet ns, \quad f_{PWM} = 240 \bullet kHz$$

If the t_{RR} jumps to 200ns, the efficiency decreases to 72.5%, so the MOSFET body diode recovery time plays an important role in determining efficiency.

Load impedance, also influences efficiency: For the values used above for the RFP22N10, the efficiency goes from 84.1% to 84.8% with an 8Ω load when switching losses are taken into account. With a 2Ω load, efficiency drops to 77.7%.

Nevertheless, Class-D efficiencies are much higher than comparable Class-A and Class-AB Systems. To optimize Class-D efficiency, one has to minimize the conduction and switching losses.

Figure 2 shows measured efficiency at a DC bus voltage of 30V using an Audio Precision Tester to calculate output power into a purely resistive 4Ω load. Notice that at very low output power, that the efficiency drops off dramatically. The onset of clipping of the output voltage waveform with a 30V. bus voltage occurred at an output power of 94W.

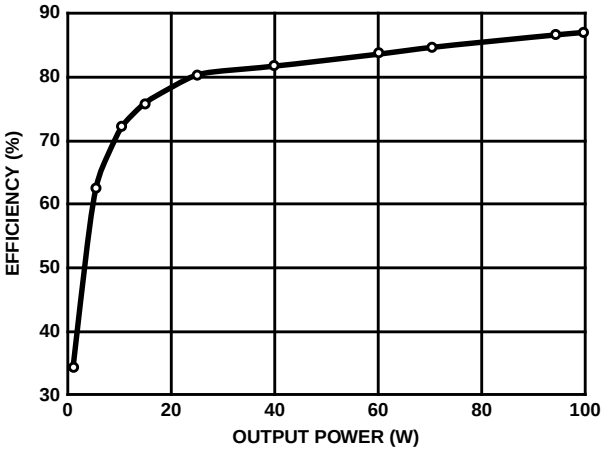

FIGURE 2. EFFICIENCY vs OUTPUT POWER (W)

MOSFET Choice, Bridge Dissipation

In order to properly choose the MOSFET switches (and heat sinks, if required by the design) one must be able to predict the MOSFET conduction and switching losses at the maximum power output of the amplifier. The full development, ending in Equation 9 below, is given in the Appendix. It is based upon the value of total power dissipation less sum of the load and stray power dissipation values previously calculated. One fourth of the bridge dissipation is the power developed in a single MOSFET switch.

$$P_{BRIDGE} = \left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \right)^2 \bullet r_{DSON} \cdots \quad \text{(EQ. 9)}$$

$$+ f_{PWM} \bullet V_{BUS} \bullet \left[2 \bullet \frac{\left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \bullet \frac{2}{\pi} \right)^2}{I_{RATE}} + I_{RATE} \bullet t_{RR}^2 \right]$$

In choosing MOSFETs, keep in mind that while a larger MOSFET goes hand-in-hand with minimizing the r_{DSON}, the gate capacitance increases with MOSFET size. Also the t_{RR} increases with MOSFET size. These comments apply to

MOSFETs generally. Nevertheless there is no substitute for studying the MOSFET Data Sheet. Even then, physical measurements are sometimes the only way to know for certain what commutation di/dt and reverse recovery time will result in a given situation.

Since minimizing the sum of both switching and conduction losses at the design frequency of interest will provide maximum efficiency of Class-D switching amplifiers, an understanding of the power dissipation components shown in Equation 9 which make up total MOSFET power dissipation is a must. See end-note [3] prior to the Appendix section.

Finally, the designer must weigh the cost tradeoff of heat sinking along with the cost of the MOSFETs in order to minimize the total system cost. The least expensive power section, moreover, may not be the most efficient.

Overcurrent and Short Circuit Protection

Audio amplifiers provide a voltage gain to amplify a signal from a preamplifier output. If the output is shorted, the amplifier will try to provide sufficient current to establish a voltage at the output which is equal to the input signal multiplied by the gain of the amplifier. Short circuit protection will help reduce down time and expensive repairs.

In addition to short-circuit protection, some form of current limit protection will reduce the output voltage applied across the load and can help to protect the amplifier and its load from overheating. The amplifier can also be protected from those who would connect too many speakers across the output or connect a speaker with too low an impedance.

Both of these fault modes, the direct short and the overload, require different protection schemes. In the case of the direct short, one usually wishes to disable the output drive as rapidly as possible and call attention to the condition by requiring some direct intervention by an operator to “reset” the amplifier. This can be as simple as incorporation of a reset button on the back of the amplifier, or a bit more inconveniently by requiring amplifier power down.

In the Intersil HIP4080AEVAL2 Audio Amplifier Board (refer to schematic at end of this application note), a reset button on the PC Board resets the amplifier after an overcurrent is detected. This level can be set via potentiometer, P4, from approximately 0A to 80A. (Tolerance, approximately 10%.)

The current limit circuit is of the spillover type, which means that when the current limit level is reached, the output of op amp, U5D, swings toward the +12V rail from its normal zero volt level. When the current reaches a level which turns on JFET, Q1, current is pulled through R14 at the output of the error amplifier, U5A. The op amps used in the HIP4080A demo board are Intersil type CA5470. The magnitude of the voltage output of the error amplifier is reduced before being compared with the triangle wave signal at the HIP4080A IN+ input pin. The current limit level, set by P2, provides overcurrent settings from approximately 0A to 80A. with a tolerance of approximately 10%.

The HIP4080A’s internal comparator compares the triangle wave and the error signal from the error amplifier, creating a Pulse Width Modulation signal, PWM. The PWM signal controls the gate outputs of the HIP4080A, which in turn control the power MOSFETs. The output of the MOSFET bridge is essentially a high voltage representation of the PWM waveform at the comparator output. When filtered by the low pass filter and the speaker load, this power PWM signal reconstructs the original audio input signal.

The short-circuit and current limit protection derive their current feedback signals from a 0.1Ω dropping resistor in the MOSFET bridge. Comparator U1B compares this feedback signal with the voltage set up by voltage divider, R4 in series with P4. The comparator output, normally at ground potential, will swing high under short circuit conditions and toggle the RESET pin of the U2A (D-Latch), in turn pulling the DIS (disable) pin of the HIP4080A high, disabling all gate outputs of the driver IC and turning off all MOSFETs in the bridge. The comparators used in the HIP4080A demo board are Intersil type CA3290.

During power up of the 12V supply to the HIP4080AEVAL2 Board, the U2A D-latch, Intersil type CA4013, is also reset, thereby, disabling the HIP4080A driver until after a time delay set-up by resistor, R7, and capacitor, C7. When the exponentially increasing voltage on C7 reaches or exceeds 6V, the output of comparator, U1A provides a positive clock pulse to the D-latch, thereby setting it. This action causes the LED, D1, to extinguish and the DIS pin of the HIP4080A to be pulled low, releasing gate pulses to the MOSFET bridge and enabling the amplifier output.

The HIP4080AEVAL2 demo doesn’t include a reliable means to short the error amplifier feedback circuit during power-up. As a result, “thumping” might be encountered during power-up. New designs should attempt to avoid this.

Power Supply/Biasing Considerations

Simplicity and low cost were also goals of the HIP4080AEVAL2 design. Consequently a single-polarity 12V power supply was chosen. Twelve volts avoids overdriving the MOSFET gates which would increase the internal power dissipation of the HIP4080A. Using 12V rather than +15V also decreases turn-off times of the power MOSFETs, thereby reducing somewhat the Miller feedback effect as well as the commutation di/dt rate and peak recovery current of the MOSFET body diodes due to a somewhat longer turn-on time.

Closing the Loop

Often, feedback techniques are used to linearize and maintain tight, consistent control of amplifier gain and frequency response. A high gain feedback loop will enhance transient response and minimize distortion over a wide frequency range. The frequency range of concern is 20Hz to 20kHz.

The design of the feedback loop to be used with a Class-D amplifier is a bit different from the one which might be used with a linear amplifier because there are no digital delays involved in the linear amplifier. The basic feedback block diagram used will nevertheless take the form of that shown in Figure 3.

In order to maintain feedback loop stability where a switching regulator or some other “digital” delay is involved, the feedback loop must have a unity gain crossover frequency

(rad/sec.) less than or equal to half of the frequency represented by the digital delay. In the Class-D amplifier there is a digital delay comprised of the PWM switching frequency. So if the switching frequency is chosen to be roughly ten times the maximum desired output frequency, say 240kHz, then unity gain crossover must be no higher than 120kHz.

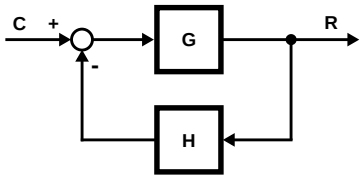

FIGURE 3.

In analyzing the feedback loop, we don't need to consider the high-pass filter at the front end of the amplifier, whose main purpose is to block DC input signals (or offsets) from being applied to the load. For simplicity purposes, we will also ignore the current limit circuit, since it is a spillover type and is not in the loop until the onset of current limiting. The loop will be designed to maintain a phase margin of at least 30 degrees.

With the above in mind, the control loop is comprised of the forward path which includes the error amplifier (Intersil CA5470), U5A, the pulse width modulator, PWM, comprising the triwave generator comparison with the error signal output from the error amplifier, and the gain associated with the MOSFET bridge. The PWM-Bridge combination can be modeled as a fixed gain with a single order delay term equal to:

$$\frac{1}{2 \bullet \pi \bullet f_{PWM}}$$

The feedback path of the feedback loop is comprised of the differential feedback amplifier, U5C, and the resistor which feeds the differential amplifier output signal to the error amplifier, U5A, summing junction. The differential amplifier gain should be set equal to the reciprocal of the desired closed-loop gain. If a $20V_{RMS}$ output is desired for a $1.0V_{RMS}$ input signal, for example, then the differential amplifier gain should be 1/20.

The differential feedback amplifier should also have a slew rate of at least 5V/µs unless input filtering is going to be used. If this isn't done, the feedback amplifier will not be able to respond to the high signal slew rates at the output of the MOSFET bridge inverter. The full power bandwidth capability should be at least 0.5MHz, to minimize input filtering. The Intersil, Type CA5470 op amp meets the minimum requirement with some input filtering so as not to exceed the amplifier's slew rate and bandwidth capabilities. The filter delays introduced into the feedback circuit must be compensated for by a similar lead term (zero) in the error amplifier transfer function. Since the feedback amplifier is a differential amplifier, the impedances looking out of each summing junction must be matched to ensure good common-mode rejection, since the common-mode voltage will contain large components of the switching frequency.

A simplified combination schematic/block diagram is shown in Figure 18 and a full schematic of the HIP4080AEVAL2 printed circuit board is shown in Figures 19 and 20 in the Appendix.

The generalized feedback control system is modeled basically as a forward gain block, G, whose input is the error signal from the loop summing node, and whose output is the output to the speaker. See Figure 3. "C" represents the input control signal and "R" represents the response or output. The summing node for the audio system is the inverting summing junction of the error amplifier, U5A, which actually sums currents. The equation which describes its transfer function can be easily developed, since we know that the gain of an inverting operational amplifier is simply the feedback impedance divided by the input impedance. Therefore, the error amplifier transfer function is, where s is the Laplace operator:

$$G_{ERR} = \frac{\frac{R_{LEAD} \bullet C_O \bullet s + 1}{C_O \bullet s}}{R_{IN}} \quad \text{(EQ. 10)}$$

The summing junction shown in Figure 4 sums currents rather than voltages and the error amplifier sums the current difference between the R_{IN} and the R_{FBK} resistors such that the difference between the currents must flow in the feedback impedance of the error amplifier.

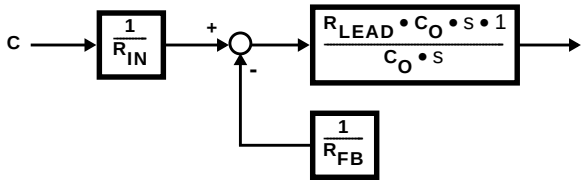

FIGURE 4.

Block diagram transformation techniques can be used to simplify Figure 4 so that the block representing the reciprocal of R_{IN} can be brought inside the loop, so that the control loop will sum voltages again and look more like the block diagram of Figure 3. To do this, the control loop equations representing the open-loop gain and the forward gain must be identical before and after the transformation. So in Figure 4 if we bring the factor $1/R_{IN}$ inside the loop, then the loop gain will have been reduced by the factor, R_{IN}. So, the loop gain must be multiplied by the factor R_{IN} to compensate for the initial reduction. Figure 5 shows the transformed, but identical section of the loop.

Notice that both the feed-forward and the loop gains of the systems in Figure 4 and 5 are identical. The partial loops shown in Figures 4 and 5 are incomplete because they don't include the gain of the PWM-Bridge Inverter in the forward path and the gain of the differential amplifier in the feedback path.

The PWM-Bridge Inverter gain, heretofore referred to as K_C, will be equal to simply twice the DC bus voltage divided by the peak-to-peak triangle wave voltage. For the HIP4080AEVAL2 demo, the bus voltage is approximately 36V and the peak-to-peak triangle wave voltage is about 5.5V to 6V. So K_C is about 12. Keep in mind that there is a transport delay due to the PWM switching frequency, which we could model as a first order delay of the reciprocal of the

PWM frequency. But if we just remember that we want to have unity open loop gain at about half of this frequency, we can ignore this delay in our analysis.

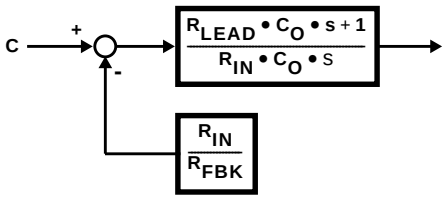

FIGURE 5.

The differential amplifier feedback gain, G_{DIF}, is shown in Equation 11A. The gain of a differential amplifier is simply the feedback impedance divided by the input impedance looking into the inverting input, provided that the impedances looking out of both summing junctions are exactly equal. That is why we specified earlier that tightly matched resistors should be used for the resistances making up this circuit. Usually 1% resistors are good enough, but the final decision is determined by how much common-mode rejection is desired. The quantification of the common-mode gain with component tolerance is outside the scope of this application note, but any good book on operational amplifier design and applications will go into this subject in detail.

$$G_{DIF} = \frac{\frac{R_{DIFFOUT}}{R_{DIF1} + R_{DIF2}}}{1 + \tau_{DIF} \bullet s} \quad \text{(EQ. 11A)}$$

where:

$$\tau_{DIF} = \frac{R_{DIF1} \bullet R_{DIF2}}{R_{DIF1} + R_{DIF2}} \bullet C_{DI} \quad \text{(EQ. 11B)}$$

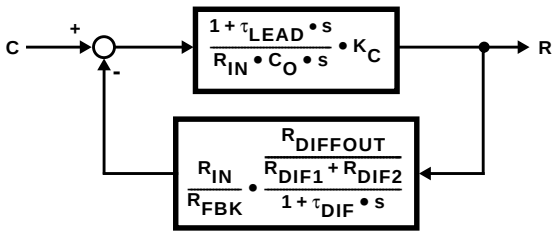

FIGURE 6. COMPLETED CLOSED-LOOP

The completed closed-loop Audio System Block Diagram is shown in Figure 6.

Figure 6 shows a forward gain block and a feedback gain block. Control theory requires that for closed loop stability, the open loop gain must be less than unity when the phase shift equals or exceeds 180 degrees. Also for frequencies below unity gain crossover, the closed loop gain (what the amplifier actually looks like if it were in a black box), 1/H, is the reciprocal of the feedback gain block. At frequencies above the crossover frequency, the closed loop gain approaches the magnitude of the forward gain block (i.e., what you would have if there were no feedback at all). There is little practical interest in frequencies above unity gain crossover, because the feedback effect is minimal there.

A closer look at Figure 6 shows that there is a zero in the forward gain block and a pole in the feedback gain block. If the time constants associated with the pole and zero are exactly equal, then their effect on the loop gain is eliminated and the loop looks like a pure integrator and is a Type 1 system with respect to output voltage, the variable being measured by the feedback. This type of loop exhibits zero error at DC, with increasing following errors at higher frequencies as predicated by the open loop gain at those frequencies.

What effect will certain changes in several component values have on performance? Decreasing R_{IN} will increase the magnitude of the output voltage of the audio amplifier without changing the open loop gain (stability and response are unaffected). This is because R_{IN} is in the denominator term of the forward gain and in the numerator of the feedback block. Increasing the feedback resistor, R_{FBK}, will increase the closed loop gain, but it will decrease open-loop gain and will therefore, have an effect on stability and response, so this component should never be used only to adjust amplitude gain of the amplifier.

If the feedback gain of the loop is satisfactory (you get the desired output amplitude for a given input signal magnitude), you can increase the open loop gain without disturbing the feedback gain by decreasing the value of C_O. To decrease the open loop gain, you can increase the capacitance value of C_O. Variations in bus voltage directly affect the gain constant, K_C, and the open-loop gain as well. Therefore, the open loop gain must provide stability at the highest bus voltage operating level which will be encountered. Ideally, the bus voltage won't vary a lot and this won't be a major concern. It could be a concern when attempting an amplifier design which is intended to be used on a variety of DC bus voltage levels. One way to avoid a problem is to increase R_{FBK} in proportion to any increase in bus voltage. While this will increase the closed loop gain, this is probably desirable so that the maximum output can be obtained from a constant input level, while keeping open loop gain constant.

The Bode plots shown in Figure 7 show a nice linear roll off with frequency of the open loop gain with a unity gain crossover of approximately 150kHz. The phase margin which is the angular difference between 180 degrees and the phase lag of the open loop gain (150 degrees for the compensation shown in Figure 7) is 30 degrees and the loop will be stable and reasonably damped. Further increases in open-loop gain will of course raise the crossover frequency of the loop and will encourage instability due to the switching frequency of the PWM. Crossover frequency increases must be accompanied by proportional increases in switching frequency. Unfortunately, this also tends to reduce efficiency due to increases in recovery losses and commutation losses in the bridge inverter.

Output Filter Requirements and Design

Class-D amplifiers differ from linear amplifiers in that switching amplifiers require an output filter capable of removing the high frequency components of the PWM waveform. The switching frequency components, while not audible, will radiate EMI from the wires going to the speaker. In cases where the speaker will be located together with the amplifier (pow-

ered speakers), the filtering may be either simplified or eliminated by appropriate shielding techniques. Several types of filter designs can be used and their advantages, disadvantages and design go beyond the scope of this application note. Several good references are available which will be helpful in the evaluation and synthesis of the popular filter types available (see end-notes [1] and [2]).

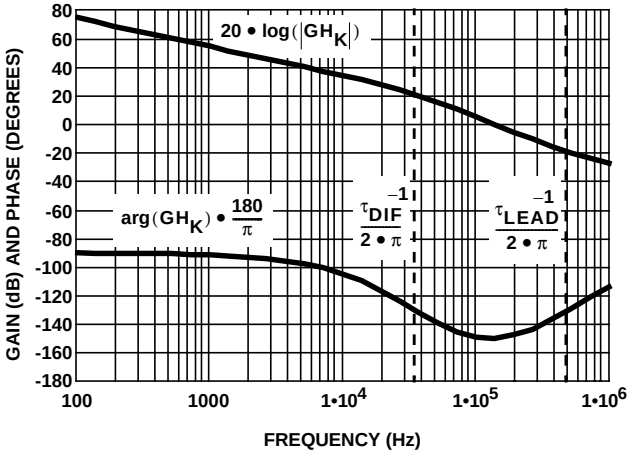

FIGURE 7.

The Butterworth Filter has a frequency response characteristic which most nearly fits the asymptotic response of a low pass filter of n-th order. The 4 pole Butterworth Filter rolls off at 80dB per decade of frequency. The Chebyshev Filter exhibits slightly sharper attenuation with frequency than the Butterworth, but with somewhat higher phase shift or signal delay. The Bessel Filter is optimized to produce a maximally flat delay in the passband and the step response has virtually no overshoot or ringing and the impulse response doesn't oscillate, but the frequency response is much less selective than in the other types and roll-off is not nearly as sharp as with the other types.

The HIP4080AEVAL2 Demo Board was designed using a 4-pole Butterworth Filter. Table 12-2 in the Electronic Filter Design Handbook was used to derive the values for a 4Ω load. A cut-off frequency of 30kHz was chosen and it was assumed that the source resistance of the inverter bridge was 0.1Ω. The values derived for the two inductors were 32.5µH and 23µH, respectively, and for the capacitors, 2.1µF and 0.508µF, respectively.

The sample calculation for the normalized filter component values shown in Equation 12 are based upon 30kHz and 4Ω, respectively, for the cutoff frequency and load impedance. Equations 13 and 14 show the equations which transform the normalized values into the actual values required for the filter. The cutoff frequency in radians/sec. are calculated from the desired cutoff frequency in Hz using Equation 15.

The Electronic Filter Design Handbook [2], Table 12-2 shows tables for normalized values for these filters. For the 4-pole filter, assuming 0.1Ω source impedance at the bridge input end of the filter, the normalized values are:

$$L1_{N:} = 1.5307 \qquad L3_{N:} = 1.0824$$
$$C2_{N:} = 1.5772 \qquad C4_{N:} = 0.3827 \qquad \text{(EQ. 12)}$$

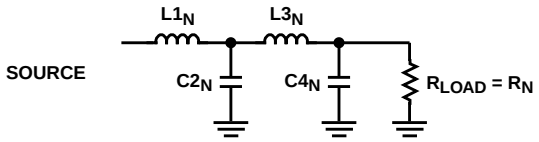

FIGURE 8.

The normalized values (see Figure 8) must be transformed to actual inductance and capacitance values at the cutoff frequency and load impedance desired using the following normalization transformations,

for the inductors:

$$LI = LI_N \bullet \frac{R_N}{\omega_{3dB}} \qquad L3 = L3_N \bullet \frac{R_N}{\omega_{3dB}} \qquad \text{(EQ. 13)}$$

and for the capacitors:

$$C2 = \frac{C2_N}{R_N \bullet \omega_{3dB}} \qquad C4 = \frac{C4_N}{R_N \bullet \omega_{3dB}} \qquad \text{(EQ. 14)}$$

where ω_{3dB} is the cutoff frequency in radians per second and R_N is the desired load resistance in ohms.

Therefore;

$$\omega_{3dB:} = 2 \bullet \pi \bullet 30 \bullet kHz \qquad \omega_{3dB:} = 1.885 \bullet 10^5 \bullet \frac{RAD}{SEC} \qquad \text{(EQ. 15)}$$

and; R_N = 4Ω for the HIP4080AEVAL2 Board. When the transformations shown above are performed, the following actual values for the filter components result:

$L1 = 32.482 \bullet \mu H$
$L3 = 22.969 \bullet \mu H$
$C2 = 2.092 \bullet \mu F$
$C4 = 0.508 \bullet \mu F$

Notice from the filter component transformation equations above that the actual values of the filter components are dependent upon the normalizing load resistance and the cutoff frequency. Both inductances and capacitances vary inversely with frequency, whereas inductances vary directly with load resistance and capacitances vary inversely with load resistance. For example, if the load resistance was changed to 8Ω then the capacitor values calculated above would be halved and the inductor values doubled if the cutoff frequency remained 30kHz.

Since the HIP4080AEVAL2 filter employs 2 inductors in each of the two output lines and 4 capacitors instead of two, the values of the inductors must be halved and the capacitors doubled as shown in Figure 9.

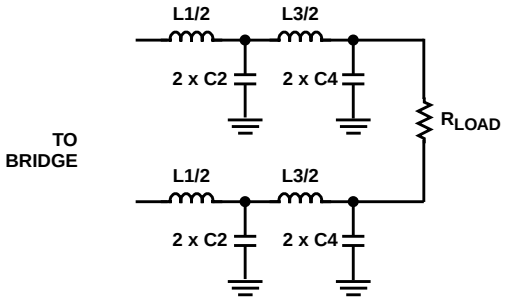

FIGURE 9. HIP4080AEVAL2 FILTER IMPLEMENTATION

Zobel Filter

In addition to the filter used to remove the PWM switching frequency content from speaker leads which may be routed near sensitive electronics, a Zobel Filter is used to make the chosen speaker look like a pure resistive load. With linear amplifiers, any phase delay between voltage and current in the output waveform would naturally result in a reduced power factor and a corresponding reduction in efficiency. Of course the efficiency of these amplifiers was already poor even at unity load power factor.

The normalized filter design tables assume that the load is purely resistive. Deviations from a pure resistive load causes filter pole shifting and deviation from the filter's characteristic performance.

Fortunately, it is easy to design a Zobel Filter, which basically consists of a series R-C circuit which is placed directly in parallel with the speaker load, which is assumed to be predominately a series R-L circuit. By setting the Zobel Capacitor equal to the inductance of the load divided by the square of the load resistance, cancellation of the load filter combination's reactance is facilitated and the combination looks just like the load resistance, R.

$$C_{ZOBEL} = \frac{L_{LOAD}}{R^2_{LOAD}} \quad \text{(EQ. 16)}$$

The Zobel Network Resistor in series with C_{ZOBEL} is set equal to the resistance of the load or speaker voice coil resistance. More information about compensating speakers is found in end-notes [4] and [5].

Conclusions

Distortion

Audiofiles and designers of audio amplifiers worry that Class-D amplifiers will exhibit excessive harmonic distortion. While the distortion plus noise at the highest frequencies seems to be somewhat higher than exhibited by linear amplifiers, the THD of Class-D amplifiers can be kept down to 1% or lower at the high end of the frequency range.

At the low end of the frequency range, Class-D amplifiers exhibit lower THD than Class-AB amplifiers exhibit. Crossover distortion of the Class-AB amplifier appears to cause this low-end distortion. Class-D exhibits distortion related to switching transients in the inverter bridge, which is generally low.

Nevertheless, at the high end of the frequency spectrum, Class-D amplifiers exhibit increasing THD, perhaps reaching or exceeding 1% at 20kHz and above. This phenomenon seems to be a result of open loop gain roll-off as the feedback loop crossover frequency is approached. The feedback loop exhibits less and less ability to adjust for distortion in the output waveforms as this point is reached. The gain of the HIP4080AEVAL2 Demo is about 10 at 20kHz, which means that the output signals will duplicate the input command signal with a following error of 10%. Fortunately, this doesn't mean that the resulting THD will be 10%, but it can contribute to an increase in distortion with frequency.

Another contributor to distortion is ringing on the PWM output terminals of the amplifier. Trapped inductances between the MOSFETs in an inverter leg of the bridge cause transient voltages comprising very high frequency components. Also, small discontinuities in the output waveform caused by the amount of dead time between upper and lower MOSFET conduction periods adds to distortion. While these components are beyond the cutoff frequency of the filter, some of these components make it through the filter and add to distortion. Figure 10 shows actual THD + N% versus frequency for the HIP4080AEVAL2 Demo Board which used a function generator to produce a more linear triangle wave than is produced by the on-board triangle wave generator. Distortion was found to be cut by half to two-thirds through use of an off-board linear triangle wave generator.

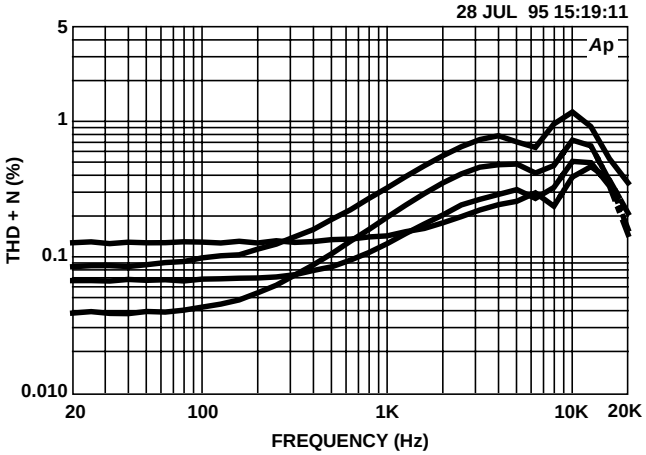

FIGURE 10.

In Figure 10, using 3kHz as a reference point, the plots from top to bottom reflect the THD + N% at output power of 70W, 25W, 5W and 1W respectively. The Audio Precision internal filters were set at 22Hz and 30kHz for the low and high frequency filters, respectively.

The trend toward higher distortion with rising frequency would occur even without a feedback loop, since the fixed PWM switching frequency and dead-time content means that at high frequencies the dead-time content occurs over a larger percentage of the output waveform cycle than they do at low frequencies. Also, an uneven distribution of these components undoubtedly occur from half-cycle to half-cycle.

Proof of the fact that the switching frequency effects the level of THD + N% can be seen from Figure 11, which shows THD + N% as PWM frequency is varied from 150kHz to 350kHz. The lowest distortion results occur at a switching frequency of 150kHz and the highest occurs at a switching frequency of 350kHz. At 100kHz, however, the distortion grows very large as the loop becomes unstable and the distortion is clearly evident in the output waveform. The curves in Figure 11 were created at a constant output power of 5W and a DC bus voltage of 30V using the Audio Precision 30kHz internal low-pass filter.

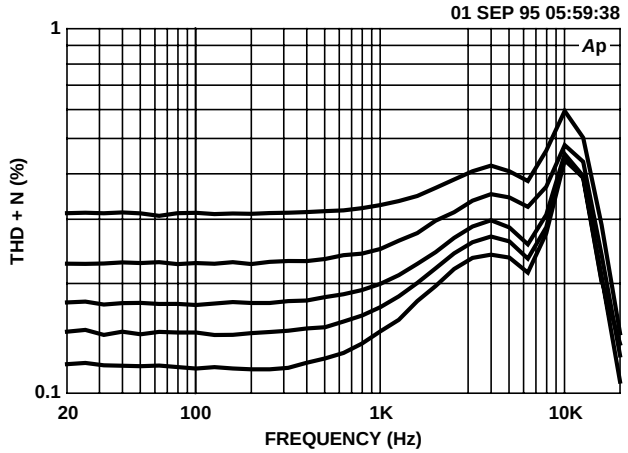

FIGURE 11. THD + N (%) vs FREQUENCY (Hz)

One other improvement was made which is reflected in generally lower distortion figures in Figure 12. The addition of phase to ground series R-C snubbers substantially reduce the voltage transients as viewed from the output terminals of the MOSFET bridge as power is swept from 0.3W to 100W at 1kHz. The snubbers reduce the THD + N% and protect the MOSFETs and the HIP4080A from undue voltage stress and possible failure. More about this in the "Other Design Considerations" Section.

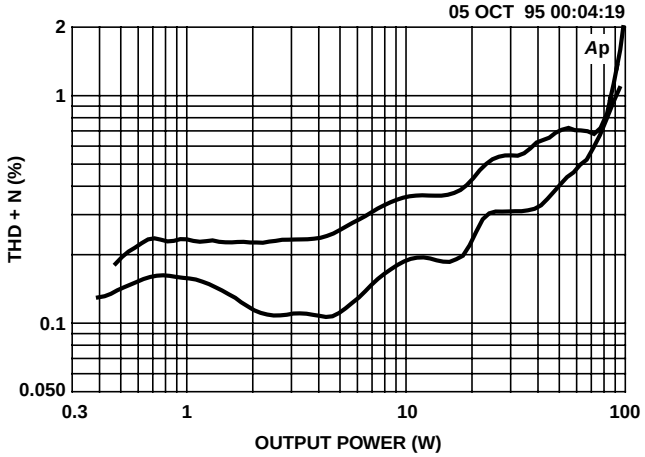

FIGURE 12. THD + N (%) vs OUTPUT POWER

Figure 13 shows a sweep of THD + N% as a function of input amplitude in V_{RMS} at two different excitation frequencies. The lowest value produced 1W into a 4Ω load, while the largest input value of 1V corresponded to 100W into the 4Ω load. The lower curve represents an input frequency of 1kHz and the upper represents an input frequency of 10kHz. As expected, the higher frequency produces more distortion as it becomes increasingly difficult for the control loop to regulate and as the dead-time content becomes a larger part of each cycle of the output waveform as mentioned earlier. The PWM switching frequency for this test was 240kHz, although as Figure 11 shows, better results might have been attained had 150kHz been used. In conclusion, listening tests indicate that the measured distortion of around 1% in the neighborhood of 20kHz is not discernible to the human ear, whereas distortion at the lower end of the frequency spectrum can be noticeable. But this is the very area where the Class-D amplifier shines.

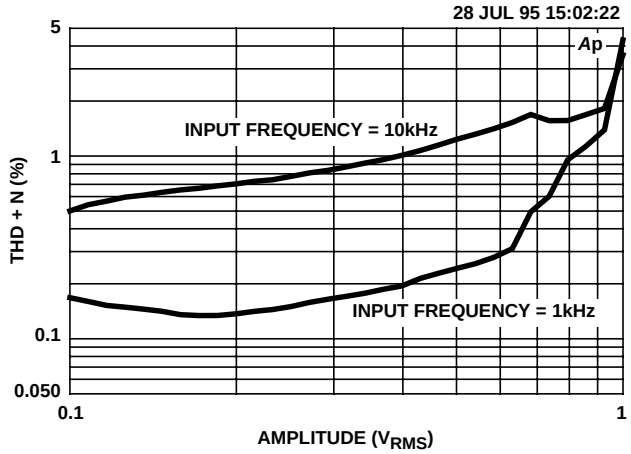

FIGURE 13. THD + N (%) vs AMPLITUDE (V_{RMS})

Intermodulation Distortion

Figure 14 shows CCIF % intermodulation distortion as a function of input amplitude with a 30V bus voltage. Approximately 100W is output with the input at 2.0V_{RMS}. The intermodulation distortion is comparable with the better Class B amplifiers. The CCIF Test uses two equal amplitude high frequency stimulus signals closely spaced in frequency. For the HIP4080AEVAL2 testing 19kHz and 20kHz signals were used. At the upper end of the power range, onset of clipping occurred.Bandwidth

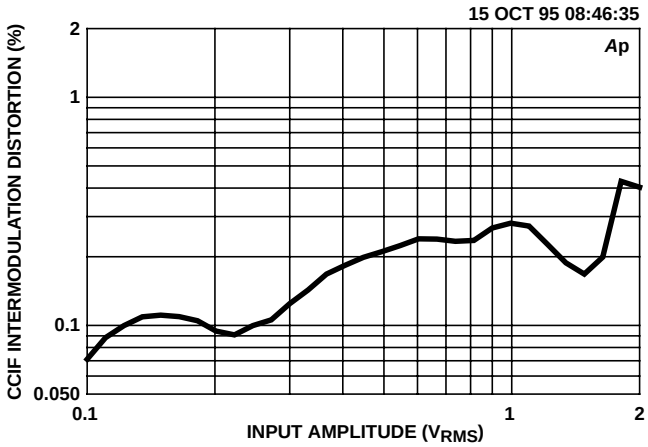

FIGURE 14.

Figure 15 shows the closed-loop frequency response of the HIP4080AEVAL2. The response is flat (under ±0.5dB) from 10Hz through 20kHz. The slight wiggle at the upper end of the passband may be due to the tolerance of the components within the 4-pole Butterworth Filter.

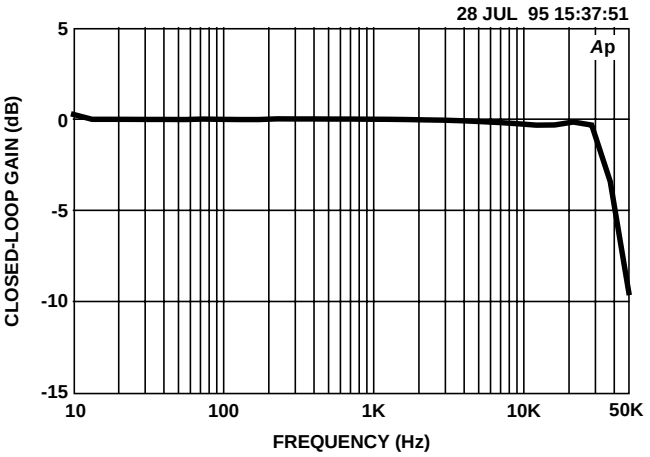

FIGURE 15. CLOSED LOOP FREQUENCY RESPONSE

Signal to Noise Ratio

Figure 16 shows the signal-to-noise ratio of the HIP4080AEVAL2 demo board, modified with the 2kΩ resistor in series with the input blocking capacitor. The two curves shown were performed with 1W and 10W output power to a 4Ω load. Excellent rejection seems possible with Class-D amplifiers

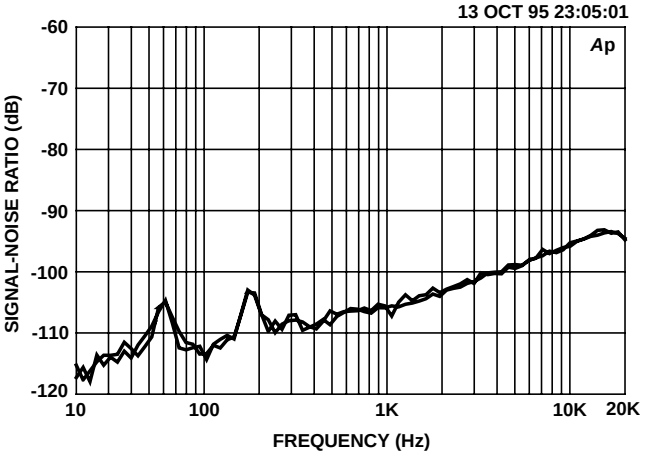

FIGURE 16. SIGNAL-NOISE RATIO BANDPASS (dBr) vs BPBR (Hz)

Other Design Considerations

Transient Suppression

As with all switch-mode amplifiers and power supplies, where high currents are being commutated between several MOSFETs in the power circuit, there are voltage transients. These voltage transients originate from an attempt to rapidly change the current flowing in trapped inductances within the bridge circuit and between the bridge circuit and the DC power source. Figure 17 shows the major sources of trapped inductance.

Since the largest stray inductance originates between the DC bus power supply and the bridge inverter, it is always advisable to apply either a capacitor or an RC snubber across the bridge inverter (from V+ to V- or ground).

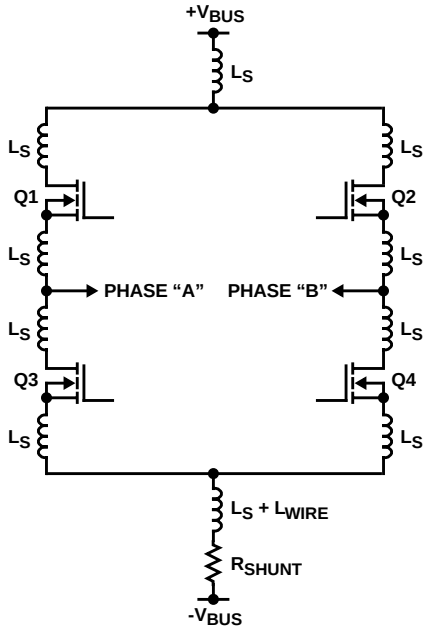

FIGURE 17.

While a simple capacitor will reduce the magnitude of voltage ripple (ringing) due to abrupt MOSFET switching transients, a resistor placed in series with the capacitor will dampen the ringing by absorbing the energy stored in these inductances. The value of the resistance should be kept low, so that the peak current spike will not develop an excessive voltage drop across the resistor. Usually a value from 1/2Ω to 5Ω is suitable. The capacitor must be large enough to absorb the energy from the trapped inductances. This energy, in joules, is given by the well known equation below.

$$\frac{1}{2} \bullet L \bullet I^2 \qquad \text{(EQ. 17)}$$

In practice, however, one does not know how much trapped inductance there is and the peak current may also vary due to variations in load current and variations in MOSFET body diode recovery currents. One is left making a best guess calculation of the required capacitance and leaving some room in the layout for a somewhat larger capacitor.

Figure 17 also shows that there are trapped inductances between the two MOSFETs making up each leg in the inverter, and between these MOSFETs and the positive and negative busses. This inductance is generally a lot smaller than the inductance in the loop between the inverter bridge and the supply source. Nevertheless this inductance generates transients across the individual MOSFETs, sometimes causing voltage spikes that exceed the bus voltage by 50% or more. The magnitude of these spikes are in direct proportion to the commutation di/dt and resultant recovery of the MOSFET body diode of the MOSFET which is turning off. Negative voltage transients are also common on the 'phase' or common point of an upper-lower MOSFET pair. When excessive, they can damage the HIP4080A or any other type of MOSFET driver for that matter.

One way to reduce the excessive voltage overshoot is to employ the Series R-C snubber from the phase to V_{BUS} terminals. This snubber will experience a lot more charge trans-

fer through it than does the DC bus snubber, because the phase voltage is a PWM-ed square wave operating at a switching frequency, f_{PWM}. The resulting power dissipation (watts) due to charging and discharging the snubber capacitor will be:

$$C_{SNUB} \bullet V_{BUS}^2 \bullet f_{PWM} \quad \text{(EQ. 18)}$$

Almost all of this power will of necessity be expended in the series snubber resistor. Judicious choice of capacitor value will result in using the smallest possible value of capacitance capable of controlling the transients on the phase node to acceptably safe levels and will result in a resistor power rating which is not so large as to cause your colleagues to smirk. Another consideration is, of course, distortion, since excessive phase voltage transients will translate into higher THD+N levels.

Layout Requirements

The layout recommendation in this section will cover both recommendations which we followed in laying out the HIP4080AEVAL2 Board and those which we subsequently discovered would yield further improvements in performance. This is done so that designers can reap the greatest benefits from Class-D amplifiers without having to reinvent the wheel.

The size of the snubber components mentioned previously will obviously be affected by the amount of trapped or stray inductances within the MOSFET inverter section. Therefore, techniques to minimize these inductances are worth the effort. The trace distances between MOSFETs should be minimized. Also the trace lengths between the MOSFETs and the positive and negative DC busses should be short. Large loops in the inverter bridge circuit should be avoided. Strive to use ground planes for one or both bus polarities. For example, make the negative DC bus bottom side copper and the positive DC bus top side copper.

Usually several R-C snubbers placed between positive and negative DC busses, one across each upper-lower MOSFET pair will minimize voltage transients and protect the MOSFETs and the driver IC. If some power supply ripple is expected, much larger (i.e., electrolytic) capacitors must be used in addition to the R-C snubbers.

Consider a separate ground plane for the signal level IC common connections. To minimize transients from the inverter from impinging upon the HIP4080A connection of the ALS and BLS pins are best connected to the signal common ground plane.

Component Choice

A good audio amplifier will require operational amplifiers with high gain-bandwidth product. The CA5470 amplifier used in the HIP4080AEVAL2 is capable of use in systems with a crossover frequencies upwards of 150kHz. For higher crossover frequencies choose a better amplifier. The amplifier used for the differential feedback should also have reasonably low input offset voltage or offset nulling capability should be added. The offset voltage of the amplifier reflected at the load will be 10 to 30 times greater depending upon the closed-loop gain.

The CA5470 amplifier's 15mV maximum offset can be almost 0.5V at the load. High frequency operational amplifiers need even more care in layout than low frequency op amps to ensure that they don't pick up noise from the power supply and that stray signals don't feed into the summing junctions. Therefore, keep the summing junction traces short and keep bias voltage traces away from high frequency signals. If in doubt place bypass capacitors on the power supply pins at sensitive op amps to enhance power supply rejection.

In performance evaluations of the HIP4080AEVAL2 Board, it was noticed that the distortion dropped significantly when the input gain pot was not full maximum setting. This was quickly traced to the fact that noise coming into the amplifier from external cables was coupled directly through the blocking capacitor to the summing junction of U5B. The simple addition of a 2kΩ resistor cured this problem and is a worthwhile addition on new designs.

Setup Procedures

Hookup

The HIP4080AEVAL2 Demo Board requires an external DC source of power to operate the MOSFET bridge, and a separate low voltage DC power source to power the 12V DC regulator which supplies power to the control ICs, bias circuits and the HIP4080A.

The low voltage supply is connected to terminals J4 (positive 15V to 20V) and J5 (negative or common). The high voltage DC (up to 40V maximum) should be connected to J2 (positive) and J3 (negative or common). If the desired high voltage DC supply is in the 15V to 20V region, one connection may be made for high and low DC power by bringing the high voltage into jacks J2 and J3 as described above and "jumpering" JP1 located between jacks J2 and J4 on the HIP4080AEVAL2 Demo Board. Since the on-board voltage regulator, U3 is a linear regulator, it will drop several volts between its input (J4 to J5) and the regulated output value which should be nominally 12VDC. For this reason, no less than 14V to 15V should be applied between J4 and J5.

The fuse, F1, is a 10A, 125V Buss GMC fuse which functions as backup protection for the Overcurrent Trip feature discussed below.

The HIP4080AEVAL2 Demo Board is designed to operate best with 4Ω loads, since the Zobel Filter design is designed for a 4Ω load and a typical speaker coil inductance of 16μH. The precise character of the Butterworth Filter is maintained only if the speaker is appropriately compensated. Refer to the section discussing the Zobel Filter for more information as well as the end-note references.

The sequencing of power application is really not critical, although when using separate supplies, it is customary to bring up the low voltage supply prior to the high voltage supply and, when powering down, it is customary to drop the high voltage supply prior to the low voltage supply. After the low voltage supply (and the high voltage supply, if these are tied together) is energized, the FAULT lite will momentarily light for several seconds. This is normal, unless it never extinguishes. If this happens, it may be that the overcurrent

trip potentiometer, P4, setting has been set too low. The proper setting of this pot is discussed under the section, Overcurrent Trip.

PWM Frequency Adjustment

The PWM frequency adjustment has been made at Intersil and is set for 240kHz. You may, however, wish to experiment with the effect different switching frequencies have upon THD+N. Turning the pot, P3, clockwise REDUCES the triangle wave frequency as viewed from pin 6 of U9C (See Figures 19 and 20 in the Appendix). However, do not attempt to reduce the frequency below 150kHz, because operating the triangle wave frequency too near the feedback loop crossover frequency will cause instability. Remember that the applied bus voltage alters the loop crossover frequency which impacts stability.

Overcurrent Trip

This setting has been made at Intersil and should not require adjustment. Potentiometer, P4, if turned clockwise, REDUCES the current level at which the overcurrent trip is latched. To raise the trip level, P4, must be turned counterclockwise, but it is not recommended to raise this level above that set by Intersil.

Current Limit

This setting has been made at Intersil and should not require adjustment. Potentiometer, P2, if turned clockwise, REDUCES the current level at which the current limit is attained and clipping of the output signal commences. To raise the current limit level, P2, must be turned counterclockwise. If the connected load needs to be protected at a lower level than the factory setting, then turn P2 clockwise to attain the correct level. First a dummy load which can handle the desired load must be connected to the HIP4080AEVAL2 output jacks and an input signal applied which results in the desired current limit output current. Then P2 may be adjusted downward until clipping just becomes apparent as viewed at pin 1 of U5A. In practice, this output can be more easily viewed from either end of resistor, R14.

[1] Schaumann, R., Ghausi, M.S., Laker, K. R., “Design of Analog Filters, Passive, Active RC and Switched Capacitor,” Prentice Hall, Englewood Cliffs, New Jersey 07632, 1990, Chap. 1-2.2

[2] Arthur B. Williams, “Electronic Filter Design Handbook,” McGraw Hill Inc., 1981.8/31/95 Page 1.

[3] An Excel/Lotus spreadsheet is available that incorporates HIP408x and MOSFET Power Dissipation calculations for “what-if” design considerations using different application requirements, i.e., Output Power, Load Impedance, $r_{DS(ON)}$, Clock frequency, etc. Butterworth Filter L and C component values are also provided for 2, 3 and 4 pole filters. This spreadsheet is located on the Intersil INTERNET http://www.intersil.com.

[4] Johnson, Jeffrey H., “Power Amplifiers and the Loudspeaker Load,” Audio, August, 1977.

[5] Staggs, Victor, “Exploring Loudspeaker Impedance,” Speaker Builder, May, 1994.

Appendix

Switching Loss Calculations

There are two components of switching loss, one having to do with commutating current out of the body diode of one of the MOSFETs into the drain of the opposing MOSFET upon turn-on, and a component due to the recovery energy of the body diode of the off-commutated MOSFET. These can be summarized as follows:

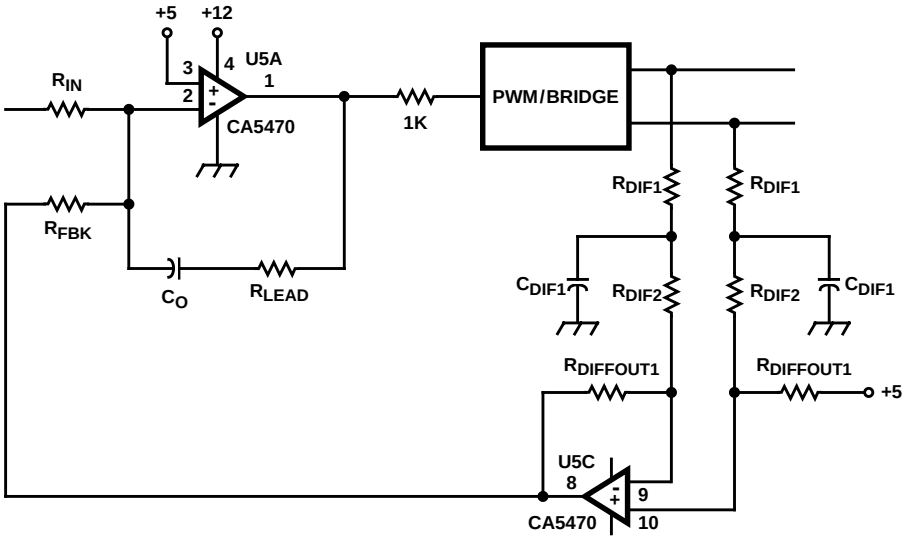

FIGURE 18. CONTROL LOOP SIMPLIFIED BLOCK DIAGRAM

For the commutating losses (one MOSFET):

$$P_{COMM} = \int_0^{t_{COM}} f_{PWM} \bullet V_{BUS} \bullet I_{LOAD} \bullet \frac{t}{t_{COM}}\, dt \quad \text{(EQ. 1)}$$

Which simplifies to:

$$P_{COMM} = \frac{1}{2} \bullet f_{PWM} \bullet V_{BUS} \bullet I_{LOAD} \bullet t_{COM} \quad \text{(EQ. 2)}$$

Since the average commutation time, t_{COM}, is related to the average current and the commutation di/dt, I_{RATE}, as follows:

$$t_{COM} = \frac{I_{AVG}}{I_{RATE}} \quad \text{(EQ. 3)}$$

For the diode recovery losses, a triangular current waveshape is assumed with a peak diode recovery current of I_{REC}. The blocking voltage V_{BUS} is impressed across the body diode once the peak recovery current point is reached. The total time during which reverse recovery current flows is defined as t_{RR} and the recovery energy is therefore, the integral of the current-voltage product over the recovery time:

$$J_{RR} = \frac{V_{BUS} \bullet I_{REC} \bullet t_{RR}}{2} \quad \text{(EQ. 4)}$$

Typically, the Intersil MOSFET Data Book gives the t_{RR} in conjunction with the initial forward current and the required di/dt resulting in the t_{RR} value given. If we solve for I_{REC} in terms of the di/dt rate and t_{RR}, we can then substitute for I_{REC} in terms of I_{RATE} and t_{RR} in the equation for energy. The energy-switching frequency product finally yields the recovery power loss.

$$P_{RR} = \frac{1}{4} \bullet V_{BUS} \bullet I_{RATE} \bullet t_{RR}^2 \bullet f_{PWM} \quad \text{(EQ. 5)}$$

The total power, P_{TOTAL}, is then the sum of the load and conduction losses as well as the switching losses:

$$P_{TOTAL} = \frac{\frac{V_{BUS}^2}{2}}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)} \ \ldots$$

$$+ f_{PWM} \bullet V_{BUS} \bullet \left(2 \bullet \frac{I_{LOAD}^2}{I_{RATE}} + I_{RATE} \bullet t_{RR}^2\right) \quad \text{(EQ. 6)}$$

The above general equation for total power uses the instantaneous load current I_{LOAD} for its determination. The average value of the maximum unclipped sinusoidal value for I_{LOAD} is related to V_{BUS} and R_{TOTAL} as in Equation 7 and will allow total power to be described without having to measure the actual load current.

$$I_{AVG} = \frac{V_{BUS}}{R_{TOTAL}} \bullet \frac{2}{\pi} \quad \text{(EQ. 7)}$$

The total power dissipation at maximum output magnitude and the corresponding efficiency are shown in Equation 8 and Equation 9, respectively.

$$P_{TOTAL} = \frac{\frac{V_{BUS}^2}{2}}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)} \ldots$$

$$+ f_{PWM} \bullet V_{BUS} \bullet \left[2 \bullet \frac{\left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \bullet \frac{2}{\pi}\right)^2}{I_{RATE}} \ \ldots \right.$$

$$\left. + I_{RATE} \bullet t_{RR}^2 \right] \quad \text{(EQ. 8)}$$

$$\eta = \frac{\frac{R_{LOAD}}{(2 \bullet r_{DSON} + R_{LOAD} + R_X)}}{1 + f_{PWM} \bullet \left[\frac{16 \bullet V_{BUS}}{\pi^2 \bullet I_{RATE} \bullet (2 \bullet r_{DSON} + R_{LOAD} + R_X)} \ldots \right.} \quad \text{(EQ. 9)}$$

$$\left. + 2 \bullet I_{RATE} \bullet \frac{t_{RR}^2}{V_{BUS}} \bullet (2 \bullet r_{DSON} + R_{LOAD} + R_X) \right]$$

MOSFET Power Dissipation Calculations

As Equation 10 shows, bridge power dissipation is the sum of conduction losses in the bridge and all commutation switching losses.

$$P_{BRIDGE} = \left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X}\right)^2 \bullet r_{DSON} \ \ldots \quad \text{(EQ. 10)}$$

$$f_{PWM} \bullet V_{BUS} \bullet \left[2 \bullet \frac{\left(\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \bullet \frac{2}{\pi}\right)^2}{I_{RATE}} + I_{RATE} \bullet t_{RR}^2 \right]$$

By substituting I_{PK} for:

$$\frac{V_{BUS}}{2 \bullet r_{DSON} + R_{LOAD} + R_X} \quad \text{(EQ. 11)}$$

in Equation 10 for bridge power above, a more intuitive result brings understanding to the power dissipation components of the bridge, Equation 12 below.

$$P_{BRIDGE} = I_{PK}^2 \bullet r_{DSON} \ldots$$

$$+ f_{PWM} \bullet V_{BUS} \bullet \left(2 \bullet \frac{I_{PK}^2}{I_{RATE}} \bullet \frac{4}{\pi^2} + I_{RATE} \bullet t_{RR}^2\right) \quad \text{(EQ. 12)}$$

The first term in Equation 12 is simply the product of the $r_{DS(ON)}$ of one switch and the square of the peak current which would flow if two switches and the load were placed directly across the bus potential. The second term represents the switching losses of the four MOSFETs comprising the bridge. The total power dissipation of one switch is simply one fourth of the total bridge dissipation as shown in Equation 13.

$$P_{SW} = \frac{P_{BRIDGE}}{4} \quad \text{(EQ. 13)}$$

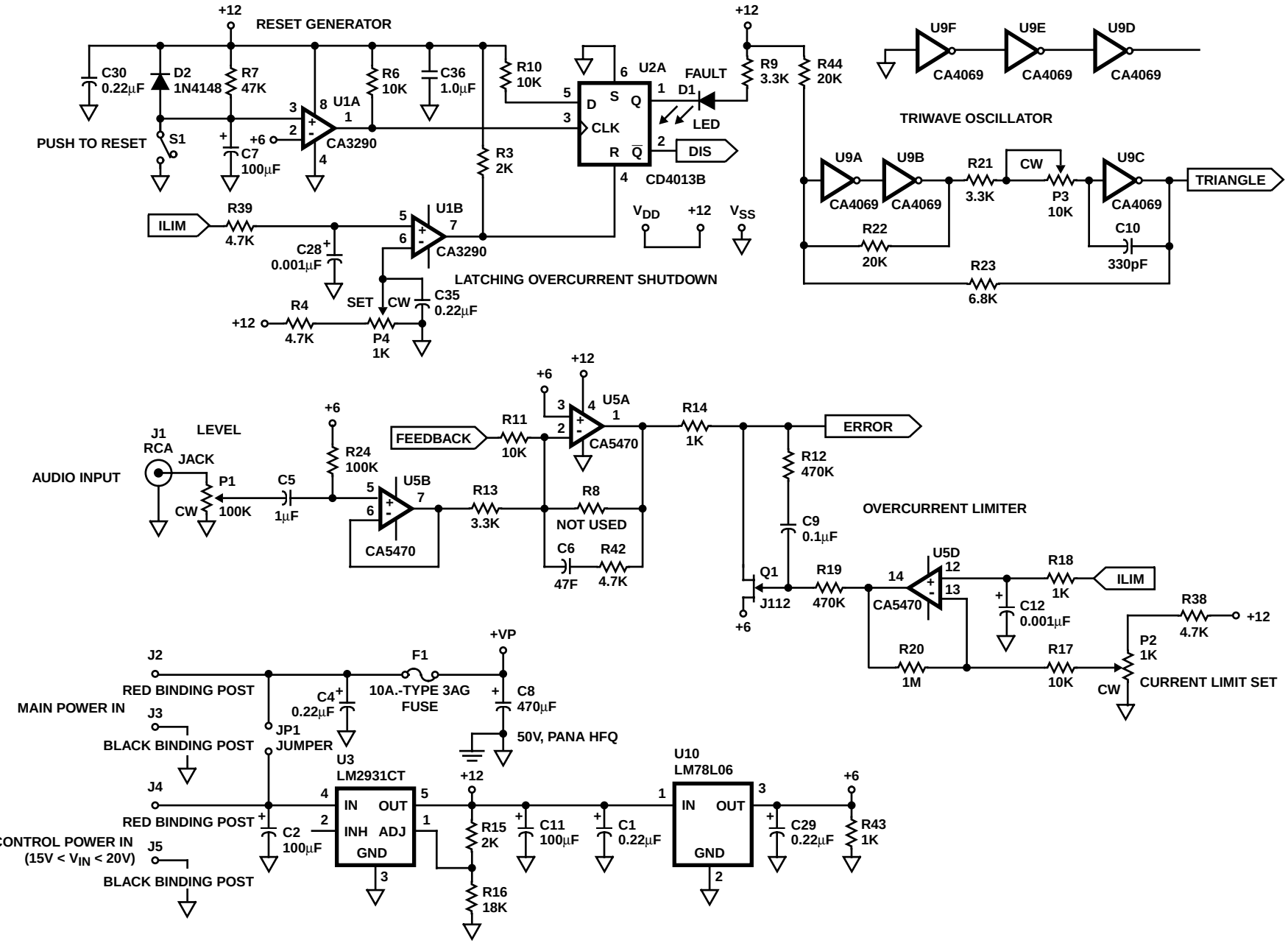

FIGURE 19. SCHEMATIC

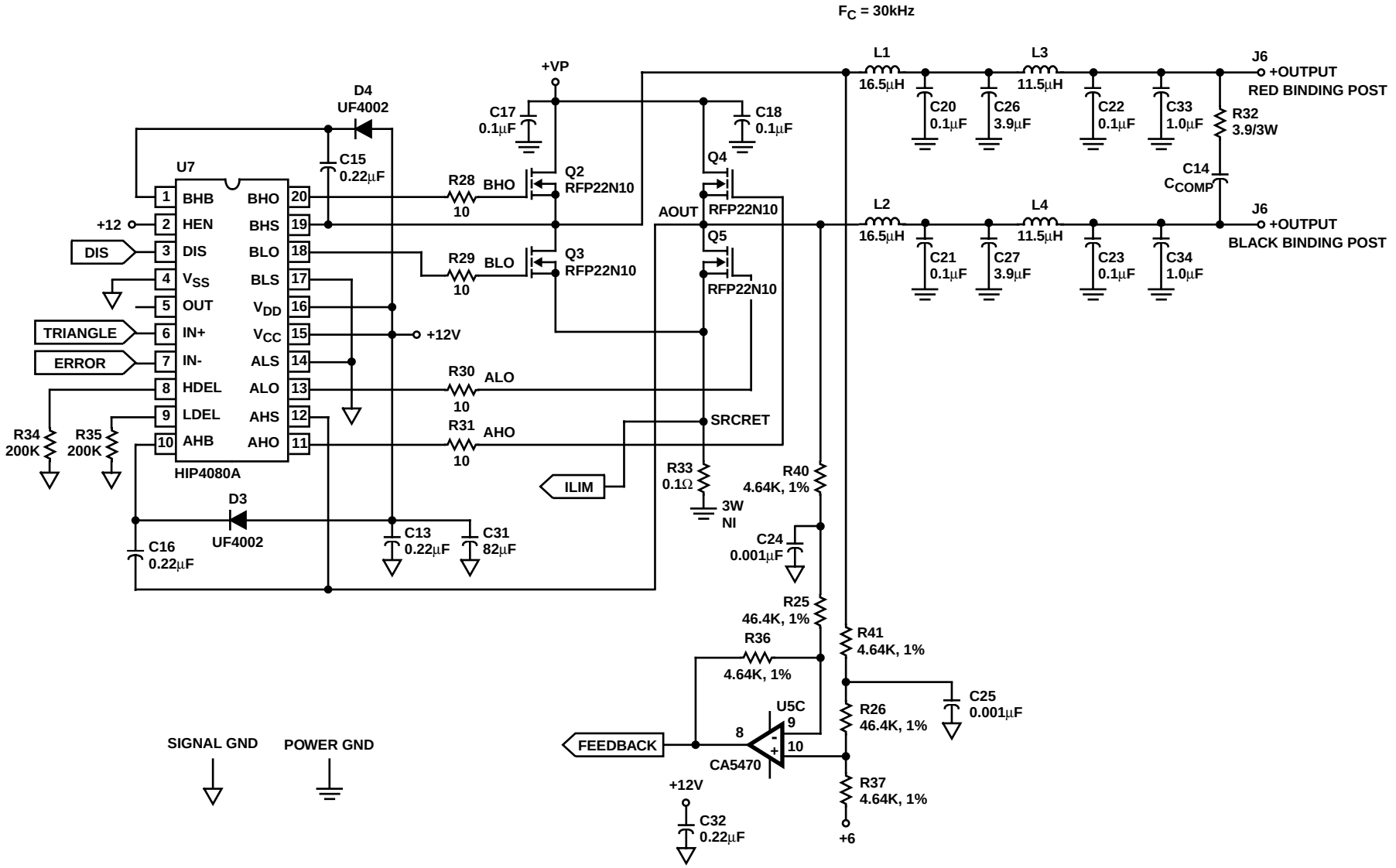

FIGURE 20. SCHEMATIC

HIP4080EVAL2 Parts List

LINE ITEM NO.	QTY PER PCB	REFERENCE DESIGNATION	DESCRIPTION	RETAILER				MANUFACTURER	
				NAME	STOCK NO.	CATALOG	PAGE	NAME	PART NO.
0	1	P.C.B.	Bare Circuit Board	EPC	HIP4080AEval2	-	-	E.P.C.	Rev C MK95
1	9	C1, C4, C13, C15, C16, C29, C30, C32, C35	0.22µF 63V Z5U 20% Mono Cer	Digikey	P4918	951	219	Panasonic	ECU-S1J224MEA
2	6	C17,C18,C20, C21,C22,C23	0.1µF 100V X7R 10% Mono Cer	Digikey	P4910	955	225	Panasonic	ECU-S2A104KBA
3	1	C2	100µF 50V Electro	Digikey	P6268	951	181	Panasonic	ECE-A1HU101
4	1	C5	1µF 50V Electro	Digikey	P6260	951	181	Panasonic	ECE-A1HU010
5	1	C6	47pF 100V NPO Cer Disk	Digikey	P4452	951	212	Panasonic	ECC-F2A470JCE
6	1	C7	100µF 10V Electro	Digikey	P6214	951	181	Panasonic	ECE-A1AU101
7	1	C8	470µF 50V Switch-grade Elect	Digikey	P5772	951	187	Panasonic	ECA-1HFQ471
8	1	C9	0.1µF 50V Radial Film	Digikey	P4525	951	205	Panasonic	ECQ-V1H104JL
9	1	C10	330pf 63V COG Mono Cer	Digikey	P4806	951	218	Panasonic	ECU-S1J331JCA
10	1	C11	100µF 16V Electro	Digikey	P6227	951	181	Panasonic	ECE-A1CU101
11	2	C12, C28	0.001µF 100V YP5 Cer Disk	Digikey	P4185	951	212	Panasonic	ECK-F2A102KBE
12	2	C33, C34	1µF 100V Radial Film	Digikey	EF1105	951	208	Panasonic	ECQ-E1105KF
13	1	C14	1µF 63V Radial Film	Digikey	P4548	951	205	Panasonic	ECQ-V1J105JM
14	2	C24, C25	0.001µF 100V Radial Film	Digikey	P4785	951	203	Panasonic	ECQ-B1102JF
15	2	C26, C27	3.9µF 100V Radial Film	Digikey	EF1395	951	208	Panasonic	ECQ-E1395KF
16	1	C31	82µF 16V Switch-grade Elect	Digikey	P5665	951	186	Panasonic	ECA-1CFQ820
17	1	C36	1µF 1210 50V Chip Cap	Digikey	-	-	-	Panasonic	-
18	1	D1	LED	Digikey	P300	951	137	Panasonic	LN21RPHL
19	1	D2	1N4148	Newark	1N4148	113	83	-	-
20	2	D3, D4	UF4002TR	Mouser	UF4002TR	-	-	Diodes, Inc.	-
21	1	F1 HOLDER	5X20mm Fuse Holder	Mouser	534-3527	-	-	-	-
22	1	F1	10A 250V FAST BLOW	Digikey	F955-ND	955	319	-	-
23	1	J1	RCA Receptacle, PC Mount	Mouser	161-4214	-	-	-	-
24	3	J2, J4, J6	Red Binding Post	Bisco	-	-	-	Keystone	7006
25	3	J3, J5, J7	Black Binding Post	Bisco	-	-	-	Keystone	7007
26	2	L1, L2	16.5µH (19t #20 on T106-3)	Amidon	-	-	-	Amidon	T106-3
27	2	L3, L4	11.5µH (24t #20 on T68-15)	Amidon	-	-	-	Amidon	T68-15
28	1	P1	100K Trimpot	Digikey	36C15	951	250	Panasonic	EVN-36CA00B15
29	2	P2, P4	1K Trimpot	Digikey	36C13	951	250	Panasonic	EVN-36CA00B13
30	1	P3	10K Trimpot	Digikey	36C14	951	250	Panasonic	EVN-36CA00B14
31	1	Q1	J112 N-Channel JFET	Allied	J112	113	32	Motorola	J112
32	4	Q2, Q3, Q4, Q5	RFP22N10	Intersil	SOAR	-	-	Intersil	-
33	4	Q2, Q3, Q4, Q5	Heat Sinks	Digikey	HS104-1	951	108	-	-
34	4	Q2, Q3, Q4, Q5	6-32 X 3/8" Machine Screws	Digikey	H356	951	301	-	-
35	4	Q2, Q3, Q4, Q5	Nylon washer, #6	Digikey	3370K-ND	951	299	-	-
36	4	Q2, Q3, Q4, Q5	Nut, 6-32 Hex	Digikey	H220	951	301	-	-
37	2	R3, R15	2K 1/4W CF 5% Resistor	Digikey	2.0KQBK	951	226	Yageo	-
38	4	R4, R38, R39, R42	4.7K 1/4W CF 5% Resistor	Digikey	4.7KQBK	951	226	Yageo	-

HIP4080EVAL2 Parts List (Continued)

LINE ITEM NO.	QTY PER PCB	REFERENCE DESIGNATION	DESCRIPTION	RETAILER				MANUFACTURER	
				NAME	STOCK NO.	CATALOG	PAGE	NAME	PART NO.
39	4	R36, R37, R40, R41	4.64K 1/4W 1% MF Resist	Digikey	4.64QBK	951	226	Yageo	-
40	3	R9, R13, R21	3.3K 1/4W 1% MF Resist	Digikey	3.3KQBK	951	226	Yageo	-
41	4	R6, R10, R11, R17	10K 1/4W CF 5% Resistor	Digikey	10KQBK	951	226	Yageo	-
42	1	R7	47K 1/4W CF 5% Resistor	Digikey	47KQBK	951	226	Yageo	-
43	1	R8	NOT INSTALLED	-	-	-	-	-	-
44	2	R25, R26	46.4K 1/4W 1% MF Resist	Digikey	46.4KQBK	951	226	Yageo	-
45	2	R12, R19	470K 1/4W CF 5% Resistor	Digikey	470KQBK	951	226	Yageo	-
46	3	R14, R18, R43	1K 1/4W CF 5% Resistor	Digikey	1KQBK	951	226	Yageo	-
47	1	R16	18K 1/4W CF 5% Resistor	Digikey	18KQBK	951	226	Yageo	-
48	1	R20	1M 1/4W CF 5% Resistor	Digikey	1MQBK	951	226	Yageo	-
49	1	R22	20K 1/4W CF 5% Resistor	Digikey	20KQBK	951	226	Yageo	-
50	1	R23	6.8K 1/4W CF 5% Resistor	Digikey	6.8KQBK	951	226	Yageo	-
51	1	R24	100K 1/4W CF 5% Resistor	Digikey	100KQBK	951	226	Yageo	-
52	4	R28, R29, R30, R31	10 1/4W CF 5% Resistor	Digikey	10.0QBK	951	226	Yageo	-
53	1	R32	3.9Ω 5% 3W	Digikey	P3.9W-3	951	227	Yageo	-
54	1	R33	0.1 3W 5% WW Resistor	Digikey	SC3D-0.1	951	228	Yageo	-
55	2	R34, R35	200K, 1/4W CF 5% Resistor	Digikey	200KQBK	951	226	Yageo	-
56	1	R44	20K, 1/4W CF 5% Resistor	Digikey	20KQBK	951	226	Yageo	-
57	1	S1	Push Button Switch	Mouser	102-1271	-	-	C&K	8121SD9AV2GE
58	1	U1	CA3290E	Intersil	CA3290E	SOAR	-	-	-
59	1	U2	CD4013BE	Intersil	CD4013BE	SOAR	-	-	-
60	1	U3	LM2931CT	Digikey	9192B-ND	951	89	National	-
61	1	U5	CA5470E	Intersil	CA5470E	SOAR	-	-	-
62	1	U7	HIP4080AIP	Intersil	HIP4080AIP	SOAR	-	-	-
63	1	U9	CD4069UBE	Intersil	CD4069UBE	SOAR	-	-	-
64	1	U10	78L06 Voltage Reg.	Digikey	NJM78L06A	-	-	Motorola	-
65	1	SU1	8-pin IC Mach. Screw Sockets	Digikey	AE7208	951	75	Assmann	-
66	3	SU2, SU5, SU9	14-pin IC Mach. Screw Sockets	Digikey	AE7214	951	75	Assmann	-
67	1	SU7	20-pin IC Mach. Screw Sockets	Digikey	AE7220	951	75	Assmann	-
68	4	Standoff	Board Standoff	Newark	81N2587	113	1226	-	-

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