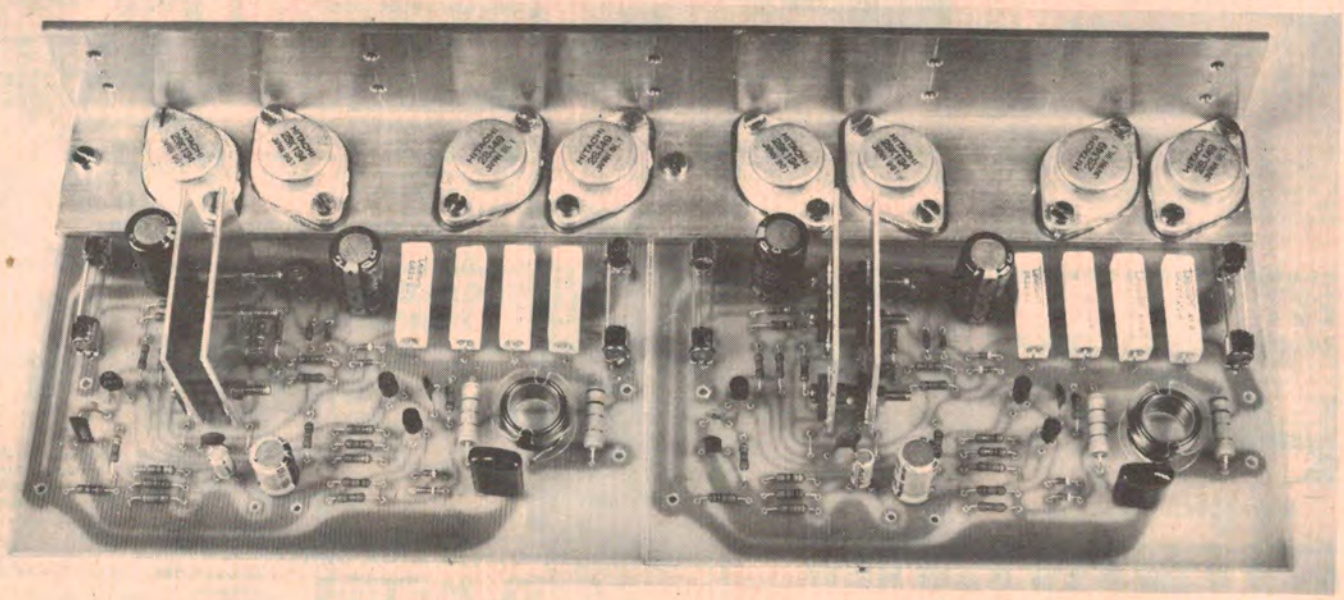


MOSFET power amplifier

Part 2.

David Tilbrook

This month we continue with the discussion on the amplifier's design, followed by further construction details to enable you to build a stereo power amplifier using two modules.

LAST MONTH we decided on the use of the MOSFET output devices, and can now proceed with the design of the rest of the power amplifier. The biggest problem is the reduction of distortion in the output stage. In most power amplifiers this is accomplished with negative feedback.

There is a trend at the present away from amplifiers with large amounts of overall negative feedback. Claims have been made that negative feedback is the cause of transient intermodulation distortion and results in amplifiers with dubious stability characteristics. The anti-negative feedback purists have suggested that 10-20 dB of overall negative feedback should be considered the maximum in a high-quality audio amplifier. To my knowledge, however, and on the basis of numerous experiments into the problem, there is no sound engineering basis for this position. So long as a good stability margin is maintained and providing the amplifier is designed so that the feedback loop will not saturate on any input signal, with the exception of an amplitude overload, there is no reason why 40-60 dB *or more* of negative feedback could not be applied.

In order to understand the relationship between negative feedback and distortion it is necessary to look at some of the fundamentals of feedback amplifiers.

The modern transistor power amplifier is similar to the IC op-amp. Both have an input difference amplifier, followed by a voltage gain stage or stages. The output from the voltage gain stage is fed to the output stage that provides a sufficiently low output impedance to drive the expected load. Figure 11 is a block diagram of a typical power amplifier.

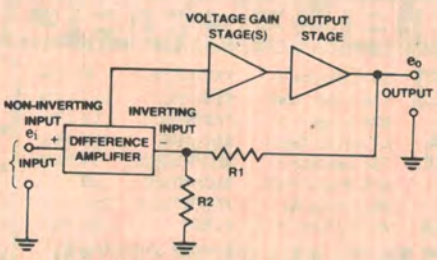


Figure 11

The difference amplifier has two inputs. A signal applied to the *non-inverting* input will be amplified and *appears at the output with the same phase as the input signal.* A signal applied to the *inverting* input is also amplified but *appears at the output with the oppositve phase to the input signal.* The non-inverting input is sometimes referred to as the positive input and is generally marked on diagrams with a '+', while the inverting input is sometimes referred to as the negative input and is marked on diagrams as a '−'.

If identical signals are fed to both inputs simultaneously, the result at the output is 0 V. i.e: only the difference between the two input signals will appear at the output.

In Figure 11 the input signal, e_i, from the output of the preamplifier, is applied to the non-inverting input of the difference amplifier. The output signal voltage, e_o, is attenuated by the resistive potential divider formed by R1 and R2 and then fed to the inverting input of the difference amplifier. If we assume that the input impedance of the inverting input is high, the output signal voltage, e_o, will give rise to a signal current through R1 and R2 to ground. So:-

$$i_o = \frac{e_o}{R1 + R2} \text{ by Ohm's law.}$$

The signal voltage developed across R2, which is the signal voltage seen by the inverting input, is given by:-

$$i_o R2, \text{ or } \frac{R2 e_o}{R1 + R2}$$

Now, if the output signal e_o is at 0 V while the input e_i is taken slightly positive, the input stage will amplify the difference between the two voltages and feed this signal to the voltage amplifier where it is further amplified. The output signal from the input stage is proportional to the difference between the input and the output of the power amp and is therefore often referred to as an *error* signal. In this case, the error signal is a positive-going voltage that will cause the output stage to drive in the positive direction until the voltages on the two inputs of the differential amplifier are identical. To do this it must take the output signal voltage to a higher voltage than the input in order to compensate for the attenuation in the potential divider.

$$\text{Specifically, } e_o = e_i \cdot \frac{R1 + R2}{R2}$$

The factor (R1 + R2)/R2 defines the relationship between the input and output signal voltages and therefore is the gain of the power amp — sometimes called the *closed loop gain*.

The total voltage gain in the difference amplifier, voltage amplifier and output stage is called the *open loop gain* since this is the gain the amplifier would have if the negative feedback were not there. If the open loop gain was infinite, then no matter how small the error voltage became, the feedback loop could reduce it still further. Real amplifiers always have a finite open loop gain and so the equation for the closed loop gain gives us really only an approximation. Nevertheless, this is the biggest single advantage of feedback amplifiers. The gain, and therefore the transfer characteristic, is ostensibly a function of the ratio of resistors R1 and R2, provided that the open loop gain is high enough.

Consequently, feedback amplifiers are capable of extremely good performance and it is significant that almost any power amplifier available today uses this basic technique.

There are of course disadvantages to the negative feedback approach. If, for any reason, the output signal e_o cannot follow the input signal e_i, the error voltage will increase dramatically. Since the amplifier has access only to a limited supply rail (even the national power grid is a limited supply rail !), the feedback loop will clip if the error signal becomes too great. Once the amplifier overloads in this way it will remain 'latched up' for a period before recovering. The ability of the circuit to recover from overload is simply referred to as *overload recovery* and is another factor contributing to the difference in sound between amplifiers.

It is important that the amplifier can recover quickly and cleanly from an overload situation. Some amplifiers actually burst into oscillation momentarily as they pass into and out of an overload situation. This can be difficult to see on an oscilloscope if the effect is relatively minor, but it will have a profound influence on the sound of the amplifier.

Although it is true that negative feedback amplifiers are more likely to suffer badly from this problem than open loop amplifiers, it should be realised that all amplifiers suffer from this problem. The two instances where this is likely to occur are *amplitude limiting* and *slew rate limiting*. When the output voltage reaches one of the supply rails and the amplifier 'clips', the feedback loop will swing hard against

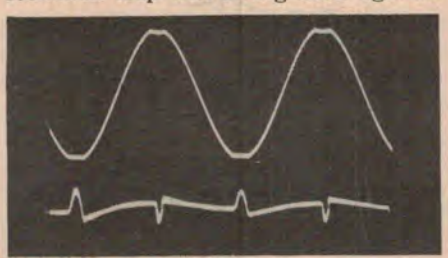
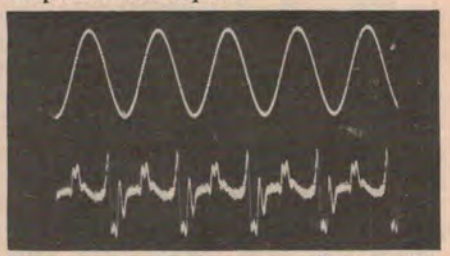


Figure 12

the opposite rail. Figure 12 is an oscilloscope picture showing the feedback loop of the ETI-477 MOSFET power amp module trying to correct for a 100 W RMS, 1 kHz sinewave that is being clipped slightly on peaks. Notice that the feedback loop comes out of overload quickly and with no sign of oscillation.

Transient intermodulation distortion

The second instance that leads to saturation of the feedback loop occurs when the signal slope of the input exceeds the slew rate of the amplifier. That is, when the signal rises or falls faster than the amplifier can. In this case, the feedback loop simply cannot 'catch' the input signal and the amplifier will be momentarily operating without feedback (open loop). As I mentioned earlier, this is one of the more controversial aspects of feedback amplifier techniques.



A bad case of TIM. Upper trace — 25 kHz power output sinewave. Lower trace — distortion. Notice that the distortion is greatest for the middle portion of the sine wave, where slew rate is highest.

The claim is made that negative feedback makes an amplifier susceptible to transient intermodulation distortion. Since a bipolar output stage is usually the slowest stage in the amplifier, it will take the longest to react to a transient input signal with high input signal slope. The argument is that since the input signal is present on the non-inverting (+) input of the difference amplifier, but not on the inverting (−) input, since it has been delayed by the output stage, the error voltage will increase to the point of clipping, thereby overloading the driver stage and generating gross distortion.

It is easy to demonstrate by experiment that this effect *does in fact occur*, and it is true that beyond the slew rate limit, the presence of a negative feedback loop will make the problem worse. *It is equally true*, however, that the negative feedback loop worsens the distortion above the amplitude limit, or clipping point, and for *exactly the same reasons*. Once the feedback loop is overloaded, either by clipping or slew rate limiting, it will take a finite time to recover and this adds an audible form of distortion to the output signal.

The point is that no high quality amplifier should be operated above its slew rate limit.

The usual approach is to ensure that the slew rate limit is high enough in the first place and to precede the input stage with a low-pass filter to limit the ▶

maximum possible signal slope of any input signal. In this way, extreme slewing distortion *cannot occur*, since no signal at the amplifier's input can exceed the slew rate limit.

As the input signal approaches the maximum slew rate, the distortion will increase, just as it does when the signal amplitude approaches the clipping point. Under these conditions however, the negative feedback loop *may actually decrease* the amount of transient intermodulation distortion by generating the appropriate error signal.

A good qualitative indicator that an amplifier is free from TIM is its square wave response. Remember that a relatively high frequency square wave (about 10 kHz) passed through a low pass filter with a 3 dB point of around 30 kHz for example, should not look square. (See Picture I on page 28 of last month's issue.) The filter gives rise to the exponential shape of the rising and falling edges and clearly limits their signal slope. Furthermore, since the ear is roughly a 20 kHz low pass filter itself, you will perceive no difference in the sound of these two signals. A power amplifier that is free from TIM should produce a 10 kHz square wave that has exponential leading and trailing edges like the waveform in Picture I last month. There are several extremely fast amplifiers on the market at present whose square wave response will look square, even at 10 kHz. If their square wave response is analysed on a high speed CRO, however, the leading and trailing edges of a 10 kHz square wave would still have an exponential shape.

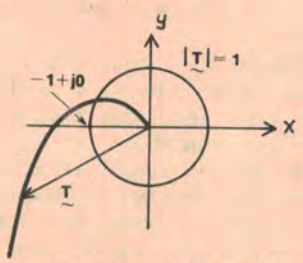
In this analysis of the TIM mechanism, the term slew rate has been used in reference only to the slew rate of the slowest active device. If the power amplifier has been designed for minimum TIM, and consequently has been fitted with an input filter to limit the maximum possible input signal slope, the filter will determine the slew rate of the amplifier. The slew rate specification quoted by most amplifier manufacturers is meaningless when it is not known whether this slew rate is determined by an active device or by a passive input filter.

Stability of feedback amplifiers

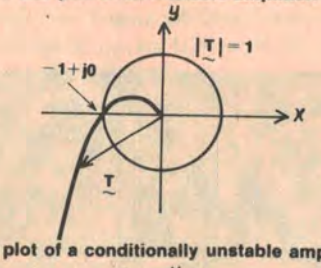
By far the biggest problem encountered with feedback amplifiers is the stability. The difference amplifier stage achieves its differencing effect by summing signals that are inverted with respect to each other; i.e: they have a 180°, or π rad., phase difference. If any reactive component in the load or the amplifier itself is allowed to cause a phase shift of more than $\pm 90°$ ($\pi/2$ radians) the differencing function of the amplifier becomes a *summing* function and oscillation results. If the oscillation occurs it will invariably lead to gross distortion in the audible range, even if the oscillation itself is well above 20 kHz. In the worst case, full power output at these frequencies (typically between 50 kHz and 1 MHz) will lead to almost instantaneous heating, and possible destruction, of the output devices and perhaps the loudspeakers.

There are some amplifiers that destroy tweeters with monotonous regularity. These amplifiers are usually those with marginal stability characteristics and can be improved with some modification to their design.

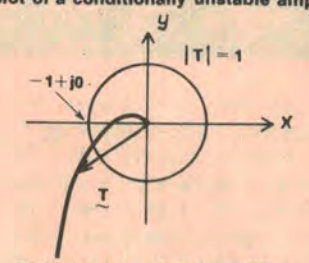
The basic rule for stability of a feedback loop is the *Nyquist Stability Criterion*. This says that the amplifier will be stable if the loop gain is less than unity when the phase shift of the loop reaches 180°. This is best shown as a polar plot like that in Figure 13. On the polar diagram, the loop gain is represented as a vector quantity, $\underset{\sim}{T}$. This is because both the phase and the magnitude of the loop gain change as a function of frequency. The phase is



Polar plot of an unstable amplifier.



Polar plot of a conditionally unstable amplifier



Polar plot of a stable amplifier.

Figure 13 **Nyquist stability diagrams.**

HOW IT WORKS — ETI 477

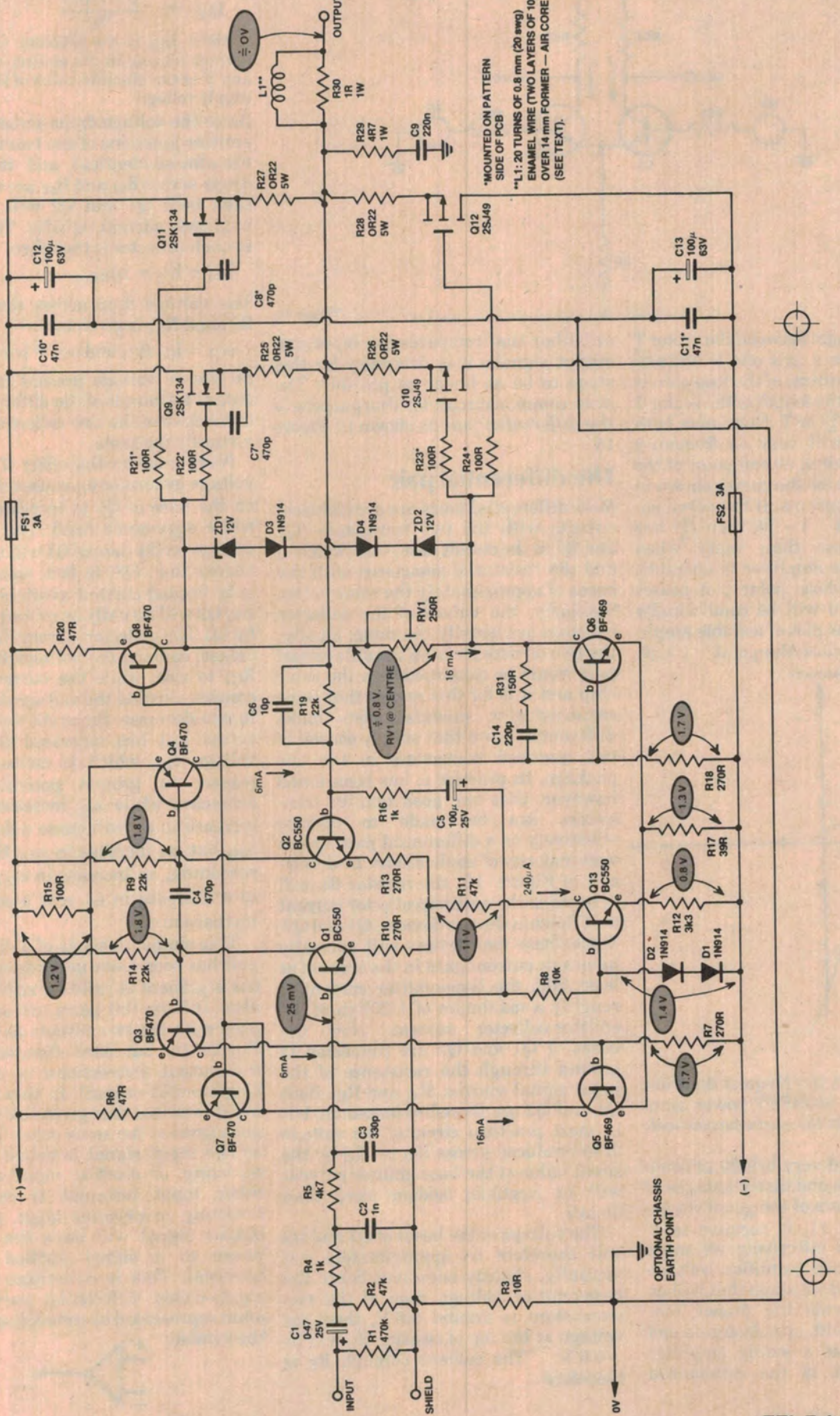
This description is confined to a dc analysis.

The input signal is fed to three RC filter sections formed by C1R2, R4C2 and R5C3. The C1R2 filter defines the low end 3 dB point of the amplifier at around 7 Hz, with an attenuation rate below this frequency of 6 dB/octave. The two sections R4C2 and R5C3 both have 3 dB points of around 30 kHz defining the top end response of the amplifier. This filter limits the maximum signal slope to less than the slowest stage in the amplifier. It also provides protection against RF interference. Resistor R1 ensures that the positive side of C1 always remains at the 0 V potential for reasons discussed in the main text.

Transistor Q13 and the associated components R8, R12 and D1, D2 form a constant current source (or sink), maintaining a final dc current through the differential pair Q1, Q2 of around 240 mA. Under no-signal conditions this current is shared equally between Q1 and Q2. The resistances of R9 and R14 are in parallel with the equivalent input resistances of the transistors Q3, Q4, decreasing the effective load resistance of the differential pair to around 15k. The voltage drop across R9 and R14 should therefore be 1.8 V approximately. This voltage, minus the 0.6 V drop of Q3 and Q4, will cause a voltage drop of 1.2 V across resistor R15, causing a current of 12 mA to flow in this resistor. This current is shared by Q3 and Q4 and causes a 1.7 V drop across resistors R7 and R18. Once again, the effective input impedance of Q5 and Q6 is in parallel with the resistors, but in this case the value of R7 and R18 is very much lower than the base impedances of Q5 and Q6, so this effect can be ignored in a dc analysis like this. The voltage across R7 and R18 minus the 0.6 V drop of Q5 and Q6 will cause 1.3 V to be dropped across the 39 ohm resistor R17, giving rise to around 32 mA through the resistor. Again Q5 and Q6 form a differential pair, and this current is shared equally by the two transistors. The load for these devices is formed by a current mirror, Q7-Q8, that ensures the current through Q5 and Q6 will remain the same. Transistors Q4 and Q5 therefore form the main voltage gain section of the amplifier and have a typical emitter-collector current of 16 mA. The preset RV1 will drop nominally 1 V across it when the output stage quiescent current has been set.

Diodes D3, D4 and zeners ZD1, ZD2 protect the MOSFET output devices from being overdriven, as described in the text. The RC-RL network on the output ensures that the amplifier has a correct load at all frequencies, thereby eliminating the problem of oscillation that could otherwise result.

This very brief analysis of the circuit is intended only to help the constructor rationalise the voltages quoted on the circuit diagram. The voltages are the result of averaging voltage measurements on a number of prototypes, and slight deviations from these should be expected. A more detailed description of the operating principles is given in the main text.


OUTPUT.
÷ 0V
L1**
R30 1R 1W
R29 4R7 1W
C9 220n
R27 OR22 5W
R28 OR22 5W
Q11 2SK134
Q12 2SJ49
C12 100µ 63V
C13 100µ 63V
C8* 470p
C10* 47n
C11* 47n
R25 0R22 5W
R26 OR22 5W
Q9 2SK134
Q10 2SJ49
C7* 470p
R21* 100R
R22* 100R
R23* 100R
R24* 100R
FS1 3A
FS2 3A
ZD1 12V
D3 1N914
D4 1N914
ZD2 12V
RV1 250R
± 0.8 V. RV1 @ CENTRE
16 mA
R20 47R
Q8 BF470
Q6 BF469
C6 10p
R19 22k
R31 150R
C14 220p
Q4 BF470
6mA
R16 1k
C5 100µ 25V
Q2 BC550
1.7 V
R18 270R
1.3 V
R17 39R
0.8 V
1.8 V
R15 100R
R9 22k
C4 470p
R13 270R
R11 47k
240µA
Q13 BC550
R12 3k3
D2 1N914
D1 1N914
R14 22k
R10 270R
Q1 BC550
R8 10k
1.2 V
1.8 V
11 V
1.4 V
R7 270R
Q3 BF470
-25 mV
6mA
1.7 V
R6 47R
Q7 BF470
16mA
Q5 BF469
C3 330p
R5 4k7
C2 1n
R4 1k
R2 47k
R3 10R
C1 0·47 25V
R1 470k
OPTIONAL CHASSIS EARTH POINT
INPUT
SHIELD
0V
(+)
(-)
*MOUNTED ON PATTERN SIDE OF PCB
**L1: 20 TURNS OF 0.8 mm (20 swg) ENAMEL WIRE (TWO LAYERS OF 10) OVER 14 mm FORMER — AIR CORE (SEE TEXT).

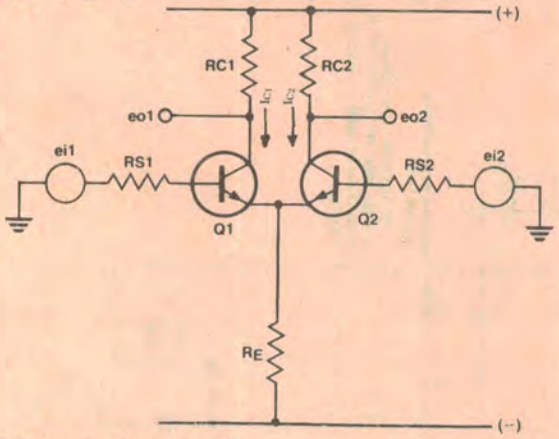


Figure 15

shown as the angle between the vector $\underset{\sim}{T}$ and the positive x axis and is written: arg $\underset{\sim}{T}$. The magnitude of the loop gain is represented by the length of the vector T and is written $/\underset{\sim}{T}/$ or T. Now, since both arg $\underset{\sim}{T}$ and T will vary as frequency varies, the terminal or end point of the vector will describe the curves shown in the Nyquist diagrams. If the curve encloses the point $-1 + j0$, then $/\underset{\sim}{T}/$ has not become less than unity when arg $\underset{\sim}{T} = \pi$ so the amplifier is unstable. An amplifier whose polar plot passes through $-1 + j0$ will be conditionally stable. The polar plot of a stable amplifier will not enclose the point $-1 + j0$.

Figure 14

Figure 14 shows the Nyquist diagram for the ETI-477 MOSFET power amp. module. *Note that the curve passes well inside* $-1 + j0$.

We have looked very briefly at some of the advantages and disadvantages of feedback amplifiers of the general type shown in Figure 11. If negative feedback is to work effectively we must design a difference amplifier, voltage gain stage and output stage that will go together to provide the proper conditions of phase shift, open loop gain and slew rate so that a stable amplifier results. Since it is the differential amplifier that compares the input and output signals, it is necessary for this stage to be as linear as possible. The most common circuit for this purpose is the *differential pair* as shown in Figure 15.

The differential pair

Most differential pairs are symmetrical circuits with the two transistors (Q1 and Q2 in the circuit here) well matched and the resistance associated with the bases of approximately the same value. Similarly, the values of the collector resistors are usually the same. Ideally, the two devices forming the differential pair would be constructed on the same chip and it is for this reason that some semiconductor manufacturers make differential pairs that simply consist of two matched transistors in the one package. In practice it has been found however, that two good quality transistors can be made to operate effectively as a differential pair for the vast majority of applications. In the circuit of Figure 15, the resistor R_E will determine the emitter/collector current that flows in the two devices, Q1 and Q2. Since these two devices will normally have a dc current gain in the order of at least 200, the base-emitter current is roughly a maximum of 1/200 th of the emitter-collector current. Now the bases of Q1 and Q2 are connected to ground through the resistance of the input signal sources, R_{s1} and R_{s2}. Both Q1 and Q2 are therefore biased on, but in most practical circuits, the voltage drop produced across R_{s1} or R_{s2} by the small value of the base-emitter current will be neglible; seldom more than 50 mV.

The voltage at the bases of Q1 and Q2 will therefore be approximately 0 V (actually, slightly negative). Since the base-emitter voltage drop of the two transistors is around 0.6 V, then the voltage at the top of resistor R_E will be -0.6 V. The current through R_E is therefore

$$I_{RE} = \frac{V - 0.6}{R_E}$$

where I_{RE} is the absolute value of the current flowing in the emitter resistor R_E, and V is the absolute value of the negative supply voltage.

Since the voltage drops across the base-emitter junctions of the two transistors are almost identical, and the voltage drops across R_{s1} and R_{s2} are negligible, then both Q1 and Q2 will share the available current equally. The current in each collector is therefore

$$I_{C1} = I_{C2} = \tfrac{1}{2} I_{RE}$$

The voltage drop across the resistors R_{C1} and R_{C2} is given by

$$v_{C1} = I_{C1} R_{C1} \text{ and } v_{C2} = I_{C2} R_{C2}$$

So the dc voltage present on the two output terminals of the differential pair (i.e: between the two collectors) will be virtually the same.

Now, consider the effect if the input voltage generator e_{i1} causes the voltage on the base of Q1 to increase slightly, while e_{i2} remains fixed. The increased voltage on the base of Q1 will turn Q1 on harder than Q2. In fact, since there is only limited current available through R_E, Q2 will actually be robbed of current by Q1. The collector current I_{C1} will increase, causing the voltage drop across R_{C1} to rise, while the current I_{C2} decreases, causing the voltage drop across R_{C2} to decrease. Since the voltage drop across R_{C1} has increased the output voltage e_{o1}, which is measured with respect to ground potential (0 V), decreases while e_{o2} increases. So an increase in e_{i1} will cause a decrease in e_{o1}, but an increase in e_{o2}. By similar reasoning, an increase in e_{i2} gives rise to a decrease in e_{o2} and a consequent increase in e_{o1}.

This simple analysis of a differential pair has been made using dc signals but the argument is valid for ac waveforms also. Differential pairs are sometimes used with the two outputs as shown in Figure 15, but more often, only one of the output connections is used (i.e: single-ended output). In this case, the input terminal that gives rise to an output signal of the same sense (or phase) as the input signal is called the *non-inverting, or positive, input* while the other input terminal is called the *inverting*, or *negative* input, since the output signal will have the opposite phase to a signal applied to this terminal. This is sometimes called a single-ended differential pair and is often represented in circuit diagrams by the symbol:

This symbol could be used equally validly for the differential pair alone, an IC op-amp or the differential pair, voltage and current stages of a power amplifier. The essential feature is simply the presence of inverting and non-inverting inputs and a single output.

So far we have seen that it is the *difference* between the two base voltages that will give rise to an output. Ideally, if the signal voltages on both inputs are varied identically, then each transistor should still share half the available current and no output should result. Such an input signal is called a *common-mode* input signal. In real differential pairs common-mode signals are still amplified slightly. The ability of the differential pair to reject common-mode signals is called the *common-mode rejection ratio* and is normally given as the ratio of the differential voltage gain to the common-mode voltage gain. i.e:

$$\text{CMRR} = 20 \log \frac{A_d}{A_c}$$

where A_c is the common-mode voltage gain
and A_d is the differential voltage gain

In order to calculate A_c and A_d we first need look at the voltage gains for input signals e_{i1} and e_{i2}. In Figure 15 we will let the output associated with the e_{o2}signal voltage be the differential pair output. Then, the base of Q1 is the non-inverting (+) input and the base of Q2 the inverting (−) input. The signal e_{i1} first suffers attenuation due to R_{s1} and the base resistance of Q1. Furthermore, Q1 is acting as an emitter follower and therefore has a voltage gain of slightly less than unity. Finally, the input signal is fed to the emitter of Q2 which acts as a common-base stage and provides the voltage gain. If we let A_1 be the gain of the non-inverting input, i.e:

$$A_1 \text{ (definition)} = \frac{e_{o2}}{e_{o1}}$$

then it can be shown that:

$$A_1 = \frac{(R_E \parallel R_e)(R_{C2})}{(R_e + R_E \parallel R_e)(R_e)}$$

where A_1 is the voltage gain of the + input
R_E is the value of the emitter resistor
R_{C2} is the value of the collector resistor
R_e is the emitter resistance

The e_{i2} signal fed to the inverting input of the differential pair also suffers attenuation, in this case due to R_{s2}. The signal is then fed directly to the base of Q2. So for signals at the inverting input, Q2 acts as a common emitter amplifier. If we let A_2 be the gain of the inverting input, i.e:

$$A_2 \text{ (definition)} = \frac{e_{o2}}{e_{i2}}$$

$$\text{then } A_2 = -\frac{R_{C2}}{R_e + R_E \parallel R_e}$$

It is obvious at a glance that the expressions for A_2 and A_1 are not the same; it is this difference that causes the common-mode signal to be amplified.

Now, the output signal voltage e_{o2} is really a function of both the common-mode and difference signals.

$$e_{o2} = A_c e_{ic} + A_d e_{id} \quad \ldots\ldots\ldots\ldots (1)$$

where e_{ic} is the common-mode input signal
and e_{id} is the difference input signal

Now, $A_d = \frac{e_{o2}}{e_{id}}$: substituting in (1) gives

$$A_d = \tfrac{1}{2}(A1 - A2)$$

Similarly, $A_c = \frac{e_{o2}}{e_{ic}}$

giving $A_c = A_1 + A_2$

Substituting the equations for A_1 and A_2 into the new equation for A_c gives:

$$A_c = A_1 + A_2$$

$$= \left(\frac{R_c}{R_e + R_E \parallel R_e}\right)\left(\frac{R_e}{R_E + R_e}\right)$$

Similarly, substituting the equations for A_1 and A_2 into the equation for A_d gives:

$$A_d = \tfrac{1}{2}(A_1 - A_2)$$

$$= \tfrac{1}{2}\left(\frac{R_c}{R_e + R_E R_e}\right)\left(\frac{2R_E + R_e}{R_E + R_e}\right)$$

The common-mode rejection ratio is given by:

$$\text{CMRR} = 20 \log \frac{A_d}{A_c}$$

$$= 20 \log \frac{\tfrac{1}{2}\left(\frac{R_c}{R_e + R_E R_e}\right)\left(\frac{2R_E + R_e}{R_E + R_e}\right)}{\left(\frac{R_c}{R_e + R_E \parallel R_e}\right)\left(\frac{R_e}{R_E + R_e}\right)}$$

Thus,

$$\text{CMRR} = 20 \log \frac{(2R_E + R_e)(R_E + R_e)}{2(R_E + R_e)(R_e)}$$

Now, if we assume that R_E is very much larger than R_e, this equation can be simplified to:

$$\text{CMRR} = 20 \log \frac{(2R_E)(R_E)}{2R_E(R_e)}$$

$$= 20 \log {}^{R_E}/_{R_e}$$

This simple equation shows that, in order to ensure a high CMRR it is necessary to make the value of the impedance R_E as high as possible. The problem is that Q1 and Q2 require a certain amount of emitter current to function linearly and with low noise. Remember that the differential pair will normally be used as the input stage in a power amplifier and is therefore handling small signal voltages, so noise generated in this stage will affect the signal-to-noise ratio of the amplifier. Since the negative supply voltage is fixed, and the amount of current required by the input is determined by factors such as noise and distortion, this automatically predicts a value of R_E, and so long as we are restricted to the use of a resistor to determine the emitter current, there is little that can be done to increase the CMRR.

These problems are solved, however, if R_E is replaced with a constant current source as shown in Figure 16.

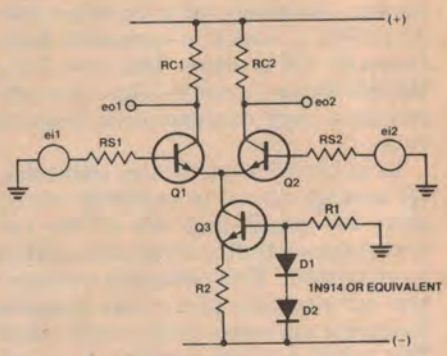


Figure 16

The resistor, R1, acts as a current limit between ground and the negative supply rail via the two diodes, D1 and D2. If the supply rail is around −50 V, for example, a 10k resistor will cause approximately 50/10k = 5 mA to flow through the diodes. The two diodes are turned on and the voltage drop across each of them at this current will be around 0.7 V. The base of Q3 is therefore held 1.4 V above the negative supply voltage (i.e: at −48.6 V.) The base-emitter junction of Q3 will drop roughly 0.6 V, allowing the remaining 0.8 V to be dropped across R2. This voltage across R2 will remain almost constant, regardless of variations in the negative supply voltage. If the negative rail is affected by a heavy transient current, from the output stage of the power amplifier for example, the supply voltage might change momentarily from −50 V to −40 V. The voltage at the base of Q3 will still be 1.4 V above that of the negative supply, so the 0.8 V drop across R2 will remain largely constant. Now we have a fixed voltage ▶

(0.8 V) across a fixed value of resistance (R2) and therefore the current flowing through R2 is fixed also. Since the current flowing in the base-emitter junction of Q3 is negligible in comparison to that flowing in the emitter, most of the current must be supplied by the emitter of the differential pair. That portion of the circuit associated with Q3 is known as a constant current source (or a constant current sink). The operating point of the differential pair is totally determined by the value of R2. Furthermore, since the emitter current is not affected by supply variations, ac mains ripple or signal voltages present on the negative supply rail are not connected to the emitters of the differential pair and a good negative supply rejection results. Now, since Q3 is really operating as a common-base amplifier, the impedance seen by the emitters of the differential pair is the output impedance of a common base amplifier — which is extremely high, typically 1M or more. This now forms the resistance R_E and its high value will ensure a good common-mode rejection ratio.

In practical circuits, the transistors Q1 and Q2 cannot be matched exactly with the result that one of the two transistors will often attempt to conduct more current. This unbalances the pair and increases the generation of second harmonic distortion in the input stage. The solution to the problem is to add resistors in series with the emitters of the differential pair. This, in effect, applies local negative feedback which increases the input impedance of the stage. The voltage gain becomes more independent of the parameters of the input transistors.

This linearises the input stage transfer characteristic and therefore decreases distortion considerably. Differential pairs are sometimes referred to as *transconductance amplifiers* since the output impedance of the stage is relatively high and the input signal voltage is really giving rise to a signal output current. If this current flows through a resistance such as R_{C2} the result is the signal output voltage e_{o2}. Generally however, the output of the differential pair will be loaded down by some degree of capacitance and the output signal voltage will no longer be linearly related to the input signal voltage. The differential pair is really a constant current source, capable of being modulated by the input signal. The rate of change of the output signal current with respect to input signal is called *transconductance* and is given the symbol 'g_m'.

One of the biggest advantages of the addition of emitter resistors to the input stage (sometimes called *emitter degeneration)* is that it allows control over the g_m of the differential pair and will prove invaluable later when considering stability and slewing distortion.

The voltage gain stage

As we saw in the section on feedback amplifiers, it is necessary to have adequate open-loop gain to enable the negative feedback loop to effectively linearise the output transfer characteristic. Since it is the main voltage amplifier stage that is responsible for most of the gain in the amplifier, it is necessary to calculate the required open-loop gain so that the gain of the voltage gain stage can be determined. In order to do this we must look again at the effect of negative feedback on the various paramaters of the amplifier.

In Figure 11, the power amplifier was represented as consisting of a difference amplifier, voltage amplifier and an output stage. All three of these stages can have voltage gains, depending on the particular design. The power amplifier can be represented by a block diagram based on the functions in the power amp, however, rather than the actual circuit. Such a diagram is shown in Figure 17.

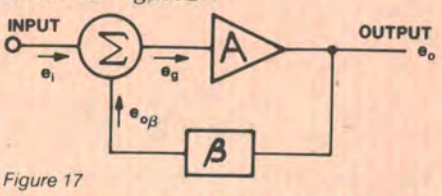


Figure 17
Symbolic representation of a feedback amplifier typical of most power amps.

The symbol 'A' represents the total open loop gain of the amplifier while block 'β' represents the feedback factor or that fraction of the output signal fed back to be summed with the input.

The voltage amplifier stage, A, simply sees an input signal voltage e_g which consists of the sum of the input signal e_i and that amount of the output, e_o, that is returned by the feedback circuit, i.e: $e_o\beta$

Therefore:

$$e_o = A\,e_g$$
$$= A(e_i + \beta\,e_o)$$

thus $e_o\,(1 - \beta\,A) = A e_i$

or $$e_o = \frac{A}{1 - \beta A}\,e_i \qquad \ldots\ldots\ldots\ldots (2)$$

Since this is negative feedback, β is negative, so the equation becomes:

$$e_o = \frac{A}{1 + \beta\,A}\,e_i \qquad \ldots\ldots\ldots\ldots (3)$$

This is now a general feedback equation for the simple feedback amplifier of Figure 17. It gives the overall closed loop gain with respect to the open loop gain A and the feedback factor, β.

The β here should not be confused with the β used to represent the gain of a transistor. In this context, β is a fractional quantity and this convention has been in use since long before the invention of the transistor. The β here is that fraction of the output signal fed back; it is given by:

$$\beta = \frac{R2}{R1 + R2}$$

where R1 and R2 are the resistors forming the negative feedback potential divider in Figure 11.

Equation (3) above therefore becomes:

$$e_o = \frac{A\,e_i}{1 + \left(\frac{R2}{R1 + R2}\right) A}$$

Multiplying both the numerator and the denominator by (R1 + R2) gives:

$$e_o = \frac{A\,(R1 + R2)\,e_i}{(R1 + R2) + AR2}$$

and dividing both through by A gives:

$$e_o = \frac{R1 + R2}{\left(\frac{R1 + R2}{A}\right) + R2} \cdot e_i$$

If we assume that the value of the open loop gain is large in comparison to (R1 + R2), then (R1 x R2)/A will approach zero and the equation approximates to:

$$e_o = \frac{R1 + R2}{R2} \cdot e_i$$

and this is the equation established from the simpler model examined earlier in this discussion. We can see that this is a convenient approximation for the closed loop gain assuming the open loop gain is very high. Notice also that this is equivalent to writing:

$$e_o = \frac{1}{\beta} \cdot e_i$$

or the closed loop gain is approximately $1/\beta$.

It was stated earlier that the effect of the negative feedback was to linearise the transfer characteristic of the amplifier. It does this by decreasing the dependence on the gain of the individual transistors in the amplifier. We are now in a position to justify this statement.

First, consider the effect on the amplifier's closed loop gain by a substantial variation in the open loop gain. Suppose that the amplifier's open loop gain is 10^5, so $A = 10^5$, and let 1/100th of the output signal be fed back to the input by the negative feedback loop. So, $\beta = 10^{-2}$.

Using the general feedback equation, (3), the gain of the amplifier is:

$$\frac{10^5}{1 + 10^{-2}.10^5} = \frac{10^5}{1 + 10^3} = 99.9$$

If the open loop gain is now decreased by a factor of 100, which would be most improbable in a practical power amplifier design, the closed loop gain becomes:

$$\frac{10^3}{1 + 10^{-2}.10^3} = \frac{10^3}{1 + 10} = \frac{10^3}{11} = 90.9$$

The huge variation in the open loop gain has been reduced by negative feedback to a variation of only 10%. The gain of the amplifier is therefore greatly stabilised by the application of negative feedback.

Negative feedback and distortion

Negative feedback will also affect the input and output impedances and the small signal frequency response of the amplifier. It will also reduce distortion generally, and as stated earlier, is one of the few ways to reduce distortion in the output stage.

If a signal, e_i, were applied to the amplifier without negative feedback, the output would be the result of the loop gain, A, and a distortion component, D. If we let e_{oo} be the open loop output signal voltage, then

$$e_{oo} = A\,e_i + D$$

If negative feedback is applied, however, the input signal voltage must be increased to obtain the same output level since the gain has been reduced by the negative feedback. If we let e_{oc} be the output signal voltage with the amplifier operating in closed loop, then e_{oc} will be determined by the closed loop gain (call it a) and a distortion component, d.

$$e_{oc} = a\,e_i + d$$

Now, the closed loop gain is given by:

$$a = \frac{A}{1 + \beta A}$$

$$e_{oc} = \left(\frac{A}{1 + \beta A}\right) e_i + d$$

Now, since the relationship between the open loop output signal and the closed loop output signal is given by:

$$e_{oc} = \frac{e_{oo}}{1 + \beta A}$$

$$\text{then, } \frac{e_{oo}}{1 + \beta A} = \left(\frac{A}{1 + \beta A}\right) e_i + d$$

Substituting for e_{oo} from the equation

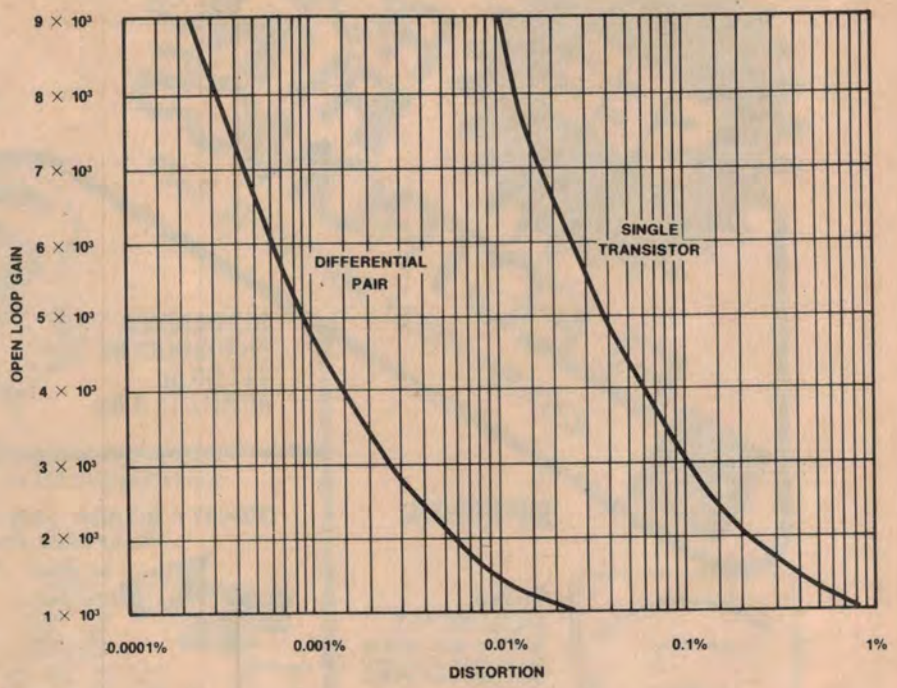


Figure 18

$$e_{oo} = A\,e_i + D$$

$$\text{gives } \frac{A\,e_i + D}{1 + \beta A} = \left(\frac{A}{1 + \beta A}\right) e_i + d$$

$$A\,e_i + D = A\,e_i + d(1 + \beta A)$$

$$\frac{D}{A\,e_i} = \frac{d(1 + \beta A)}{A\,e_i}$$

$$d = \frac{D}{1 + \beta A}$$

where d is the distortion with feedback applied,
D is the distortion, open loop,
β is the feedback factor,
A is the open loop gain.

The distortion generated in the amplifier operated open loop is decreased by a factor of $1/(1 + A\beta)$. So, if with the open loop gain, A, or the feedback factor β are *increased*, the distortion is *decreased*. This does not imply that we should design power amplifiers for maximum open loop gain and rely on negative feedback to reduce distortion since the problem of stability of feedback loops still exists.

If, however, the amplifier is designed with a realistically low open loop distortion, the feedback loop can be used to decrease the remaining distortion to negligible levels while still not using *unnecessary* overall negative feedback.

When designing amplifiers intended, as this project is, for extremely low distortion, it is essential that all stages in the amplifier be designed for as low a distortion as possible. When the negative feedback is applied, truly excellent performance can be expected.

In any practical power amplifier design the bulk of the open loop gain is provided by the main voltage gain stage. The difference amplifier will generally provide some voltage gain, but its main ojbective is to provide a linear difference signal with respect to its two inputs. In some power amps the output stage is operated in a common emitter configuration and therefore provides some voltage gain as well. In the ETI-477 module however, the output stage is a common drain or source follower MOSFET design and consequently has a voltage gain slightly less than unity.

It follows from the discussion of the effect of negative feedback on distortion that this main voltage amplifier must provide a large voltage gain with low distortion and with low phase-shift to minimise stability problems.

An analysis of the distortion characteristics of the differential pair, discussed earlier, reveals that it is significantly better than a single transistor operated in common emitter configuration. If we assume that the distortion in a bipolar transistor is due exclusively to the exponential relationship between collector current and base-emitter voltage, the distortion generated by a differential pair and a single transistor can be calculated by techniques of Fourier analysis. The results of this analysis are plotted in Figure 18 for a differential pair with a 10% mismatch. The superiority of the ▶

differential pair is clearly evident and it is for this reason the differential pair was chosen as a basis for the design of the voltage gain stage in the ETI-477 MOSFET power amp module.

As well as having low distortion itself, a differential voltage amplifier will enable both outputs of the input differential pair to be used, thus giving a balanced output. This overcomes the problem of asymmetrical loading of the input pair by the input impedance of a single-ended voltage amplifier, a problem that would otherwise lead to increased distortion in the first stage.

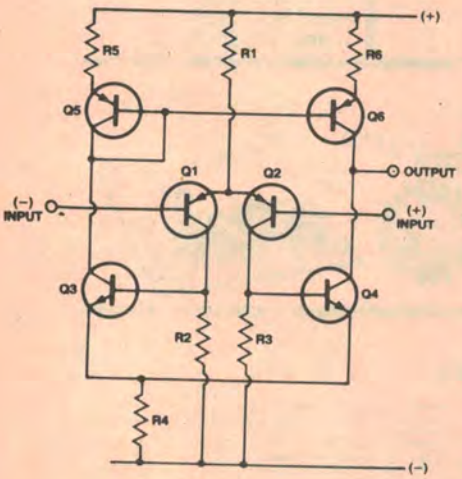


Figure 19

Figure 19 is a circuit diagram of the voltage gain stage developed for this project. The stage is really a double differential pair with a 'current mirror' load. Transistors Q1 and Q2 form the first differential pair with R1 as the common emitter resistor. The output of the Q1, Q2 pair provides a differential drive to Q3 and Q4. The latter pair however, must be converted into a single-ended stage suitable for driving the output stage. This is the job of the current mirror formed by Q5, Q6, R5 and R6. Transistor Q5 has its base-collector junction shorted and therefore acts like a diode, but with the same characteristics as the base-emitter junction of Q6. The bases of Q5 and Q6 are connected together and therefore the voltage on the bases is identical. Since Q5 forms a "mirror image" of the base-emitter junction of Q6, the voltage drop across the two transistors will be almost identical, depending on how well the two transistors are matched. Since the voltage on the bases and the voltage drop across the base-emitter junctions is almost identical, the voltage on the bottoms of R5 and R6 will be almost identical. If these two resistors are made the same value, the current through each resistor, and therefore the current in the collectors of Q3 and Q4, will be identical. This ensures the Q3, Q4 pair will operate symmetrically, even when a single-ended load is attached to the pair.

Furthermore, since the collector of Q3 is connected directly to the base of Q6, the transistors Q6 and Q4 combine to form a push-pull pair with very high gain.

The transistors used in this stage need to be able to handle the full supply voltage and still function with low distortion. They must also be high-speed devices so the overall feedback loop will be fast enough to ensure freedom from transient distortion.

The transistors finally chosen for this stage were the BF469 and BF470. These are a complementary video output pair and as such combine both high V_{ceo} of around 250 V and high speed.

In order to achieve good transient performance when driving the slightly capacitive load of the output stage it is necessary to run a fairly large amount of current through this stage, especially the final differential pair and the associated current mirror. In the 477 there is approximately 16 mA through these transistors, and the average power dissipation is therefore around 0.8 W.

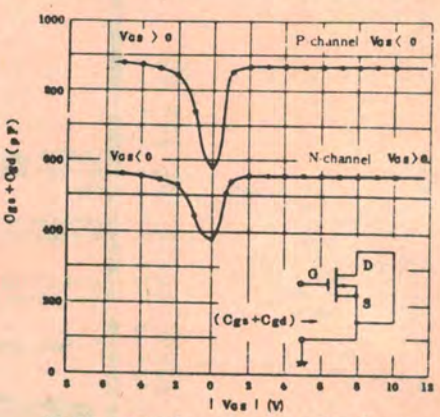
These transistors will run fairly hot, approximately 60°C on the small heatsink shown, but the transistors are well inside their maximum ratings. The result is a voltage amplifier stage of exceptional linearity and very high gain. Coupled with a well-designed input differential amplifier and a good output stage, the phase linearity produced by this voltage stage is excellent, and makes it an easy matter to ensure total stability of the amplifier.

The 477 power module

Since the output of the voltage gain stage has been designed to have sufficiently low output impedance to drive the gates of two MOSFETs in parallel, the output stage consists simply of the MOSFETs themselves. If a preset pot is inserted between the collectors of Q6 and Q4 in the voltage amplifier stage of Figure 19, the voltage across this preset can be used as the bias voltage for the output stage. This is shown in the circuit diagram for the 477 module.

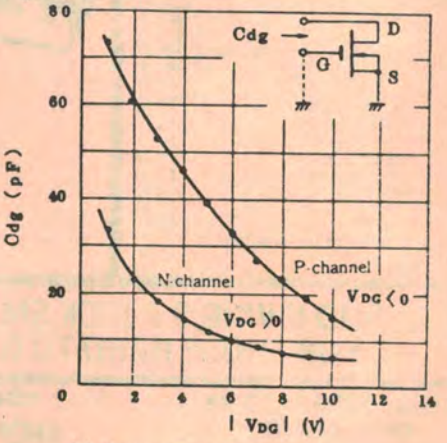
The gates of the output devices are connected to either side of the preset via resistors R21, R22, R23 and R24. As mentioned earlier, these resistors increase the time constant associated with the MOSFET gate capacitance, reducing the frequency response of the output stage slightly but ensuring stability.

A study of the inter-terminal capacitance of these MOSFETs reveals that the characteristics of the N-channel and P-channel devices differ. Figures 20, 21 and 22 show comparison curves between



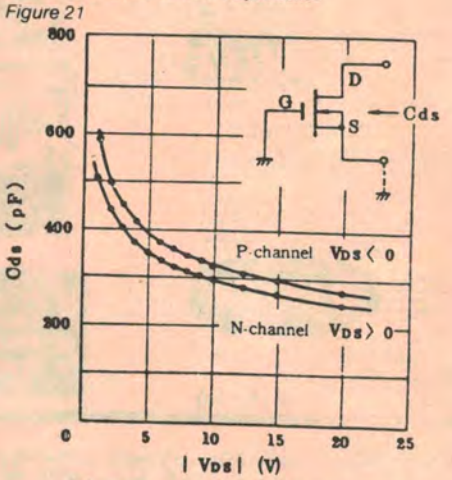
(a) Gate to Source Capacitance + Gate to Drain Capacitance

Figure 20



(b) Drain to Gate Capacitance

Figure 21



(c) Drain to Substrate Capacitance

Figure 22

the N-channel and P-channel MOSFETs used in this project. The important difference is the value of gate-source capacitance for the two devices (Figure 20). If this is not equalised the presence of asymetrical reactance in the output stage makes it almost impossible to ensure stable operation. The only cure is to decrease the open-loop gain of the whole amplifier, so that the negative feedback is reduced, and accept the consequent increase in distortion.

The most common method employed to achieve this is to increase the value of the emitter resistors in the input stage. This reduces the voltage gain of the input stage, at the same time increasing its small-signal bandwidth. Consequently, in a power amplifier employing MOSFETs in the output stage, the relatively small amount of negative feedback available will not be able to linearise the transfer characteristics of the output devices, and the result is an amplifier with only mediocre performance.

The use of resistors in the emitters of transistors generates a local negative feedback effect and will improve nearly every parameter of the transistors. The correct balance between the amount of local and overall negative feedback employed in any particular amplifier design must be established by considering such factors as the distortion generated in the output stage and the speed, gain and linearity of the other stages in the amplifier. Any attempt to put a figure on the 'optimum' ratio of overall to local negative feedback that attempts to be universal for all amplifiers is to me a gross oversimplification.

The problem of the asymetry of the gate-source capacitance is cured by the addition of the capacitors C7 and C8 shown in the 477 circuit diagram. With these capacitors in the circuit and with the 100 R resistors R21, R22, R23 and R24, the only other component required to ensure total stability of the output stage is the power RLC combination formed by R29, C9, R30, L1 and the supply bypass capacitors C10, 11, 12 and 13.

When a square wave, for example, is fed into a purely capacitive load, the output stage will virtually see a short circuit, since the high frequency (>100 kHz) fourier components of the sine wave will see very little impedance in the capacitive load.

The inductor L1 ensures that this does not happen by inserting a reactance that increases at high frequencies. The resistor R30 is placed in parallel with the inductance so the top end frequency response of the amplifier is not unduly affected.

This inductor is made by winding 20 turns of 0.8 mm (20swg) enamel-covered copper wire around a plastic bobbin normally supplied for use with potcores. The bobbin in the prototype modules has a 12 mm outside diameter and is 10 mm long; winding two layers of ten turns gives the desired value of inductance around 5 uH.

The other two components of this network, R29 and C9, ensure that the amplifier always has a load at high frequencies. Without this 4.7 R load the gain of the output stage is slightly greater than unity, due to the presence of positive feedback caused by the effective capacitance around the output devices, and this causes oscillation.

The 220 n capacitor is necessary since the resistor must be removed from the circuit for frequencies inside the audio passband or the high power dissipation in the resistor would destroy it instantly. You should expect this resistor to get hot when testing the amplifier with full power square waves or high frequency sine waves, but this condition will not occur under normal operation.

Resistors R25, R26, R27 and R28 provide slight emitter degeneration to the output devices. This helps to linearise the output transfer characteristic of the amplifier and thereby assists in ensuring stability of the output stage.

In bipolar designs where output transistors are used in parallel these resistors are essential to make the parallel devices share the load current equally. In a MOSFET design, however, this is only of secondary importance, since the negative temperature coefficient will increase the impedance of any output device that conducts more than its share of local current.

The final components needed to ensure stability of the output stage are the supply bypass capacitors C10, C11, C12 and C13. Capacitors C12 and C13 are 100 uF electrolytics that provide general supply bypassing to frequencies inside the audio passband, but have little effect at 1 MHz, where the MOSFET would tend to oscillate.

For this reason capacitors C10 and C11 have been included also. These capacitors must be positioned very near the output devices, since the resistance of only several centimetres of p.c. board track will greatly decrease their effectiveness.

In the 477 these capacitors are mounted on the rear of the circuit board with one lead soldered directly to the drains of the output devices.

The gate resistors R21, R22, R23 and R24 and the gate power capacitors C7 and C8 are also mounted on the rear of the circuit board, again soldered directly to the MOSFETs.

Incidentally, if you are experimenting with MOSFET circuits a few fundamental precautions with layout will save many headaches. The length of wire soldered to the gate of the MOSFET is critical. Hitachi quote 50 mm as the maximum length of wiring that can be safely connected to the gate, and in many applications even this is too long.

This is the reason the 477 pc board was designed so the power transistors solder directly on to the board rather than adopting the approach of mounting the output devices on the heatsink and running flying leads between the board and the MOSFETs. Certainly wherever flying leads are used the gate resistors should be soldered directly to the gate of the MOSFET with as little wire left on the gate side of the resistor as possible. The gate wiring can be soldered between the p.c. board and the other side of the gate resistor. You may never experience this problem with flying leads, but this is a simple and effective precaution that is worth regarding as a fundamental design rule when working with MOSFETs.

The remaining components in the output stage are the zener diodes ZD1 and ZD2 and their associated diodes D3 and D4, and the bias preset RV1. It was mentioned earlier that the maximum gate to source voltage of these MOSFETs is 14 V. If this voltage is exceeded the MOSFET can be destroyed, so the zeners and diodes are placed between the gate and the output of the power amp to prevent the drive voltage ever becoming more than 12.6 V above or below the output voltage.

This condition would mainly occur when the output is driving a short circuit or a capacitance load big enough to look like a short circuit. Under these conditions the output voltage cannot deviate much from 0 V since it is shorted to 0 V, and the negative feedback loop will drive the output of the voltage gain stage into clipping in an attempt to compensate for the error.

The gate to source voltage is now around ±50 V, well above the absolute maximum voltage for the output devices. The diodes D3 and D4 are necessary to prevent the zeners from shorting out the gate drive under normal operating conditions.

The current flowing through the preset RV1 will give rise to a voltage drop across the preset that can be varied ▶

by adjusting RV1; this acts as the bias voltage for the output devices. If the diodes D3 and D4 are not present, the gates of Q10 and Q12 for example can never go more than 0.6 V above the output voltage, due to the 0.6 V forward voltage drop of the ZD2. Since the voltage drop across RV1 is around 1 V, the drive voltage to the gates of Q9 and Q11 can never go higher than the sum of these two voltages, i.e: 1.6 V, above the output voltage, and this limits drive to the MOSFET. The same occurs to negative-going signals due to the 0.6 V forward turn on voltage of ZD1.

The combination of all these techniques yields an output stage that is totally free of instability and with a bandwidth of a round 5 MHz! Furthermore, the transfer characteristics and phase response of the output stage are predictable, making it relatively easy to ensure stability of the overall feedback loop.

The voltage amplifier of the 477 module is of the type shown in Figure 19 and is formed by transistors Q3 through to Q8 and the associated passive components.

The only components not discussed earlier are R31 and C14 (477 circuit diagram) that make up a series RC network. This applies local negative feedback around the voltage amplifier output stage by decreasing the impedance between the collector and the base of Q6.

Remember that the signal on the base, is πrads out of phase with that on the collector of a transistor operated as this one is, in common emitter. The effect of this negative feedback is to decrease the open loop gain for frequencies well above the audio passband.

The input differential pair is formed by Q1 and Q2, with R10 and R13 supplying emitter degeneration.

Q3, R8, R12 and diodes D1 and D2 form the constant current source for the input pair and maintain the current at around 240 uA. This relatively low amount of emitter current was chosen specifically to ensure a good noise figure in the first stage.

The capacitor C4 decreases the impedance between the two inputs of the voltage amplifier stage i.e: the bases of Q3 and Q4) and therefore decreases the gain of the differential pair at high frequencies. This is the main phase compensation in the amplifier and is often referred to as phase lag compensation.

The resistors R19 and R16 form the negative feedback potential divider and therefore determine the closed loop voltage gain of the power module.

The 100 uF electrolytic capacitor C5 has the effect of increasing the impedance between the base of Q2 and ground for frequencies below the audio passband.

Theoretically the resistance through C5 at dc is infinite, which increases the negative feedback, thereby decreasing the closed loop gain to unity. This ensures that any dc voltage occurring on the output of the amplifier is connected directly to the base of Q2, where it can be compared to the dc voltage present on the base of Q1. Since the base of Q1 is connected to ground via the series combination of resistors R2, R4 and R5, the voltage drop across these resistors will be determined by the base-emitter current and this resistance. Since the emitter collector current in Q1 is around 120 uA and given that the h_{FE} of Q1 is around 250, the base emitter current will be roughly

$$\frac{120\ \text{uA}}{250} \doteq 0.5\ \text{uA}.$$

So the voltage on the base of Q1 will be approx.

$$0.5\ \text{uA}(47\ \text{k} + 4\text{k}7 + 1\ \text{k}) =$$
$$0.5\ \text{uA} \times 52.7\ \text{k} = 25.3\ \text{mV}.$$

The voltages and currents shown on the circuit diagram were obtained by measurement of the prototype modules, and as shown the voltage on the base of Q1 was −25 mV, in good agreement with the calculated value. If the differential pair and the negative feedback loop are operating correctly the dc voltage on the output should be almost identical to this voltage.

We saw earlier that the problem of transient intermodulation distortion is eliminated by limiting the maximum signal slope of the input signal to something less than the slew rate of the amplifier. In the 477 module this is accomplished by a 12 dB/octave passive low pass filter formed by R4, C2 and R5, C3. Both sections have similar cut-off frequencies, but the value of the resistor R5 has been increased to reduce the loading effect it would otherwise have on R4. The value of C3 has been reduced accordingly so that within the limits of component tolerance the 3 dB point remains the same as the first stage.

The two-section filter was used, since it is possible to limit the maximum signal slope of the input to a greater extent than with the single-section filter, while still keeping response within the audio passband flat. The attenuation of the filter at 20 kHz is only 0.2 dB. Adding another 0.2 dB at 20 kHz due to the passive output filter L1, R30 gives the final frequency response figure of 0.4 dB down at 20 kHz. Both the frequency response and the slew rate of the amplifier are determined by the passive components eliminating the problem of transient intermodulation distortion.

The low frequency response of the amp should also be controlled by a passive filter on the input. In this case it is a high pass filter formed by C1 and R2. Since the amplifier is entirely dc coupled after the input capacitor C1, it would have a frequency response that extends to dc, provided the 100 μF electrolytic C5 was removed from the circuit. Since it is desirable to include C5 for the reasons mentioned earlier, it is necessary to prevent the voltage across it from becoming too great.

Remember that if the amplifier were fed by a subsonic frequency the impedance of C5 would be high and it would therefore drop nearly the full supply voltage across it. Furthermore, it is not desirable to have these large voltage swings coupled directly to the differential pair. For this reason the practice of allowing this capacitor and its associated resistor (R16 in this case) to define the low end characteristics of the amplifier is a dangerous one.

This problem is easily overcome by including a high pass filter at the input of the power amp with a higher 3 dB point than that of C5R16, and this is the function of C1 and R2. The 3 dB point of the input low end filter (C1, R2) is:

$$f = \frac{1}{2\pi R2\ C1} = \frac{1}{2\pi(0.47 \times 10^{-6})(47 \times 10^{3})} \doteq 7\text{Hz}$$

while for the negative feedback RC (C5,R16):

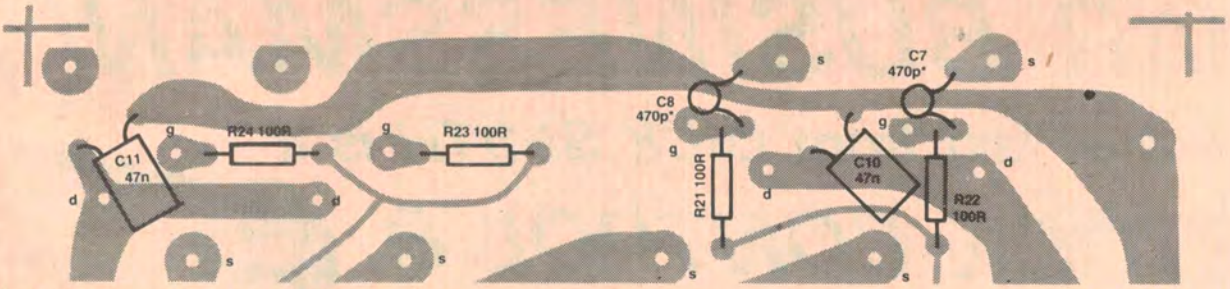
$$f = \frac{1}{2\pi R16\ C5} = \frac{1}{2\pi(10^{3})(100 \times 10^{-6})} \doteq 1.6\ \text{Hz}$$

It is clear that the input filter will determine the low frequency characteristic of the amplifier.

The resistor R1 is included in the design simply to make certain that C1 does not become charged by dc. If this is allowed to occur the result is a loud crack through the loudspeakers if the input RCA sockets are plugged or unplugged while the power amp is on.

Construction Part 2

In construction last month we gave all the necessary details for assembly of the pc board itself. The heatsink bracket shown was a 152 mm length of 40 mm x 12 mm x 3 mm thick aluminium angle extrusion. This extrusion is entirely satisfactory for hi-fi use ▶

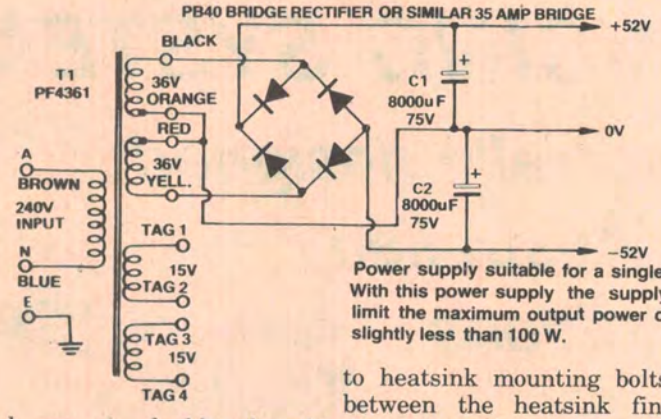


when bolted to an adequate extruded aluminium heatsink. If you intend the module for use in sound reinforcement applications, however, where the average operating levels could be near the clipping point for extended periods of time, two 152 mm lenths should be used back to back to decrease the thermal resistance.

In order for these heatsink brackets to work effectively it is important that there is good contact between the heatsink bracket and the heatsink itself. Use some heatsinking paste between these two surfaces and bolt them together firmly. In the Series 5000 power amplifier (next month) we will be using a cast aluminium front panel heatsink that we have designed and are having manufactured. The front panels will be available from us directly and also from a number of parts suppliers.

In order to ensure good thermal contact with the back of this panel it is necessary to use a 40 mm x 40 mm x 3 mm thick extrusion. Since two modules are required for the stereo amplifier the heatsink bracket can be constructed as a double length (305 mm) bracket, as shown in the photograph with this article. Alternatively two independent modules can be bolted to the rear of the front panel, but the 40 mm x 40 mm extrusion should be used.

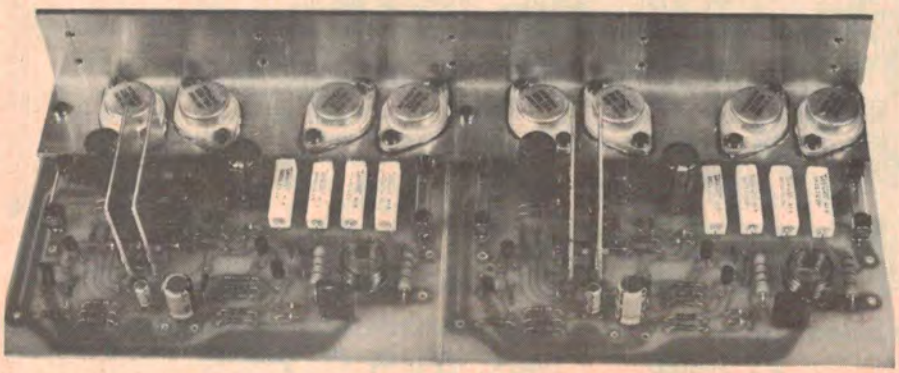
Drilling details for the heatsink brackets are given this month so that the construction of the pc boards for the Series 5000 amp can be finished this month, if desired. The heatsink bracket to heatsink mounting bolts must fit between the heatsink fins, so the dimensions shown are critical. If you elect to use two independent heatsink brackets you will need to work out the drilling details from the front panel heatsink. ●



Power supply suitable for a single 477 module. With this power supply the supply voltage will limit the maximum output power of the 477 to slightly less than 100 W.

NEXT MONTH: we complete the series of articles, describing construction of the Series 5000 Stereo Amplifier with details on the measured and subjective performance.

To house our Series 5000 stereo amp we have designed and are having manufactured this cast aluminium heatsink/front panel. It will mount in a standard 19-inch rack or be used as a stand-alone unit with the cabinet panels fitted.



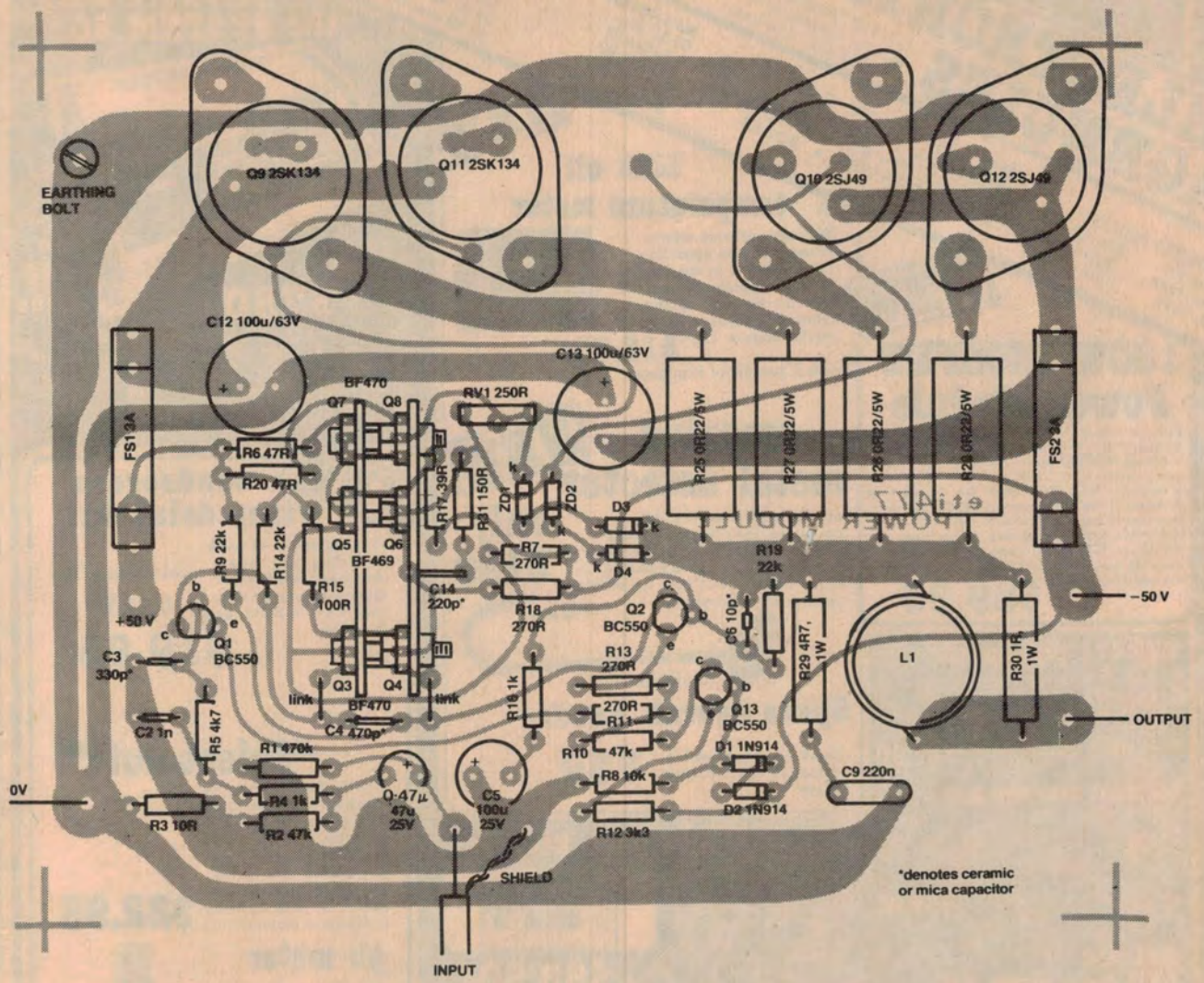
Two modules mounted on the dual bracket, details for which are given right.

ERRATA TO PART 1

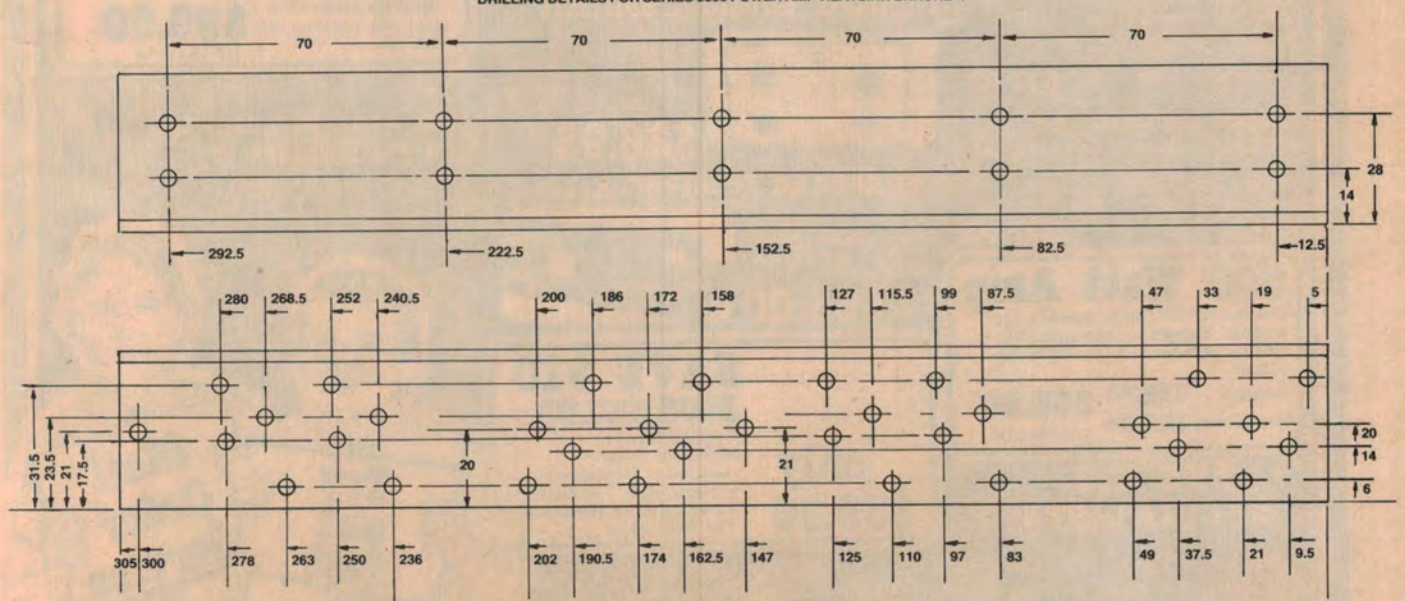
Unfortunately the value of C1 was shown incorrectly last month in the parts list and on the circuit diagram as a 47 uF 25 V electrolytic. The correct value is 0.47 uF 25 V. This capacitor is part of an input RC filter that defines the low end roll-off of the amplifier. The incorrect value of C1 will move the 3 dB point of this filter down to around 0.1 Hz, where it is completely ineffective, but it will not affect any other specification of the amplifier. Since it is important for the reasons discussed elsewhere in this article that the 3 dB point is defined at the input, the correct capacitor should be fitted.

The transistor Q13 on last month's overlay photograph has its base and collector leads shown inverted. The correct orientation for this transistor is as shown in this month's overlay, i.e: with its flat side pointing towards the resistors R13 and R10.

The capacitors C7 and C8 were shown incorrectly last month to be connected between the gates of MOSFETs Q9, Q11 and the output side of the emitter resistors R25, R27. These capacitors actually connect between the gates of MOSFETs Q9, Q11 and their respective sources. The circuit is shown correctly this month.



DRILLING DETAILS FOR SERIES 5000 POWER AMP-HEATSINK BRACKET.



ALL THESE HOLES DRILLED FOR 6 BA CLEARANCE