6.6 Audio Amplifiers

6.6.1 The Autobias Amplifier: A New (AC Coupled) Topology for Automatically Biased Audio Amplifiers Using Power MOSFETs (TA82-1)

Abstract

An obstacle blocking wide acceptance of power MOSFETs in audio amplifiers is the lack of an automatic bias technique. A unique circuit topology senses and maintains quiescent current despite the half-wave pulses inherent in class AB operation. Performance of the circuit, consisting of little more than a differential amplifier driving a totem pole output, rivals that of more complex circuits.

Introduction

MOSPOWER FETs offer a number of significant improvements in the characteristics of interest for amplifiers as compared to their bipolar counterparts, namely:

1. MOSPOWER transistors are comparatively immune to second breakdown because no transverse current flow exists, as in a bipolar, to cause current concentrations. Therefore, no complex power limiting or protection circuitry is needed.
2. The temperature coefficient of transconductance is negative. Consequently, design of thermally stable circuits is easy and devices may be readily used in parallel for increased output current.
3. The transfer curve (I_D vs. V_{GS}) is linear over most of the operating current range of the transistor which produces a low distortion output. Furthermore, the curvature which is present adheres approximately to a squarelaw, so that the resulting even-order products may be cancelled by a push-pull connection.
4. The capacitances are low which allows high frequency open-loop response. Also, FETs do not exhibit minority carrier storage time since conduction is solely by majority carriers. Consequently it is simple to build amplifiers which do not exhibit the various forms of transient distortions.

The chief problem in using MOSPOWER is providing the proper biasing. The average gate voltage must be held a few volts positive with respect to the source, depending upon the current desired and the characteristics of the transistor, especially the threshold voltage. Unfortunately, threshold voltage not only shows a dependence upon temperature (approximately 6mV/ °C), but is subject to lot-to-lot variations. Consequently, some kind of feedback scheme must be used to maintain the idle current despite variations on the order of 2 volts in the required gate voltage. The unresolved problem to date is how to sense the output idle current in the presence of the high current half-wave pulses which occur under class AB operation. The solution of this problem is the subject of this article.

The Auto Bias Scheme

The method discovered which accomplishes biasing is shown in Figure 1. In this scheme, the bias idle current is maintained by comparing the voltage obtained from the current sense resistor to a reference level. When the signal is large enough to cause cut-off of the current on negative half-cycles, thereby producing an asymmetrical waveform, the peak clipper and filter produce a voltage which is substantially the same as the zero signal level, regardless of the amplitude of the peak current. For proper operation, the DC level caused by the idle current must be set to one-half the level of the peak output from the clipper as shown in Figure 2. Note that the current waveform of Part A has an average level proportional to the peak current while the output from the clipper remains essentially constant as shown on B. Proof that this scheme really works will be given with the data obtained from the practical designs.

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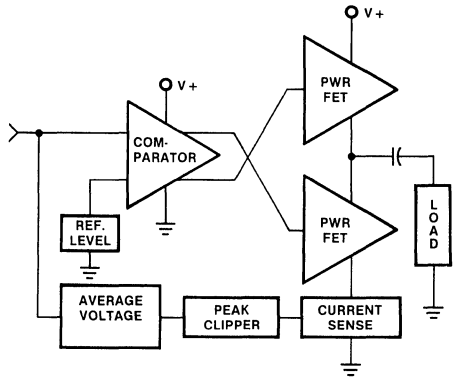
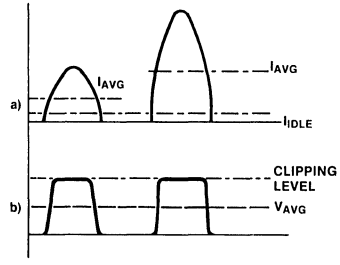


Automatically Biasing (Autobias) Scheme for Single Supply Class AB Amplifiers
Figure 1



Waveform of a) One Output Transistor Current and b) the Clipper Output. The Varying Average Level of the Current Wave Causes Negligible Shift in the Average Level of the Clipper.
Figure 2

General Description of Amplifier Topology

The objective of this project was to produce a simple circuit which would fully utilize the advantages of MOSFETs and not require any adjustments. Consequently, a direct coupled scheme using complementary devices, so much in vogue with bipolar amplifiers, was rejected as being too complex, especially when a second differential amplifier to control the quiescent current would have to be added. In addition, *p*-channel FETs suffer from the severe disadvantage that holes are lower mobility carriers than electrons. The practical result is that to produce a *p*-channel FET with gain equivalent to a given *n*-channel FET, the die area must be about twice as large, causing a corresponding increase in capacitances and higher cost. The topology chosen is a direct implementation of the block diagram shown in Figure 1. As shown in Figure 3, the circuit using npn transistors and *n*-channel FETs consists of a differential amplifier driving a push-pull totem pole output configuration. The diff-amp controls the bias current of Q_4 which acts as a current source for Q_3. This arrangement necessitates AC coupling to the load even if a split supply were used because the voltage at the drain of Q_4 is affected by several component values.

Bias is accomplished by comparing the voltage drop across R_{21} to the voltage from the reference diode, D_1. To achieve accuracy in setting the bias, the DC resistance in the base circuits of Q_1 and Q_2 must be equal (i.e., R_{10} in parallel with $R_{11} = R_2 + R_{16} + R_{17}$ and the h_{FE} of Q_1 and Q_2 should be matched). Matching of V_{BE} is not important because of the drops across R_3 and R_4 and the base circuit resistance. Should the current in Q_4 tend to increase, the resulting drop across R_{21} coupled to Q_1 lowers its collector voltage (V_{C1}) which is coupled through R_6 to the gate of Q_4, thereby holding the current of Q_4 nearly constant.

Under large signal conditions, the high current peaks must be clipped and the waveform filtered. The best place to clip is right across R_{21}. Diode D_3 performs this function and also provides dynamic bypassing. In this location, power output is maximized, as the total voltage loss across the diode is only about a volt. Total harmonic distortion also is less with the diode in this position; apparently the decreasing diode incremental resistance with increasing current compensates for a nonlinearity in the MOSPOWER FET. The diode introduces a generous number of low level high order harmonics, but a considerable reduction of the second and third harmonics occurs. R_{18} and R_{20} often can be chosen to achieve a minimum in the total harmonic distortion; their value determines the composition of harmonic content. R_{18}, R_{19} and D_2 balance both halves of the push-pull stage. At low signal levels, particularly when Q_3 and Q_4 are not well matched, R_{19} and R_{21} cause a reduction in even-order distortion products. The resistor R_{17} and diode D_4 form a second stage clipper which keeps the peak output quite constant regardless of the audio signal level across R_{21}. R_{16} and C_5 form a low pass filter to prevent the clipped waveform from being mixed with the input audio which is also applied to the base of Q_1. Distortion increases considerably if C_5 is eliminated.

To provide maximum power output from a given supply, the do level at the drain of Q_4 (V_{D4}) must be one-half of the power supply voltage (V_A) at full signal output. This level is controlled by the divider composed of R_{13}, R_8 and R_9. The level V_{D4} is thus determined by the fixed level placed on the gate of Q_3 minus the V_{GS} drop of Q_3, which usually is consistent within two volts from a given MOSPOWER production line.

The differential amplifier acts as a voltage comparator to maintain the DC bias level and as a phase splitter to drive the MOSFET output transistors. The interstage circuits are somewhat unusual. The load for Q_2 is R_7, but the signal from Q_2 must be referenced to the source of Q_3 since it is driven as a common source amplifier. This is accomplished by the bootstrap circuit R_{13} and C_4. To maximize R_7 for higher gain, R_{13} must be small, on the order of 1 KΩ; this requires C_4 to be about 400μF for satisfactory low frequency response.

Note that the divider composed of R_8 and R_9 is also bootstrapped by C_4 and R_{13} to provide benefits which are not generally obvious. The distortion is reduced slightly, but of more importance is the reduction of the turn-on current surge caused by charging the output coupling capacitor C_8. The time constant of R_{13} and C_4 determines the surge magnitude and duration.

The load resistors for Q_1 and Q_2 are R_5 and R_7, which should be matched for the lowest distortion. The DC level at the collector of Q_1 is dropped by R_6 to the appropriate level at the Q_4 gate. Since current through R_6 is supplied by a low valued constant current source, negligible loss in DC gain occurs through the coupling network. However, capacitor C_2 is needed to prevent high frequency rolloff caused by the time constant composed of the input capacitance of the MOSPOWER FET and R_6.

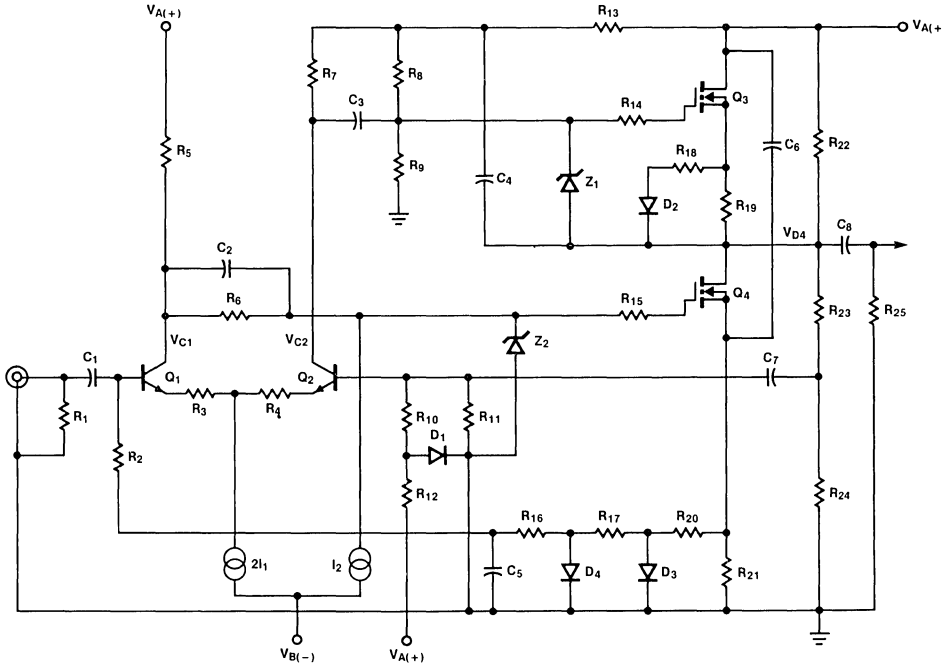
A feedback signal is developed by the R_{23}-R_{24} divider and applied to the base of Q_2 via C_7. Resistor R_{22} works with R_{23} and R_{24} to set the voltage V_{D4} to half of V_A during troubleshooting and these resistors also perform the function of a bleeder for the power supply filter capacitor. Resistor R_{25} insures that the output coupling electrolytic (C_8) has a charging current path should the amplifier be turned on with speakers disconnected. Feedback could be taken from a tap on R_{25}; this lowers distortion at low frequencies but overload recovery is poorer.

Since MOSPOWER is not plagued by second breakdown, involved overload protection circuits are not required. However, gain does not decrease with operating current, so enormous output current could be developed into a short circuit load. To prevent this, the zener diodes Z_1 and Z_2 are used to prevent excessive gate drive. Although one diode per gate will limit the peak current, in some cases the circuit can cope better with large input signal overloads if two diodes are used in series. They should be chosen to allow equal positive and negative swings about the nominal idle gate voltage.

Since most MOSPOWER devices have a cut-off frequency in the giga-cycle range, parasitic RF oscillations can be troublesome. Most assemblies require an RF bypass C_6, on the order of 0.22 μF, physically connected as shown. In addition, R_{14} and R_{15} (100Ω or so) are included as parasitic suppressors. Ferrite beads could be used in place of the resistors. In either case, the suppressors should be mounted closely to the gate terminal. In addition, leads running to the gate terminal should be either shielded or used as a twisted pair with a ground lead.

Design Criteria

In the simple circuit of Figure 3, primary tradeoffs occur between output slew rate, input impedance, matching requirements and bias point accuracy. For example, with a given pair



Basic Autobias Circuit
Figure 3

of output transistors an increase of slew rate requires that the current in the diff-amp increases. The higher currents through the resistors in the base circuits of Q_1 and Q_2 produce larger voltage drops with a greater likelihood of an error in the output idle current unless the h_{FE} matching between Q_1 and Q_2 is tightened or the values of the resistors in the base circuit are proportionally reduced. If the resistors are reduced, then to preserve the low frequency response, capacitors, C_1, C_5 and C_7 must increase at an added cost which becomes significant if values over 1 μF are necessary, since it is desirable to avoid electrolytics.

The values of the components in the bias feedback loop from R_{21} to the base of Q_1 should be proportioned in a particular manner, since both bias and audio signals are present at the Q_1 base. A large signal which overloads the diff-amp disturbs the idle current setting. Best recovery was empirically determined to occur when the capacitor values for C_1, C_7 and C_5 are equal and R_2 is at least three times R_{16}. If C_5 is made proportionally larger, the point where low frequency distortion starts to increase can be made lower; however, the idle current recovery waveform begins to assume the character of a damped oscillation.

In order to prevent a significant portion of the DC level on C_5 from biasing the diode D_4, R_{16} should be at least twenty times R_{17}. R_{17} is chosen so that the clipped output voltage from D_3 sends a current through D_4 such that the peak level from D_4 equals twice the open circuit level at the base of Q_2. R_{17} should be large enough such that the peak level across D_4 is essentially constant regardless of the amount of current flowing through R_{21} and should produce the same current in D_4 as is flowing in D_1 when D_1 and D_4 are the same type diode.

Resistors R_3 and R_4 used in series with the emitters of Q_1 and Q_2 provide two benefits. The DC drops across them lessens the V_{BE} match required between Q_1 and Q_2. In addition, since the diff-amp will normally operate slightly out of balance, these resistors tend to balance the gain through both sides of the diff-amp. Choosing them to be about twice the junction incremental resistance (25 Ω/I_E(mA)) has yielded satisfactory results.

Because the load resistor for Q_2 is bootstrapped, the signal swing at the collector of Q_2 with respect to ground slightly exceeds the output peak-to-peak level which is close to the power rail voltage. Therefore, the quiescent level of the voltage V_{C2} must be above one half of the rail by at least 3 volts to avoid signal clipping or nonlinearity of the peak negative signal. Another 2 or 3 volts should be allowed for diff-amp unbalance. These requirements force the maximum value for $R_{13}+R_7$ to be $((V_A/2)-6)/I_1$, assuming that the current drawn by the R_8, R_9 divider is negligible. To maximize gain and prevent diff-amp current fluctuations from significantly influencing the voltage at the gate of Q_3, R_{13} should be small compared to R_7; however, the smaller R_{13} becomes, the larger C_4 must become in order to have adequate low frequency response and satisfactorily limit the turn-on current surge as C_8 charges.

R_5 must equal R_7 to keep the diff-amp in balance electrically. For thermal balance V_{C1} should equal V_{C2} by satisfying the equation $(I_1+I_2)R_5=I_1(R_7+R_{13})$. R_6 is chosen to place the proper gate voltage on Q_4 by consulting typical data for the particular MOSFET being used.

The correct value for V_{G4} depends on the idle current required to minimize crossover distortion from the MOSFET. This is empirically determined and must be about 300 mA for the transistors used in the designs shown later. Using ordinary silicon diodes for the clippers yields a clipping level of 0.6 to 0.7 volts depending upon the diode characteristics. This dictates that the reference level on the base of Q_2 should be from .3 to .35 volts. If $R_{10}=R_{11}$ and D_1 and D_4 are the same type and operated at the same current, these requirements are met and a 1Ω resistor for R_{21} will set the idle level between 300 and 350 mA. To preserve the balance of the push-pull output, R_{19} must equal R_{21} and correspondingly, $R_{18}=R_{20}$ and $D_2=D_3$.

The value for R_{20} and R_{18} is empirically determined. If R_{20} is greater than twenty times R_{21}, its effect on distortion and power output is negligible; the output spectrum will be relatively free of high order harmonics but maximum power output will not be achieved. As R_{20} approaches the value of R_{21}, the "dynamic bypass" action becomes noticeable, power output increases and a marked reduction in 2nd and 3rd harmonics occurs. This results in a decrease of total harmonic distortion, but the output spectrum will have minute amounts of high order harmonics. The optimum value depends upon the MOSFET characteristics as well as that of the bypass diode. A search for the optimum point is best done by operating the amplifier open loop, i.e. R_{24} shorted, and monitoring the output with a spectrum analyzer. The most acceptable spectrum is usually obtained with an R_{20} value slightly on the high side of that which yields the lowest THD.

The remaining network to be designed is that of the divider R_8 and R_9. It sets the output level V_{D4}. For symmetrical clipping, which yields maximum power output, the voltage at the gate must equal one-half the supply voltage at maximum power output plus the nominal gate to source drop of the power MOSFET and the drop across the source circuit network. The resistances can be in the megohm range, as the FET gate is essentially an open circuit. The value of C_3 is chosen to have negligible phase shift in the frequency range of interest. Overly large values for C_2 and C_3, however, improve overload behavior when the zener diodes conduct due to excessively large low frequency signals.

Practical Applications

During the development of the autobias scheme, two practical amplifiers were designed. The first is a 25 watt version intended for home high-fidelity use, and the second is a 50 watt design of lesser power bandwidth intended for public address use.

A 25 Watt Design

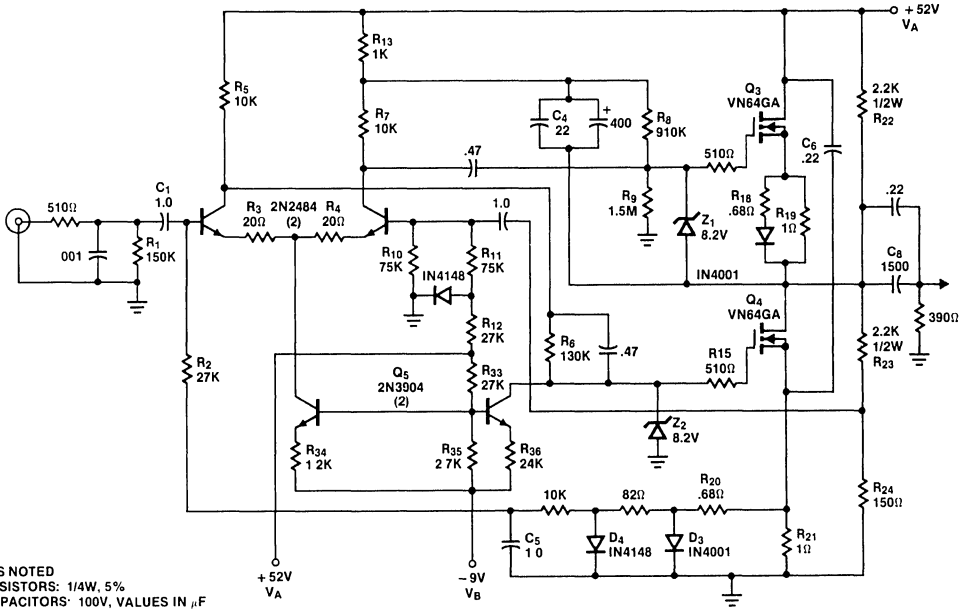
Figure 4 shows a practical 25 watt amplifier. Transistors are used for the current sources shown in Figure 3. Base drive for these transistors is derived from the main power supply V_A, so that their collector current is proportional to the rail voltage. This feature holds the voltages on the diff-amp collectors close to $V_A/2$. The sensitivity of I_Q to V_A is about 3.4 mA/volt when V_B is held constant; the sensitivity of I_Q to V_B is -15 mA/volt when V_A is held constant. In a practical amplifier with a non-regulated supply, variations in power output will cause fluctuations in V_A, but will not affect V_B; therefore, having I_Q increase slightly with power output as discussed later will tend to compensate for the 3.4 mA/volt I_Q/V_A sensitivity. In the case of line voltage variations, since V_A is about five times V_B, the sensitivities tend to cancel, leaving a net sensitivity of about 2 mA/volt.

The circuit arrangement causes ripple cancellation to take place. Ripple from V_A is applied via R_5 and R_6 to the gate of Q_4. An out of phase ripple component is also applied to the gate via the current source Q_6. By properly proportioning the filter components of the supplies V_A and V_B, output ripple can be reduced to a level acceptable for most applications without the use of unduly large capacitors or an extra filter section connected between R_5 and V_A. The bootstrap capacitor (C_4) effectively filters the ripple from the gate of Q_3. The filter for V_A should be at least 5000 μF.

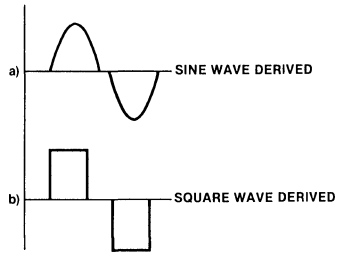
The sensitivity of the MOSFET quiescent current, I_Q, to threshold voltage ($V_{GS(TH)}$) depends upon the loop gain of the bias stabilization portion of the circuit. With the components used in Figure 4, the sensitivity is about 16 mA/volt, which is felt to be satisfactory to accommodate the typical 2 volt tolerance of a MOSPOWER production line.

It is not possible to measure the change in idle current level as the power output from the amplifier is varied using the usual sine wave test signal because the idle level is obscured by the output current. However, waveforms similar to the ones shown on Figure 5 can be fed into the amplifier; by viewing the voltage across R_{21} during the time of the zero level step, the idle level is visible. It is found that a fairly precise setting of the voltage across R_{21} is necessary if the idle level is to remain invariant with power output changes.

An increase of idle level with power output is a result of the average voltage output from the clipper and filter decreasing with signal level. The decrease results in the diff-amp raising the gate voltage to compensate for this apparent decrease in idle level. A small amount of this behavior is desirable in that it compensates for the decrease in idle level experienced as the supply voltage, V_A, drops due to increased audio power output. Should the clipper output increase with power output, the circuit will reduce the idle current level. This situation yields improved power efficiency, but the output may show evidence of cross over distortion at the higher power levels. For optimum performance, it is therefore necessary that the clipping level be maintained at slightly below twice the zero signal idle voltage from the clipper, regardless of the power output from the amplifier. The two stage clipper used is necessary to reasonably achieve this goal.



Practical 25 Watt Autobias
Figure 4



Test Waveforms Used to Observe Idle Level Under Large Signal Conditions
Figure 5

Identical tests were run on an amplifier at ambient temperatures of 25 °C and 45 °C. The current at all power levels dropped about 22 mA at 45 °C, a predictable result because the reference diode, D_1, has a temperature coefficient of 2 mV/°C, which is divided in two by the resistors R_{10} and R_{11}. Distortion as a function of power output remained essentially unchanged at the test frequencies of 75 Hz, 1 kHz, and 5 kHz.

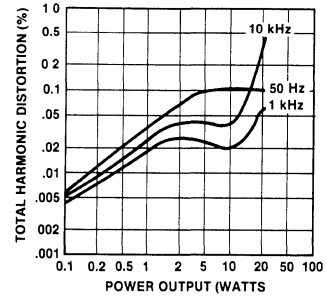
Figure 6 shows total harmonic distortion at selected frequencies as a function of power output and Figure 7 shows distortion at 1.0, 10 and 25 watts as a function of frequency. In the important mid-range, THD is under 0.1%. The increase in THD at high frequencies is caused by the extra drive required of the diff-amp to handle the MOSFET input capacitance, while the increase at low frequencies is caused somewhat by the coupling capacitors, primarily the output capacitor (C_8), but mostly is attributed to the bootstrap capacitor (C_4), and the bias filter capacitor (C_5).

The usually published frequency response at 1 watt power output is not shown as it conveys little information. Response is down 1/2 dB at 19 Hz and 100 kHz when driven from a 1 KΩ source with the input filter removed.

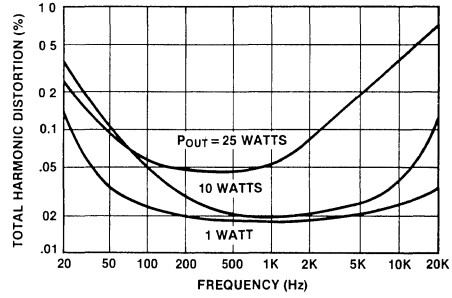
The power efficiency calculates at 53% at the 25 watt output level. The power dissipation is essentially independent of frequency and varies little with power output. It is about 17 watts at idle and increases to about 22 watts at output levels from 10 to 25 watts.

Most assemblies show no evidence of slew rate distortion until at least 30 kHz when a slight crossover glitch appears on the waveform at a level of 15 watts or more. The glitch is level sensitive due to imperfect bias tracking as a function of power output. Bias tracking also becomes worse as the frequency increases, probably because of stored charge problems in the rectifier diodes used for D_2 and D_3. This tracking error would normally not be encountered on speech or musical signals.

Choice of suitable transistors for the diff-amp is limited. Good results have been obtained by using matched pairs of type 2N2484. The gain typically is about 400 at 2 mA and although the 60 volt V_{CEO} rating seems marginal, no problems have been experienced.



Distortion vs Power Output for 25 Watt Amplifier
Figure 6



Distortion vs Frequency for 25 Watt Amplifier
Figure 7

The output devices are Siliconix type VN64GA, which typically have a transconductance of 3 mhos, an $r_{ds(on)}$ of 0.3 Ohms, and an input capacitance of 700 pF. These characteristics are needed in order to have sufficient gain in the current bias loop, good power efficiency, and wide open loop bandwidth.

Some listening tests have been run using a variety of associated equipment. Most listeners notice improved reproduction of high frequency transients and have difficulty in detecting overloads and clipping unless excessive.

A 50 Watt Design

An amplifier designed to produce 50 W into 8 Ω is shown on Figure 8. For this application low distortion is only required over a range from 50 Hz to 10 kHz. It was adapted to use an available power supply which produces + 78 V and − 52 V under no load and nominal line conditions.

Figure 9 shows total harmonic distortion at selected frequencies as a function of power output and Figure 10 shows distortion at 1, 10, and 50 watts as a function of frequency. In the important mid range, THD is under 0.1%.

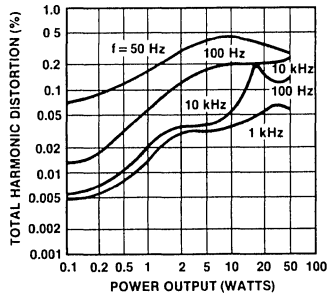
The narrower power bandwidth of the 50 watt amplifier as compared to the 25 watt amplifier is a direct result of the higher input capacitance of the higher power output devices.

To avoid serious high frequency distortion the diff-amp current was increased from 2 mA to 4 mA; the higher current necessitated a 2:1 reduction in base circuit resistance in order to avoid an excessively tight match on the current gain of the diff-amp pair with the result that the bypassing action of C5, kept at 1 μF, is less effective at low frequencies. The narrower power bandwidth of the 50 watt amplifier does not reflect a significant difference in the frequency response at 1 watt as compared to the 25 watt design.

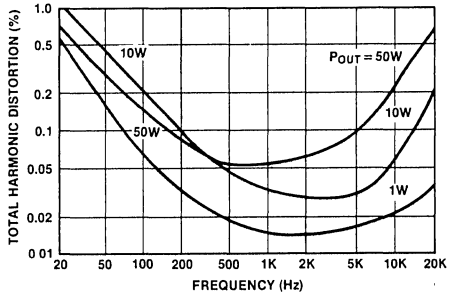
Although not shown, data at 5 watts output is similar to that at 10 watts. The low frequency distortion is higher at these levels than at 50 watts because of the imperfect filtering action of C_5. Because of the clipper circuit, the voltage on C_5 is a larger percentage of the input signal as the output drops from the 50 watt level.

The harmonic distortion spectrum is shown on Figure 11. The dynamic range of the instrument used is 90 dB. Note that the third harmonic is prominent at all power levels. The even harmonics quickly disappear, but at the 50 watt level, odd harmonics up to the 13th were detectable. Probably none of these harmonics is discernable by ear.

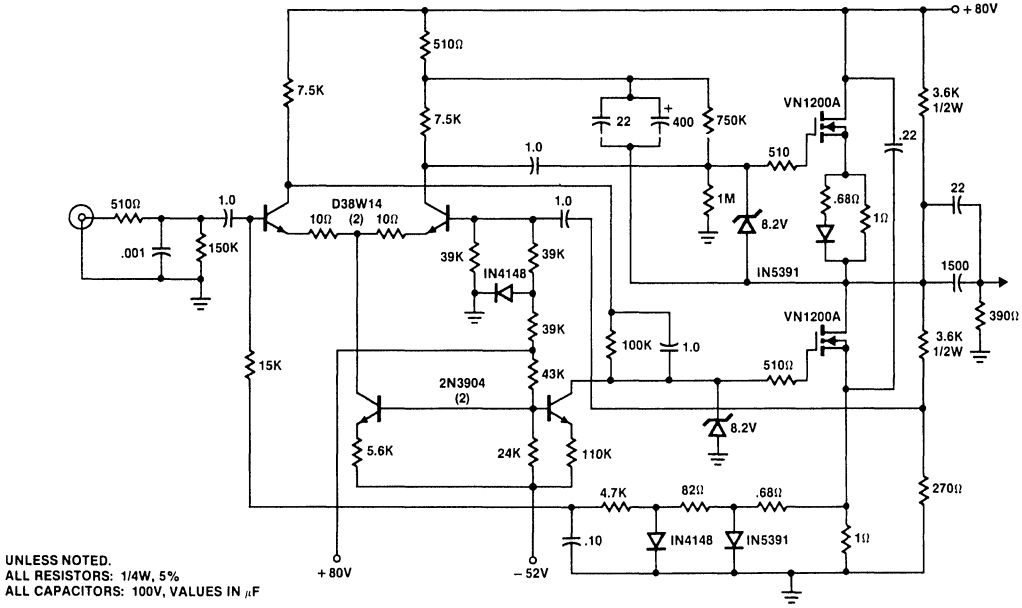
Power data is shown on Figure 12. The power efficiency calculates at 63% at the 50 watt output level. The power dissipation is essentially independent of frequency. The heat sink must handle about 40 watts of power.



Distortion vs Power Output for 50 Watt Amplifier
Figure 9



Distortion vs Frequency for 50 Watt Amplifier
Figure 10



Practical 50 Watt Autobias
Figure 8

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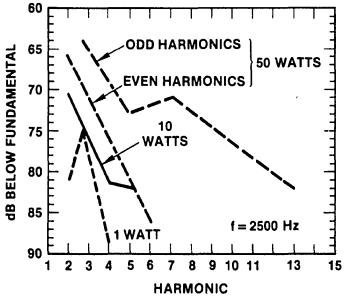
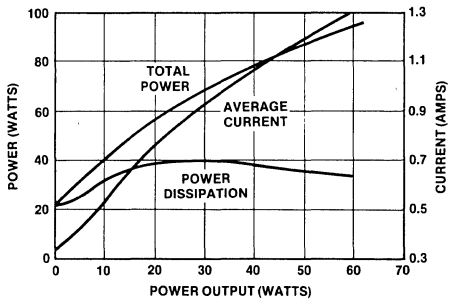


Locus of Harmonic Spectrum
Figure 11

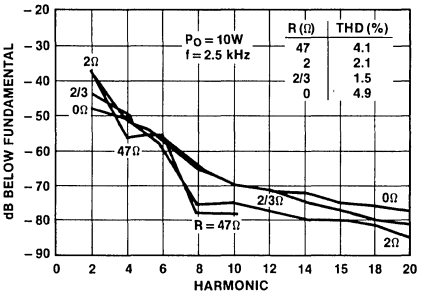


Power Requirements
Figure 12

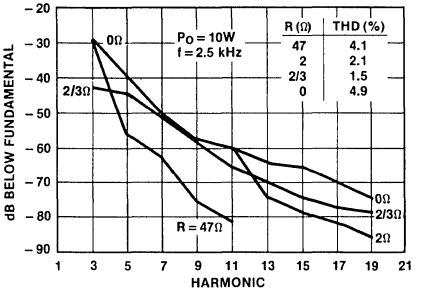
Finding suitable driver transistors for the diff-amp was not easy. The best transistor discovered to date is a D38W14 manufactured by General Electric. The transistor has $BV_{CEO} > 100V$, which allows ample voltage margin, and $h_{FE} > 400$ which places base current $< 10\ \mu A$ at 4 mA of collector current. Consequently, base current matching to within 1 μA is not too difficult and this match will produce a maximum error of 20 mV in the diff-amp which translates into a 20 mA error in the MOSFET idle current.

The MOSPOWER output transistors are VN1200As. They have 120 V breakdown ratings, an "on" resistance under 0.2 ohms, transconductance of 5 Siemens, and an input capacitance of 1200 pF. This excellent combination of characteristics plays a major part in achieving the excellent results displayed by the simple autobias circuit.

Finally, Figures 13 and 14 illustrate the tradeoffs in open loop harmonic content as the diode series resistance is varied in the dynamic bypassing scheme. With R = 47Ω, the bypassing effect is negligible, and no harmonics past the 11th are discernible. As R is reduced, high order harmonics are introduced which increase in level. However, harmonics below the 6th minimize at various values of R. In the final amplifier design, 2/3Ω was chosen as it minimized the large 3rd harmonic resulting in lowest overall total harmonic distortion. By better matching of the push-pull configuration, it should be possible to reduce the even harmonics below the levels shown.



Open Loop Output Spectrum Even Harmonics
Figure 13



Open Loop Output Spectrum Odd Harmonics
Figure 14

Conclusions

The circuit scheme presented illustrates that using MOSPOWER transistors as power output devices produces an amplifier of extraordinary performance considering the circuit simplicity. It offers the following advantages over bipolar amplifier counterparts:

1. Only one driver stage
2. Simple overload protection
3. Stable bias point
4. Power efficiency independent of frequency.

6.6.2 A Simple Direct-Coupled Power MOSFET Audio Amplifier Topology Featuring Bias Stabilization

Abstract

Utilizing the high gain and high input impedance of short channel power MOSFETs, a simple circuit has been devised to provide sufficient drive for amplifiers up to 200 watts output. The circuit described features automatic control of the quiescent bias level and offers performance which meets criteria for high quality audio reproduction.

Introduction

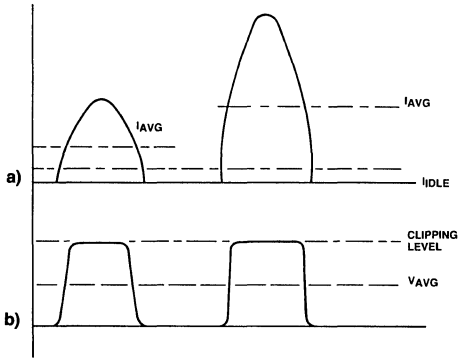
Short-channel power MOSFETs offer several characteristics attractive for audio power amplifier applications namely:

1. Low distortion at all frequencies because of a linear transfer characteristic and a very high cut-off frequency.
2. A low drive power requirement because of a nearly infinite input resistance, relatively low capacitance, and high transconductance.
3. Failure immunity because second breakdown occurs well above the power rating.
4. Freedom from minority carrier storage delay time following signal overloads because FETs are strictly majority carrier devices.
5. High power efficiency because of low "on" resistance.

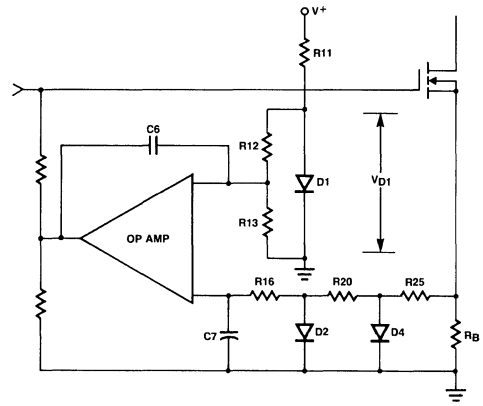
One of the major design problems has been providing a means of stabilizing the idle current level because short-channel FETs exhibit an increase of drain current with temperature at the desired idle level. Furthermore, as a result of production line variations a threshold voltage range on the order of 2 volts must be accommodated. Consequently, these FETs must be used within a closed loop bias system. The puzzler has been to provide a means of sensing the idle level despite the presence of the high current half-wave pulses which occur under Class-AB operation. A successful solution to the bias problem was the subject of an earlier paper by the author [1], however, the simple circuit in that paper used AC coupling of the audio signal. The circuit described in this paper applies this bias technique to a direct-coupled design. The resulting circuit is simple and offers outstanding performance.

The Autobias Principle

The scheme previously reported extracts the idle current from the total current by means of a clipper circuit and filter which produces a voltage related to the idle level. A small resistor in series with the source of one of the power FETs is used to sample output current. The voltage at idle is one-half of the clipping level so that when the signal is large enough to cause current cut-off on negative half cycles (thereby producing an asymmetrical waveform) the peak clipper and filter produce an average voltage which is substantially the same as the zero signal level, regardless of the amplitude of the peak current, as illustrated by the waveforms of Figure 1. The filtered voltage is used



Clipper Circuit Waveforms
a) Clipper Input
b) Clipper Output
Figure 1



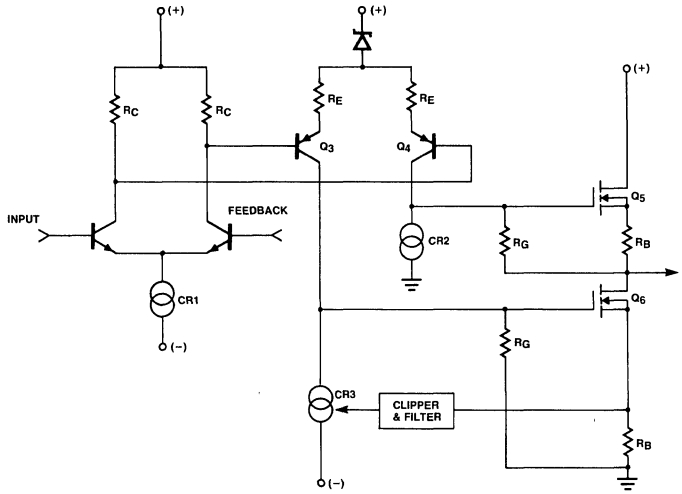
Op-Amp Bias Control for Class AB
Figure 2

in a feedback loop to control the FET gate voltage and thereby maintain the bias current within close limits.

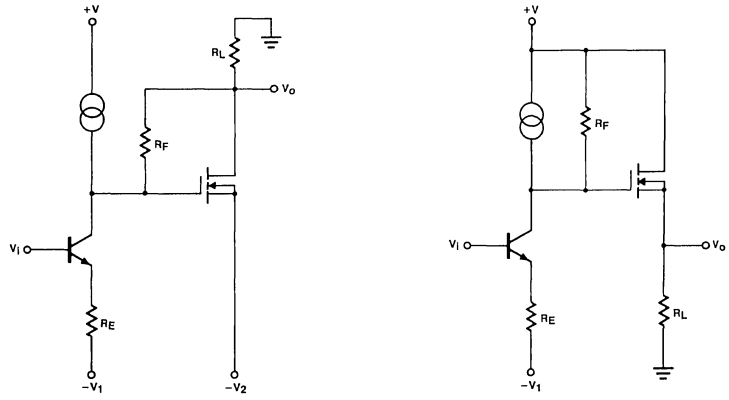
A simple technique for achieving a stable automatic bias current is shown in Figure 2. The op-amp serves as a differential amplifier in a voltage comparator loop which serves to maintain the levels at its inputs equal. Thus the idle current is simply $V_{D1}/2R_B$, since R_{12} and R_{13} are equal. The loop gain is so high that variations of FET threshold voltage or other circuit constants have no measurable effect upon the idle current level. It is important to use a two stage clipper and also match the diodes D_1 and D_2 to avoid shifts in idle level under large signal conditions; a dual matched signal diode is an ideal choice. Circuit resistors should be chosen to force equal currents through D_1 and D_2 under large signal conditions. In addition, R_{16} should be over twenty times R_{20} to prevent a significant portion of the DC level on C_7 from biasing D_2. Capacitors C_6 and C_7 filter the clipped audio signal.

Circuit Topology

The general circuit topology is shown in Figure 3. It consists of an input differential amplifier using n-p-n transistors directly coupled to a p-n-p push-pull stage which drives the output power FETs in a totem pole arrangement. A similar topology has been previously used by Sampei, et al [2], and Harvey [3], however, the implementation is different and neither circuit has automatic bias.



Amplifier Topology for Power MOSFETs
Figure 3



A Real Source Follower and a Quasi Source Follower
Figure 4

Sampei used complementary output devices whose gates are driven from a common node. The capacitive loading at the gate node is about three times higher than would be the case if n-channel FETs were driven as shown in Figure 1, because a p-channel device has about twice the input capacitance of an n-channel transistor with the same gain and on-resistance. This unfortunate situation is a result of having to construct a larger p-channel die to overcome the lower mobility of the p-type carriers. The circuit used by Harvey uses a complicated arrangement of current sources and emitter followers to achieve high gain from the input diff-amp while the p-n-p drivers act primarily as level shifters and current drivers operating at low gain.

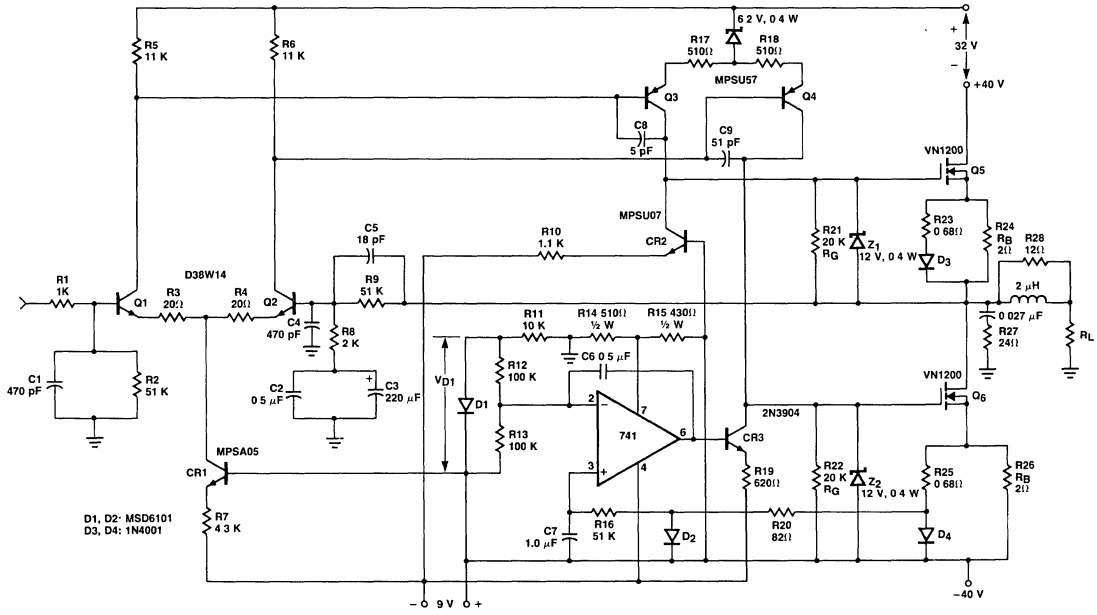
Both designs provide excellent performance, but for bias stability, FETs having a relatively long channel should be used so that the temperature coefficient of drain current is zero at the proper bias current for class AB operation. This type of FET design has poorer linearity, lower gain, and higher "on" resistance than the short channel devices now being produced in volume for general purpose applications. The design in this paper accommodates any type of FET and provides an automatic closely regulated bias control.

Totem pole output designs have not been used extensively in high quality amplifiers because of the inherent unbalance in input resistance which occurs. This is not a problem with FETs; however, an unbalance in driver frequency response occurs because the signal swing at Q_4 is several times larger than that at Q_3, which results in differing Miller capacitances. This effect was masked in bipolar designs by the poor frequency response of the output transistors but shows up when FETs are used as a small phase shift which can cause a crossover glitch at high frequencies. The problem is easily corrected by using Miller compensation capacitors of a proper ratio on Q3 and Q4. In the design shown, crossover distortion is barely evident at 100 kHz.

Circuit Implementation

Figure 5 shows a complete circuit with values suitable for a 50 watt output into an 8 Ω load. The bias control loop consists of the op-amp, CR3, Q6, and associated components. The op-amp serves as a high gain differential amplifier and integrator which further filters the output of the clipper diodes, D4 and D2, and the filter composed of R16 and C7. The op-amp controls the current source CR3 which maintains the required gate voltage for the idle current (IQ) desired. The best idle level is found by measuring distortion at a low level where class AB operation begins to occur. For the power transistors used, the effect of idle level upon low level distortion is shown in Figure 6. When making this test, it is important to select a power level where operation is beginning to move from class A to class AB.

The topology has the interesting property of allowing the output stages to operate either as common source or source follower amplifiers by simply changing the return point of the gate resistors. Figure 4 shows the follower configuration. In an amplifier with a fairly large amount of feedback, a recent paper [4] shows that the follower connection offers no advantage over a gain stage, however the follower may be useful if a high gain amplifier with a low output impedance is desired without using an overall feedback loop. Closed loop distortion tests using either configuration yielded essentially the same results with the amplifier in this paper.

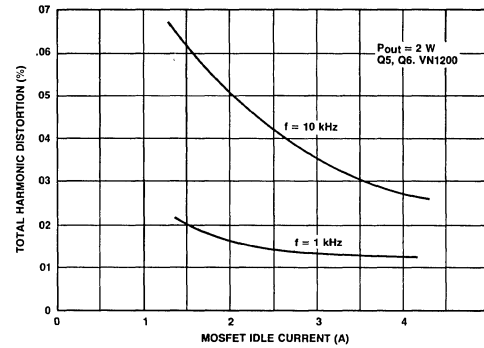


Complete Amplifier Schematic
Figure 5

The loads for the p-n-p drivers are provided by current sources (CR2 & CR3) and high-valued load resistors (RG) R21, R22. This technique permits high gain to be achieved while allowing all the driver current to charge the input capacitance of the output devices. The drivers may work class AB when the input is a fast rising signal thereby providing a high peak current in phase with the drain current to provide a high slew rate.

The drivers and the diff-amp stages are designed so that they cannot be driven into saturation. To do this requires that the stages load resistances and quiescent currents be chosen to limit the available voltage swing; to achieve reasonable gain from the diff-amp requires a driver supply voltage which at first seems unnecessarily high (32 V) but is readily available from a standard 24 volt transformer. The current drain from this supply is fairly low, however, requiring only 8 mA for each driver plus 2 mA for the diff-amp.

In addition, the driver supply is non-critical with regard to hum or absolute value. It is possible to obtain this supply by bootstrapping from the amplifier output, but a very large capacitor would be required to avoid a serious increase in low frequency distortion. The result is that bootstrapping works out to be less satisfactory and more expensive than the approach shown. The supply need not ride on the +40 V rail. It is just as satisfactory to have a +72 V supply with respect to ground; it could serve both channels of a stereo pair.



Effect of Idle Level on Harmonic Distortion
Figure 6

The −9 V line which rides on the −40 V rail also supplies about 20 mA and must be well filtered to prevent AC ripple from being amplified by CR3 and injected into the gate of Q6. A zener diode is an effective filter and also provides a reference level for the current source transistors CR1 and CR2. Neither the absolute value nor the regulation of the other supplies is critical. Any desired power output may be obtained from the circuit by simply altering the value of the main rails. Automatic switching between two supplies could also be used to improve power efficiency. No circuit changes are necessary other than altering the divider to the supply terminal, pin 7, of the op-amp to avoid exceeding its voltage rating (30 V) and using transistors with sufficient voltage breakdown.

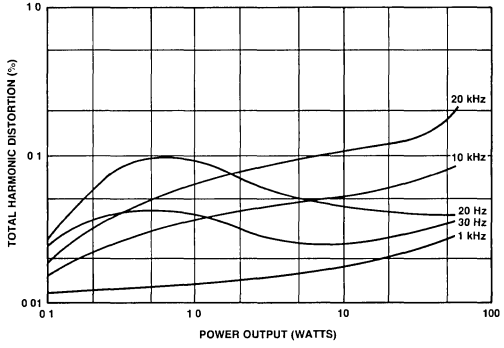
The diode D4 serves not only as part of the bias clipper network but also provides dynamic bypassing of the 2 ohm sense resistor. The diode reduces third harmonic distortion and increases power output at the expense of introducing a number of low-level high order harmonics into the output. This action is illustrated in detail in reference [1]. A similar network must be used in the source circuit Q_5 to balance both halves of the push-pull output stage.

The zener diodes Z_1 and Z_2 provide overload protection with a shorted output. They are chosen to limit the gate drive to a level such that $I_D < P_{D(rated)}/V+$. In addition, the zeners prevent large voltages from breaking down the FET gate-oxide layer. The zeners also conduct in the normal diode forward direction when the gate signal would normally swing the gate signal below the source. This action not only protects the gate but prevents the signal from saturating CR3 which would render the bias control loop inoperative.

Since most power MOS devices have a cut-off frequency in the gigacycle range, parasitic RF oscillations can be troublesome. Most assemblies require bypasses on the order of 0.22 μF, connected from supply lines at the FET location. In addition, leads running to the gate terminal should be either shielded or used as a twisted pair with a ground lead.

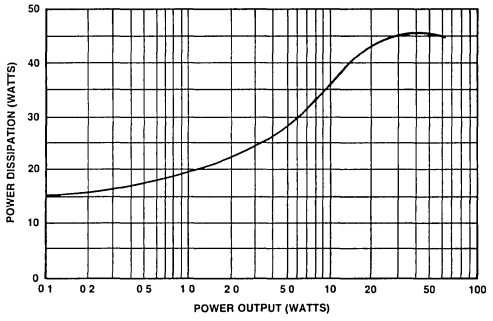
Performance

Curves of distortion as a function of frequency and power output are shown in Figure 7. In summary, total harmonic distortion is generally under 0.1% throughout the audio range. The unusual rise in 20 Hz distortion at ½ watt is caused by the imperfect filtering of the output of the clipper circuit in the bias control loop. Because of the clipper circuit, the voltage on C_5 becomes a larger percentage of the input signal as the output drops from the 50 watt level.

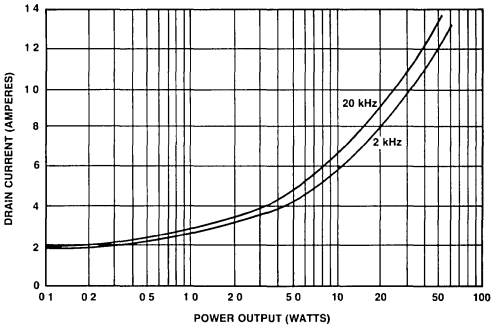


Distortion Characteristics
Figure 7

Power dissipation and efficiency as a function of power output are shown on Figures 8 and 9. Power efficiency is about 60% at full output and is essentially independent of frequency.

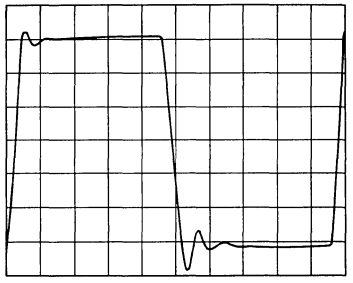


Power Dissipation in Both Output Transistors versus Audio Power Output
Figure 8



Current from Main Supplies versus Audio Power Output
Figure 9

Figure 10 shows a 100 kHz square wave output when the input filter R_1 C_1 is removed. With the filter in place, the slight 1 MHz ringing disappears. Rise time and frequency response can be varied by altering the value of C_5.



Output Voltage with 100 kHz Square Wave Input. Input Filter Removed (5 V/Division)
Figure 10

6

The output coupling filter permits capacitive loads to be driven without introducing oscillation. With a 1 μF load, distortion rises slightly at high frequencies.

Some listening tests have been conducted. Listeners are usually impressed and use terms like "smooth," "musical," and "excellent transient reproduction" to describe the sound. In addition, it is very difficult to detect when the output stages are driven into clipping. It appears that the circuit is suitable for the highest quality audio reproduction.

Summary

A simple circuit using short-channel power MOSFETs has been devised. It features high power efficiency and low distortion over the audio band, high slew rate, bias stability, fast overload recovery, and short-circuit protection. Listening tests have rated it very high in audio accuracy. Since it is potentially low cost and usable for power levels up to 200 watts, it should have wide application in the audio industry.

References

[1] Bill Roehr, *"The Autobias Amplifier, A New Topology for Automatically Biased Audio Amplifiers Using Power MOSFETs,"* Journal of the Audio Engineering Society, Vol. 30, No. 4, April 1982, pp. 208–216.

[2] Tohru Sampei, Shin-ichi Ohashi, and Shikayaki Ochi, *"100 Watt Super Audio Amplifier Using New MOS Devices,"* IEEE Transactions on Consumer Electronics, Vol. CE-23, No. 3, August 1977, pp. 409–416.

[3] Barry Harvey, *"Power-FET Amplifier Designs Boost Fidelity, Reduce Complexity,"* EDN, Vol. 25, No. 17, Sept. 20, 1980, pp. 137–142.

[4] Edward M. Cherry and Gregory K. Cambrell, *"Output Resistance and Intermodulation Distortion of Feedback Amplifiers,"* Journal of the Audio Engineering Society, Vol. 30, No. 4, April 1982, pp. 178–191.

6.6.3 A MOSFET Power Amplifier with Error Correction

Abstract

Power MOSFETs are emerging as the device of choice for high-quality power amplifiers because of their speed, reduced need for protection and falling cost. A low-distortion power amplifier design is illustrated which includes output stage error correction to reduce the effect of transconductance droop in the crossover region and thus allow operation at more efficient bias levels.

Introduction

The rapid evolution of power MOSFETs during the last few years has brought them to the point where they are now very attractive for use in audio amplifier power output stages. Important improvements which have been made include increased voltage, current and dissipation ratings, reduced "on" resistance, availability of complementary pairs and greatly reduced cost. Although a 75-watt MOSFET is still more expensive that a 150-watt bipolar transistor, the premium is small when considered relative to total amplifier cost and improved performance.

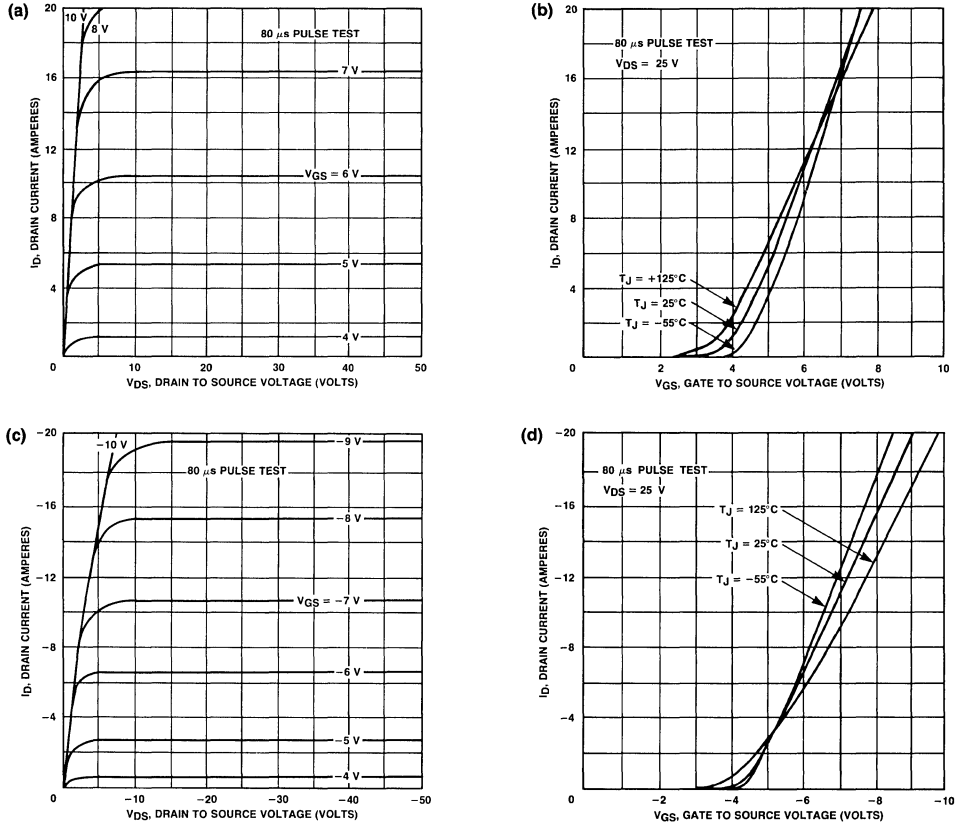
The purpose of this paper is to demonstrate the level of performance achievable with current technology and illustrate practical circuit techniques for achieving this performance.

Power MOSFETs have several fundamental advantages over bipolar power transistors, most notably speed and freedom from secondary breakdown. The latter provides higher "usable" power dissipation, improved reliability, and freedom from safe-area limiter circuits which can misbehave and cause audible degradation. MOSFETs also have some disadvantages in comparison with bipolar transistors. These include higher turn-on voltage drive requirements and smaller transconductance at low current levels. The former tends to contradict generalizations which have been made to the effect that drive circuits for power MOSFETs are less expensive, at least for the reliable source-follower configuration. The latter results in transconductance droop in the crossover region if bias currents are not fairly high. Such transconductance droop can result in crossover distortion.

In this paper we will illustrate a high-performance amplifier design which utilizes the advantages of the power MOSFET while dealing with the drawbacks of the device. Although not taken to an extreme, the underlying philosophy of the design is that small-signal silicon is inexpensive, i.e., that the overwhelming portion of expense in a power amplifier is in items like the power transformer, filter capacitors, power transistors, heat sinks, chassis and related hardware. Thus, in order to take full advantage of the performance achievable with the MOSFET output stage, a very high quality front-end and driver are provided. The driver, operating from regulated boosted supplies, is capable of providing high voltage and current swings to the power MOSFETs with good headroom. Output stage transconductance droop is dealt with by employing a simple but very effective output stage error correction technique proposed by Hawksford. [1] The resulting design achieves a 20-kHz THD figure of less than 0.0015 percent at an idle bias of only 150 mA.

MOSFET vs. Bipolar Output Stages

Design of MOSFET power amplifiers is quite straightforward and conventional as long as differ-



Drain and Gate Characteristics for Power MOSFET Types IRF-132 (a&b) and IRF-9130 (c&d)
Figure 1
(Drawings courtesy of International Rectifier, Inc.)

ences between MOSFETs and bipolar transistors are understood. Figure 1 shows the drain and gate transfer characteristics typical of the vertical DMOS devices used in this project (International Rectifier types IRF-132 and IRF-9130). [2] The important point to see here is that these enhancement devices require about 3 volts of forward gate bias to begin to turn on (e.g., gate threshold voltage, V_t) and may require as much as 10 volts to conduct high currents (12 amperes). While the required bias voltage is thus higher than for bipolar transistors, it can still be generated by the traditional V_{be} multiplier circuit. Thermal bias stability for the power MOSFETs is much better than that for bipolar transistors, even though the vertical DMOS devices have a Vgs temperature coefficient of about -5.0 mV/°C at a typical bias current of 150 mA. This is partly due to the MOSFET's lower transconductance at the bias point. The MOSFETs negative temperature coefficient of transconductance also tends to improve thermal bias stability. As a result, in some cases, a V_{be} multiplier transistor or associated reference diode need not be mounted on the heat sink.

If the popular source-follower output stage configuration is used, the substantial gate drive voltage required for high currents means that the driver stage should be provided with a "boosted" power supply voltage greater than that of the main high-current supply in order to take full advantage of the voltage swing available from the latter. The current requirements for the boosted supply are small, and it can be regulated at little additional expense, thus reducing hum, crosstalk and modulation distortion. Several high-quality bipolar power amplifiers also use boosted driver supplies, some regulated.

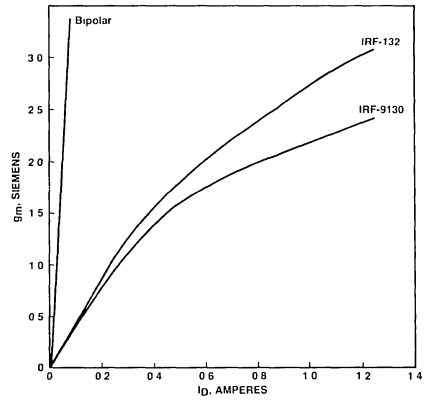
While bipolar transistors are regularly placed in parallel with small individual emitter ballast resistors, the paralleling issue is not as straightforward for power MOSFETs, at least in linear applications. It has been said that the negative temperature coefficients of transconductance and "on" resistance of MOSFETs act to suppress current hogging by one transistor, thus permitting easy paralleling of MOSFETs without ballast resistors. This appears to be true for hard-

switching applications where the paralleled devices are all fully turned-on together (i.e., channels fully enhanced by forward gate voltage) so that current and dissipation imbalances are only a result of mismatched "on" resistance.

However, the issue is more complex for linear, and especially low-distortion, applications because the operating region of interest is not the fully turned-on region, but rather the linear region wherein drain current at a specified gate voltage is important. Specifically, recognizing that the gate threshold voltage specification for these devices is 2–4 volts, an examination of the gate transfer characteristics of Figure 1 indicates that a very serious current imbalance can exist unless gate threshold voltages among paralleled devices are reasonably matched. It is also apparent that reasonable temperature differentials will not adequately reduce the imbalance. Because of the size of the worst-case threshold voltage differentials possible, source ballast resistors are not a reasonable approach to achieving balance. It thus appears that for high quality audio applications where paralleled devices are necessary, both threshold voltage and transconductance of paralleled devices should be matched. Threshold matching that guarantees that all devices are "on" to some extent in the quiescent bias state, and transconductance matching to within 20% is probably adequate.

Modern complementary MOSFETs, with maximum "on" resistances of only about 0.3 ohms, are just about as efficient as bipolar transistors in terms of voltage dropped from supply rail to load in output stages. However, they typically require a higher operating current to achieve a given transconductance. This characteristic is illustrated in Figure 2. The device transconductance in a source-follower or emitter-follower output stage is important because it determines the small signal voltage drop through the stage as a function of current. This is especially important in Class-AB stages where it is desirable that the sum of the effective transconductances of both halves be high and be constant with current so as to avoid crossover distortion. It can be seen from Figure 2 that approaching this condition with power MOSFETs requires fairly substantial bias current (as a rough starting point, that current where transconductance is one-half its high-current asymptotic value), on the order of a few hundred milliamperes.

In contrast, bipolar power transistors are typically biased at a much lower current, but this is not entirely advantageous. A typical bipolar output stage will often be biased approximately where the dynamic emitter resistance of the output devices ($1/g_m$) at crossover is equal to the associated ballast resistance as a compromise in achieving approximately constant total output stage transconductance as a function of current.



Power MOSFET Transconductance versus Drain Current. For comparison, note much greater ratio of transconductance to operating current typical of bipolar transistors
Figure 2

This is done because both halves are "on" and contribute transconductance in the crossover region while only one half contributes transconductance at currents well outside the crossover region. This usually results in bias currents of less than 100 mA per output transistor, sometimes as low as 20 mA. This small amount of bias current compared to several amperes of signal current being handled can sometimes result in unexpected temporary bias inadequacy, resulting in crossover distortion, because a small change in circuit parameters (about 50 mV) can cause the bias current to vary considerably. This can happen as a result of the time delay in the intentional thermal feedback loop created by placing the bias generator sensing junction on the heat sink; the temperature of this junction will differ from that of the power transistors as a result of thermal delay, low-pass filtering and attenuation. After a high dissipation interval ends, the amplifier may find itself temporarily underbiased because the power transistor junctions cooled down faster than the bias transistor.

Bipolar output stages can be operated in an overbiased mode, but the penalty can be dangerously reduced thermal stability if larger heat sinks are not used, or increased crossover distortion if larger ballast resistors are used. Much less thermal feedback is necessary for thermal stability of MOSFET output stages and their higher bias is less likely to disappear under transient thermal conditions. Compared to bipolar designs, Class-AB MOSFET power output stages also tend to have a wider Class-A region of operation and a smoother transition to the Class-B region of operation.

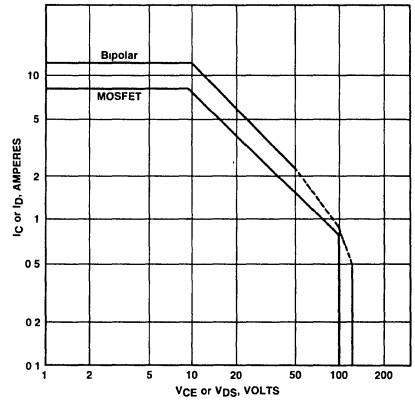
Although power MOSFETs require virtually no drive current at low frequencies, their substantial input capacitance means that drive circuits with forward and reverse drive capabilities similar to those employed

with bipolar transistors should be used for wideband, high slew-rate circuits for demanding audio applications. Although the gate-source capacitance can be on the order of 700 pF, this capacitance is effectively "bootstrapped" in a source follower output stage, typically reducing its effect by about an order of magnitude. The smaller gate-drain capacitance, about 100 pF, is also present. A 100 $V/\mu s$ slope with an effective capacitance of 170 pF thus requires a 17 mA current capability from each driver.

Power MOSFETs tend to be inherently faster than bipolars, partly because there are no minority carrier effects. Their speed is primarily limited by the ability of the drive circuitry to charge the internal gate electrode capacitance through the effective gate resistance. The wider bandwidth, reduced excess phase and reduced variation of device speed with voltage and current tend to allow greater high-frequency negative feedback with greater stability. The higher switching speed also tends to reduce dynamic crossover distortion. Furthermore, the MOSFET's higher switching speed greatly reduces the flow of Class-AB common-mode current at high frequencies which poses such a destructive threat to many bipolar designs.

However, power MOSFETs do have a tendency to very high frequency parasitic oscillations in real-world circuits. This appears to be a result of the natural high speed of the device combined with the substantial drain-source capacitance (300 pF) typical of these devices, making formation of a Colpitts oscillator easy if inductance is present in the gate circuit. This often necessitates the use of a small resistor in series with the gate. In combination with the device input capacitance, this resistor (typically about 100 ohms) can create an additional pole which tends to reduce the high-frequency improvement over bipolar transistors.

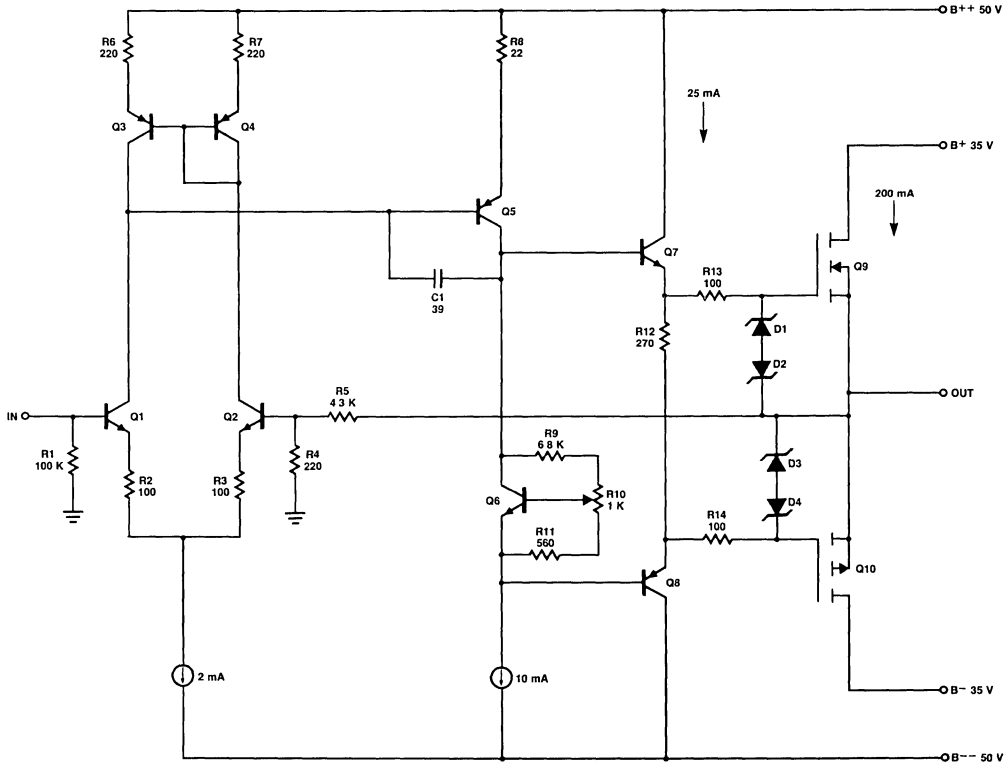
Perhaps one of the most important advantages of power MOSFETs for audio use is their freedom from secondary breakdown and large safe operating area (SOA). A highly simplified explanation of secondary breakdown in bipolar transistors is that it results from localized current hogging which in turn results from localized thermal "hot spots." Transistor current at a given base-emitter voltage has a very strong positive temperature coefficient. Thus, a "hot spot" carries more current and gets even hotter as a result. This regenerative process, once started, can be very rapid and unforgiving. It can persist even after the external voltage and current conditions re-enter the safe operating area, leading to destruction. The relationships in a power MOSFET are in contrast *degenerative* in nature because hotter regions exhibit reduced transconductance and thus tend to conduct less of the total current. This tends to equalize the temperature across the chip. The safe area of a MOSFET is thus primarily governed by simple thermal considerations of how much energy (product of power and time) is required to raise the temperature of the hottest point on the chip (which will not be much different than the average temperature of the whole chip) to a dangerous point.



Safe Operating Area (SOA) Comparison of Bipolar Ring-Emitter Transistor (2SA-1072) and a Power MOSFET (IRF-9130). Rated power dissipations are 120 W and 75 W, respectively
Figure 3

Figure 3 shows a comparison of safe operating area for a power MOSFET and a typical bipolar power transistor. Notice that there are no steep secondary breakdown SOA slopes at high voltages for the MOSFET — it is essentially limited by simple power dissipation over its full voltage range. This is also true for short-term dissipation well in excess of rated continuous dissipation, where thermal time constants govern the allowable excess dissipation. For example, a 25-ampere peak with 100 volts across the MOSFET can be handled for 10 microseconds. Figure 3 illustrates that "usable" dissipation (SOA at higher voltages) for a MOSFET may be equal to that of a bipolar power transistor of substantially higher rated power dissipation. Safe operating area at high voltages is particularly important when difficult reactive loads are being driven. In many power amplifiers the use of multiple paralleled output devices is for reasons of increased safe operating area rather than simple thermal considerations. Finally, freedom from secondary breakdown means freedom from complex safe-area limiter circuits, some of which are notorious for their misbehavior. [3]

Figure 4 illustrates a simple 50-watt MOSFET power amplifier design. It is notably similar to what a simple bipolar power amplifier design would look like. Transistors Q1 and Q2 comprise the input differential amplifier whose output is converted to a single-ended current by current mirror Q3, 4. This current feeds the common-emitter pre-driver Q5 which is provided with a constant-current load. Capacitor C1 provides Miller-effect feedback compensation and establishes a



A Simple MOSFET Power Amplifier. Note use of boosted supplies for driver circuitry to satisfy power MOSFET gate drive requirements
Figure 4

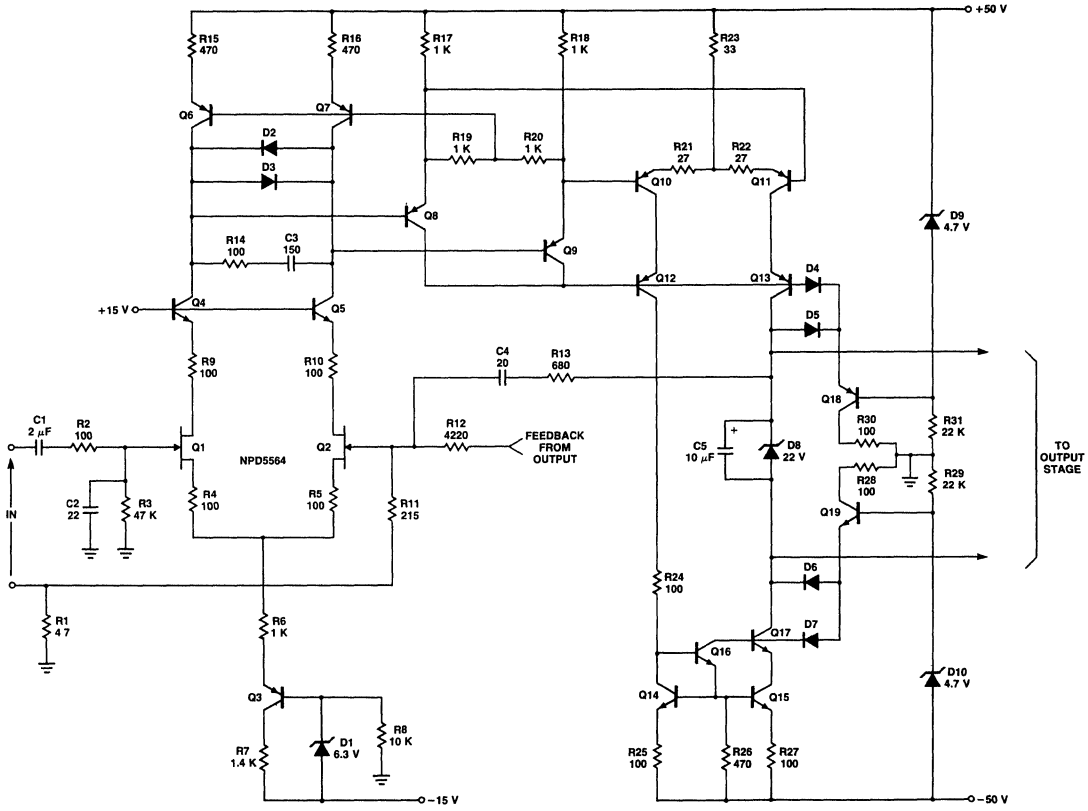
stable gain-crossover frequency of approximately 2 MHz. Transistor Q6 is connected in a conventional V_{be} multiplier circuit to provide adjustable bias (nominally about 8 V) for the output stage. If thermal feedback is required, a sensing diode placed directly in series with the emitter of Q6 (with appropriate modification of associated resistor values) and mounted on the heat sink will provide approximately the correct degree of compensation. Emitter-follower drivers Q7 and Q8 provide a low-impedance drive for the gates of power MOSFETs Q9 and Q10. The drivers isolate the high-impedance pre-driver collector circuit from the nonlinear input capacitance of the MOSFETs and provide adequate charge and discharge current for the MOSFET gate circuits. The boosted supplies for all circuits prior to the output stage enable the drive circuitry to provide adequate gate voltage to fully turn-on the MOSFETs while maintaining margin against saturation. Zener diodes D1–D4 protect the MOSFETs from excessive gate-source voltages of either polarity.

High-Performance Input and Driver Circuits

As would be the case with a bipolar design as well, many improvements can be made to the "front-end" of the simplified amplifier of Figure 4 in order to provide higher performance and take full advantage of the capability of the MOSFET output stage. Although substantially adding to the complexity of the schematic in appearance, such improvements primarily involve only small-signal, low-voltage transistors and inexpensive passive components, and thus contribute only a small percentage increase to total amplifier cost.

The front-end for the amplifier to be discussed here is shown in Figure 5. The input stage is a differential JFET-bipolar cascode with a constant current bias supply. The cascode allows the use of a low-noise dual JFET, achieving a referred input noise of less than 6 $nV/\sqrt{Hz}$. It also provides good common-mode and power supply rejection, necessary because negative feedback is not very effective in reducing power supply and common-mode impairments introduced at the input stage. The degenerated JFET input stage can handle fairly large open-loop input signals with relatively low distortion, making the amplifier relatively immune to transient intermodulation distortion (TIM) and RFI effects.

The input stage is loaded by current sources (Q6, Q7) to provide high open-loop gain at low frequencies.



MOSFET Power Amplifier Front End. Differential cascode circuitry minimizes distortion
Figure 5

Emitter followers Q8 and Q9 isolate the input stage from second-stage (pre-driver) loading effects and produce a combined common-mode feedback to properly bias Q6 and Q7. This also provides additional common-mode rejection by reducing the common-mode impedance seen by the collectors of the input stage. Limiter diodes D2 and D3 prevent excessive signal swings at the collectors of Q4 and Q5 when the amplifier is clipping.

The complementary pre-driver stage consists of a differential cascode (Q10–13) loaded with a Darlington-cascode current mirror (Q14–17) to provide a single-ended drive for the output stage. The cascode achieves high speed by eliminating Miller effect and allowing the use of fast low voltage transistors in the common-emitter differential amplifier. Elimination of Miller effect is also important in reducing high-frequency distortion resulting from nonlinear collector-base junction capacitance. [4] The cascode configuration also improves low-frequency linearity and power supply rejection by reducing Early effect. The complementary pre-driver structure, made possible by the current mirror, greatly reduces second-order distortion.

Transistors Q18 and Q19 provide regulated bias for the cascode bases and emitter-follower collectors. Adequate current is available so that these voltages remain stable even under clipping conditions. Diodes D4–D7 prevent the cascodes from saturating when the amplifier clips. Zener diode D8 provides for two identical drive signals offset by 22 volts to allow for biasing and error correction in the output stage.

Overall negative feedback connections and frequency compensation are also shown in Figure 5. R11 and R12 set the closed-loop gain at approximately 20. The resistance of this divider was chosen to be fairly low to avoid noise and maintain good high-frequency characteristics. As a result, current flow and dissipation is not insignificant (100 mW in R12 at 50-watt operating level). To avoid thermally-induced distortion at low frequencies, these resistors should be over-sized metal-film types, 1-watt and 2-watt respectively.

Feedback compensation is provided by C4 and R13 which implement rolloff feedback from the output of the pre-driver to the inverting amplifier input, estab-

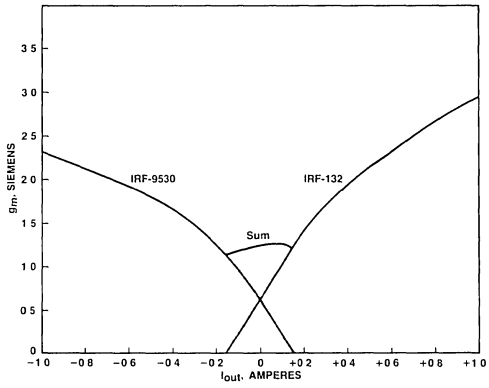
lishing a stable gain crossover frequency of about 2 MHz. Providing compensation by feedback to the input stage tends to allow improved slew rate and reduced power supply coupling; the latter because both ends of the network are ground-referenced (in contrast to the Miller-effect compensation of Figure 4). Elements C3 and R14 act to stabilize the loop formed by C4 and R13. This front-end design enables the amplifier to achieve a slew rate in excess of 300 $V/\mu s$.

Output Stage and Error Correction

In virtually any well-designed power amplifier the output stage ultimately limits performance. It is here where both high voltages and large current swings are present, necessitating larger, more rugged devices which tend to be slower and less linear over their required operating range. The performance-limiting nature of the output stage is especially true in Class-B and -AB designs, where the signals being handled by each "half" have highly nonlinear "half-wave-rectified" waveforms and where crossover distortion is easily generated. In contrast, it is not difficult or prohibitively expensive to design front-end circuitry of exceptional linearity.

Overall negative feedback greatly improves amplifier performance (including dynamic distortions such as transient intermodulation distortion [4]), but it becomes progressively less effective as the frequency or speed of the errors being corrected increases. High-frequency crossover notch distortion is a good example. For this reason, several high-performance amplifier designs now employ feedforward error correction in addition to conventional negative feedback. However, some of these designs can be complex and expensive. The philosophy of this design is based on the observation that only the output stage needs extra error correction and that such local error correction can be less complex and more effective.

While the power MOSFET has many advantages, it was pointed out that the lower transconductance of the MOSFET will result in considerable crossover distortion unless rather high bias currents are chosen. Figure 6 illustrates this effect by showing the individual and summed transconductances of both halves of a Class-AB MOSFET output stage as a function of net output current. At a bias current of 150 mA and a load of 8 ohms, this transconductance variation can result in open-loop output stage harmonic distortion on the order of one percent, as pictured in Figures 7a and 7b. Mismatches in the transconductance characteristics of the top and bottom output devices also contribute to the distortion of Figure 7. Again, while bipolar transistor transconductance is high enough and consistent enough that it is relatively unimportant in an emitter-follower stage, MOSFET transconductance is smaller

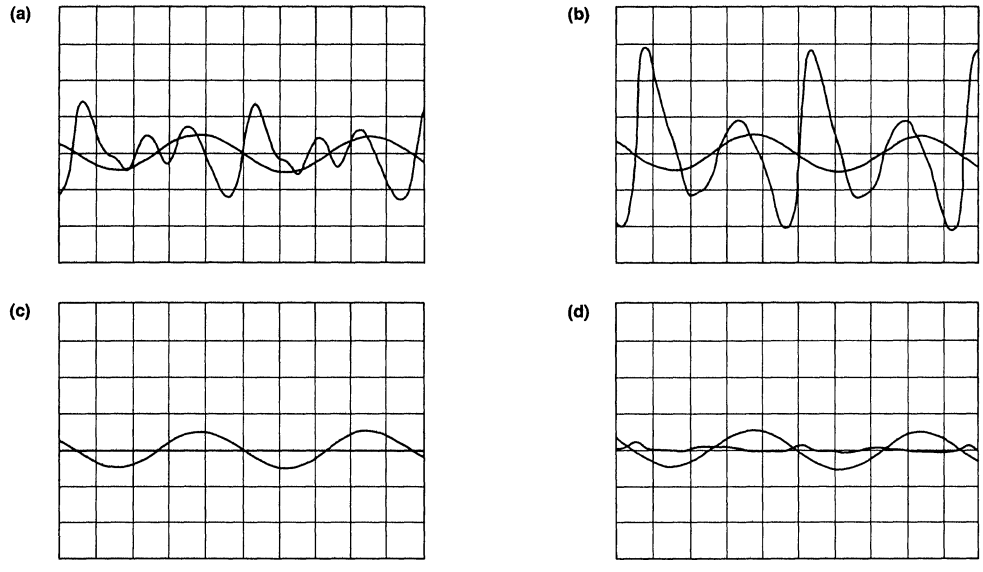


Output Stage Transconductance versus Output Current (I_{bias} = 150mA). Reduced Total Transconductance in Central Region can Cause Crossover Distortion.
Figure 6

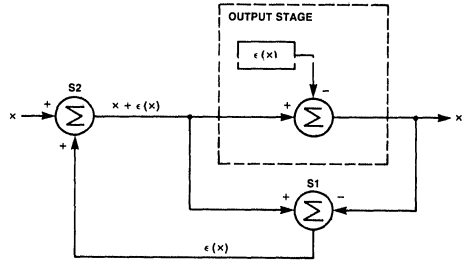
and less consistent, making it a significant parameter in source-follower stages.

Figure 8 illustrates an error correction technique described by Hawksford which is well-suited to this application. [1] Here the output stage, being a source follower, is modeled as having exactly unity gain with an error voltage e(x) added. This error represents any departure from unity gain, whether it is a linear departure due to less than unity gain, a distortion due to transconductance nonlinearity, or injected errors like power supply ripple. A differential amplifier, represented by summer S2, merely subtracts the output from the input of the power stage to arrive at e(x). This error signal is then added to the input of the power stage by summer S1 to provide that distorted input which is required for an undistorted output. Note that this is an error cancellation technique like feedforward as opposed to an error reduction technique like negative feedback. This technique is in a sense like the dual of feedforward. It is less expensive because the point of summation is a low-power internal amplifier node. It is less critical of component tolerances and frequency response matching because less circuitry is enclosed and that circuitry is simple. Feedforward tends to become less effective at very high frequencies because the required phase and amplitude matching for error cancellation becomes progressively more difficult to maintain. The technique of Figure 8 also tends to become less effective at very high frequencies because, being a feedback loop (albeit not a traditional negative feedback loop), it requires some amount of compensation for stability, detracting from the phase and amplitude matching.

A schematic of the MOSFET power amplifier's output stage and error correction circuit is shown in Figure 9. The error correction circuit is a slightly modified ver-



Output Stage Open-Loop distortion (THD); a) 1 kHz, No Error Correction; b) 20 kHz, No Error Correction; c) 1 kHz, with Error Correction; d) 20 kHz, with Error Correction. Vertical Distortion Scale 0.5 percent/div. All Measurements at Full Power (50 W).
Figure 7

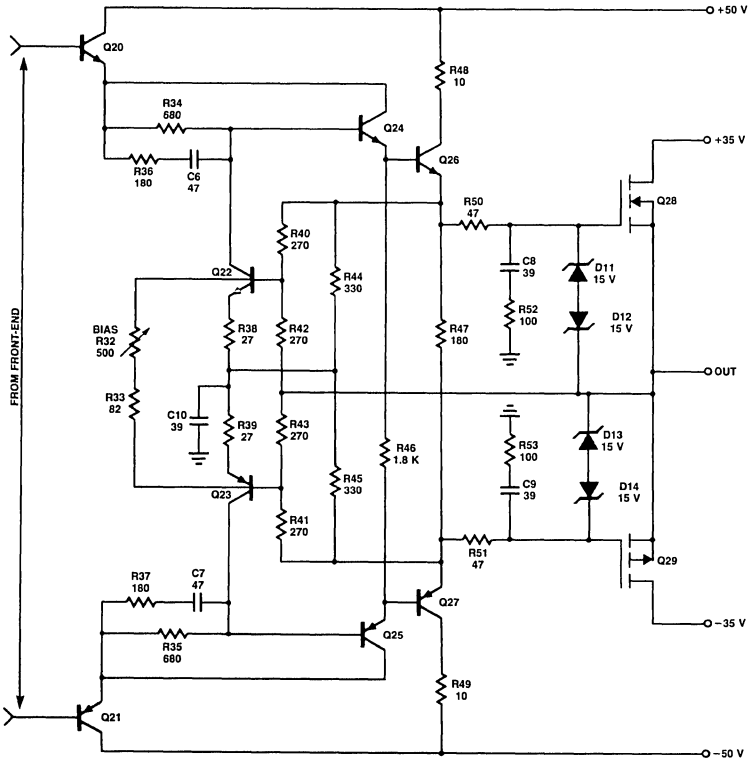


Output Stage Error Correction[1]
Figure 8

sion of one illustrated in reference 1. Emitter followers Q20 and Q21 isolate the high-impedance pre-driver output nodes from the output stage and provide a low-impedance signal for the error correction summation process. Double emitter followers Q24, Q26 and Q25, Q27 provide a high-current drive capability for the MOSFET gates and isolate the error correction summing nodes from the MOSFET gate loads. Note that Q24 and Q25 can be fast, inexpensive small-signal transistors. Transistors Q22 and Q23 and resistors R38–R45 comprise the differential amplifier for summer S2 of Figure 8. The output current of these transistors is summed with the input signal (summer S1 of Figure 8) by means of R34 and R35. For error correction, the top and bottom halves (Q22, Q23) work independently to produce identical correction signals. Input signals offset by ±11 volts, as supplied by the pre-driver circuit, provide DC operating voltage for these circuits. These offset voltages must be adequate to allow for the maximum bias plus V_{GS} signal swing required by the MOSFETs. Transistors Q22 and Q23, in conjunction with R32 and R33, control the DC voltage drop across R34 and R35. They thus set the bias for the MOSFETs by means of a V_{be}-referenced feedback loop which also includes Q24, Q25, Q26 and Q27. Resistors R38 and R39 control the loop gain of the bias loops and improve stability. Overall frequency compensation of the error correction and bias loops is provided by R36, R37, C6, C7 and C10.

Figures 7c and 7d show open-loop distortion of the output stage with error correction to be less than 0.1%, illustrating an improvement of better than an order of magnitude, even at 20 kHz. This was achieved with 5% tolerance resistors. While use of closer-tolerance resistors would improve the correction at lower frequencies, where it is unnecessary, their use would make a smaller improvement at 20 kHz because performance there is beginning to be limited by the speed of the error correction loop. Sensitivity of 20-kHz THD to tolerance in the error correction circuit has been measured to be approximately 0.0002% per percent in the closed-loop amplifier. For ultimate performance, a pot can be placed between the junctions of R38, R39 and R44, R45.

The output stage is completed by C8, C9 and R50–53 for control of parasitic oscillations and D11–D14 for protection of the MOSFET gates from excessive drive voltages. As mentioned in Section 2, power MOSFETs are considerably more prone to high-frequency



MOSFET Power Amplifier Output Stage. Q22 and Q23 Provide Error Correction Signals
Figure 9

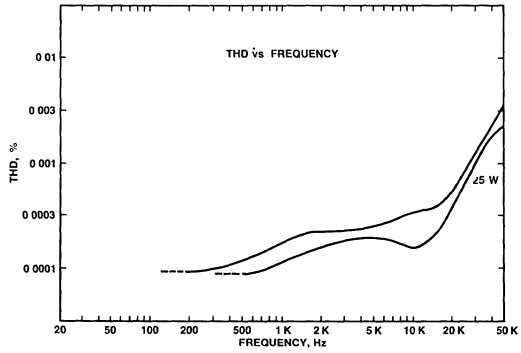
parasitic oscillations than bipolar power transistors because of their inherent high-speed nature and because of their substantial drain-source capacitance, making it easy to form an efficient Colpitts oscillator structure with inductance in the gate circuit. The amount of series gate resistance required for suppression of parasitic oscillations grows in proportion to the amount of inductance in the gate circuit. For high-speed output stage operation it is therefore important to minimize this inductance. Although not employed in Figure 9, this can be done especially well by shielding the gate leads back to the driver transistors, grounding the shield to the local bypass ground at each end. Then only a 10-ohm series resistor at the driver end and a ferrite bead at the gate end are necessary.

Performance

This amplifier employs substantial amounts of negative feedback (40 dB at 20 kHz), and 20-kHz total harmonic distortion (THD) was the primary performance metric used in the design process. In recent years several new forms of distortion have been described, sometimes in the belief that they were caused by large amounts of negative feedback and that traditional measures of distortion (e.g., harmonic and intermodulation) would be ineffective in detecting them. Some of these beliefs have been shown to be unfounded. 4–10 Nevertheless, it was decided to include some of these newer measures of distortion in the performance evaluation.

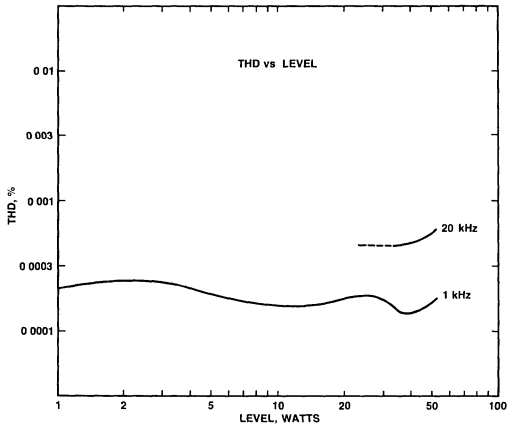
In spite of the error correction, which improves performance by more than an order of magnitude, transconductance variation in the output stage is still the dominant source of distortion in this amplifier. For this reason, output stage bias current continues to influence performance and tradeoffs can be made. The measurements presented here were made at a bias current of 150 mA, resulting in a quiescent output stage power dissipation of 11 watts for the 50-watt amplifier. It should also be noted that the transconductance characteristics of the N- and P-channel output devices were not matched.

A word about measurement technique is in order. In many cases the distortions being measured were below those levels measurable by conventional equipment and techniques. In order to add dynamic range to that provided by the equipment employed, a distortion magnifier circuit was utilized. This circuit scales the output level of the noninverting amplifier under test



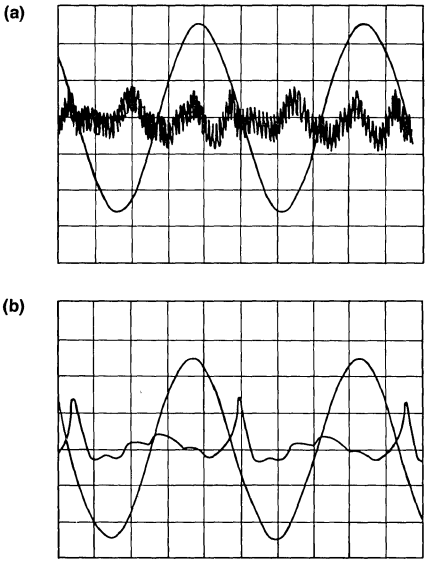
Total Harmonic Distortion (THD) as a Function of Frequency
Figure 10

down to that of the input, subtracts the two, reintroduces 11 percent of the scaled-down amplifier output signal, and finally multiplies the result by 9 for presentation to the measuring equipment. The net effect is to provide unity gain for the fundamental and a gain of ten to distortion products generated by the amplifier under test. Amplitude and phase balance adjustments were incorporated into the output signal path prior to the subtraction to achieve a fundamental null of greater than 60 dB to frequencies beyond 20 kHz. The excellent noise and distortion performance of the 5534-type operational amplifiers employed make this approach effective.



Total Harmonic Distortion (THD) as a Function of Level
Figure 11

To measure harmonic distortion, for example, a sensitive THD analyzer [11] with a 20-kHz measurement floor of about 0.001 percent was employed in combination with this distortion magnifier to achieve a residual of about 0.0003 percent at 20 kHz, primarily limited by noise of the power amplifier under test. The distortion output of the analyzer was then observed with both an oscilloscope and a spectrum analyzer.



20 kHz Total Harmonic Distortion (THD) Products at Full Power (50 W) a) without Error Correction (THD Analyzer Reads .02%); b) with Error Correction (THD Analyzer Reads .0006%).
Figure 12

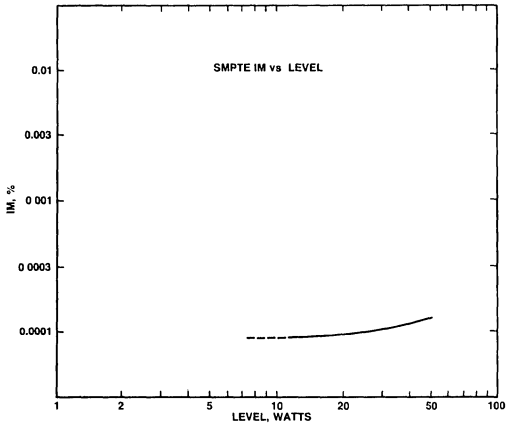
The latter further improves the measurement floor in most cases. Most of the other distortion tests employed a similar arrangement. Due to an oscilloscope calibration error, all vertical deflections in the photographs are 6.4 percent low.

Figures 10 and 11 show total harmonic distortion as a function of frequency and power. Dashed portions of the curves indicate that distortion is below the residual of the measuring system. Figure 12 shows the appearance of the 20-kHz full-power harmonic distortion products without and with output stage error correction. Figure 13 illustrates a virtually unmeasurable level of SMPTE* intermodulation distortion (60 & 6000 Hz, 4:1).

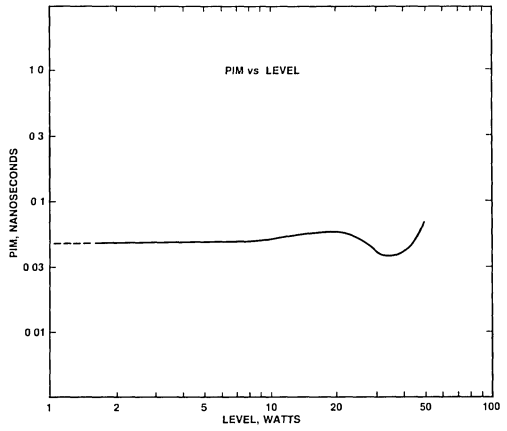
Dynamic intermodulation distortion (DIM), a test for measurement of transient intermodulation distortion (TIM), is shown in Figure 14. [12] In this test a 3.18-kHz square wave and a 15-kHz sinewave are mixed 4:1 and passed through the amplifier. A spectrum analyzer is used to measure the in-band intermodulation components. Performance is shown for both 30-kHz and 100-kHz first-order low-pass filtering of the square wave source (DIM-30 and DIM-100). As predicted by the good 20-kHz THD performance and high slew rate of this amplifier, both DIM-30 and DIM-100 distortion levels are very low; in fact, the former is unmeasurable.

Interface intermodulation distorion (IIM) [9] is measured by applying 1000 Hz to the amplifier under test

* Society of Motion Picture and Television Engineers.

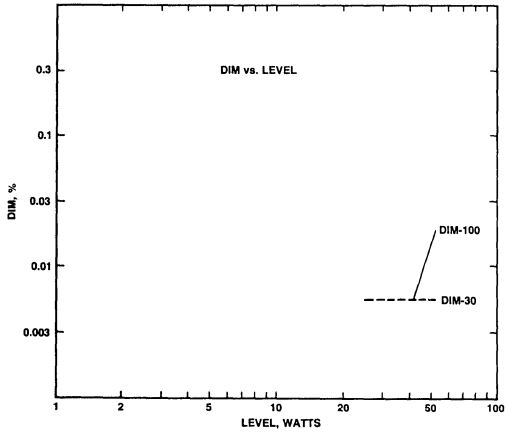


SMPTE Intermodulation Distortion as a Function of Level
Figure 13



Phase Intermodulation Distortion (PIM) as a Function of Level. Note that Phase Modulation is Expressed in rms nanoseconds.
Figure 15

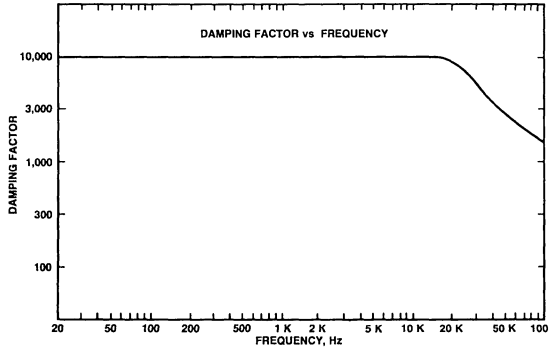
and 60 Hz to a test amplifier, each of which drives opposite ends of an 8-ohm load resistor. A spectrum analyzer is then used to measure distortion products at the output of the amplifier under test. Both amplifiers are operated at half the rated power of the amplifier under test and distortion products are referred to the 1-kHz level at the output of the amplifier under test. For this test the spectrum analyzer was preceded by a modified version of the distortion magnifier to produce a magnification of 100. IIM was unmeasurable, at less than 0.0001 percent.



Dynamic Intermodulation Distortion (DIM-30 and DIM-100) as a Function of Level
Figure 14

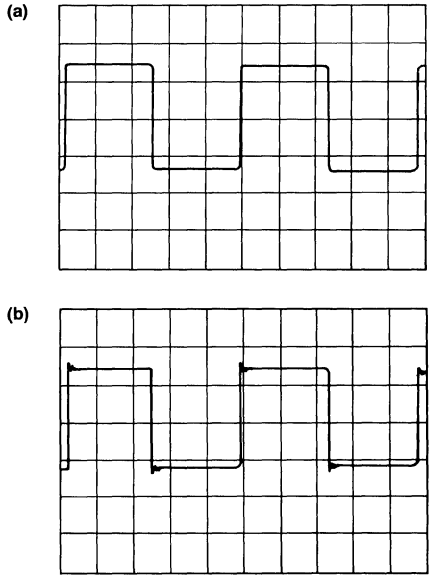
Phase intermodulation distortion (PIM) is shown in Figure 15. [10] PIM is measured in the same way as SMPTE-IM, except that phase modulation of the carrier is measured instead of amplitude modulation. The phase modulation is then expressed in time (e.g., rms nanoseconds).

Damping factor (DF) as a function of frequency is shown in Figure 16, and is extremely high. It is high for three reasons: 1) the power MOSFETS present very light loading to the drivers, producing a low open-loop output impedance essentially equal to the inverse of their transconductance; 2) the error correction circuit tends to drive this open-loop output impedance to zero; 3) substantial overall negative feedback further reduces the output impedance by an amount approximating the feedback factor (40 dB at 20 kHz). Inclusion of a parallel R-L network (0.5 Ω, 0.5 μH) at the output in series with the load for complete capacitive load stability will reduce the high-frequency damping factor to 125 at 20 kHz.



Damping Factor as a Function of Frequency
Figure 16

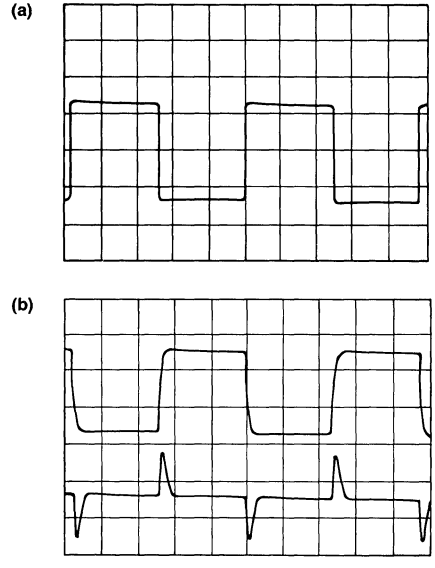
Although the need for this much damping factor is doubtful, the importance of DF on frequency response and coloration has sometimes been underestimated. This is explained by the fact that most speaker systems are designed assuming they will be driven by a pure voltage source (sometimes, it seems, with limitless



20 kHz Square Wave into an 8 Ohm Load; a) Small-Signal (1 V/div); b) Full Power (20 V/div)
Figure 17

current capability as well!). For example, the impedance of a nominal 4-ohm system may dip to 2.5 ohms and rise to over 50 ohms at various points across the frequency band due to driver and crossover resonances. A typical bipolar amplifier may have a damping factor of 100 (perhaps less at high frequencies), resulting in frequency response deviations on the order of 0.3 dB with such a load. Coloration due to low DF may also partly explain audible differences among vacuum-tube and low-feedback designs.

Figure 17 illustrates small-signal and full-power 20-kHz square waves into an 8-ohm load. Figure 18 shows small-signal and full-power 20-kHz square waves into a reactive load consisting of 1-ohm and 1 μF in series. In the full-power case the square wave has been band-limited to 200 kHz by a first-order low-pass filter. Figure 19 shows 500 kHz small-signal square waves into an 8-ohm resistive load and a reactive load consisting of 1-ohm and 1-μF in series. It also shows a full-power 500 kHz square wave into an 8-ohm load. Few bipolar amplifiers would survive this test.



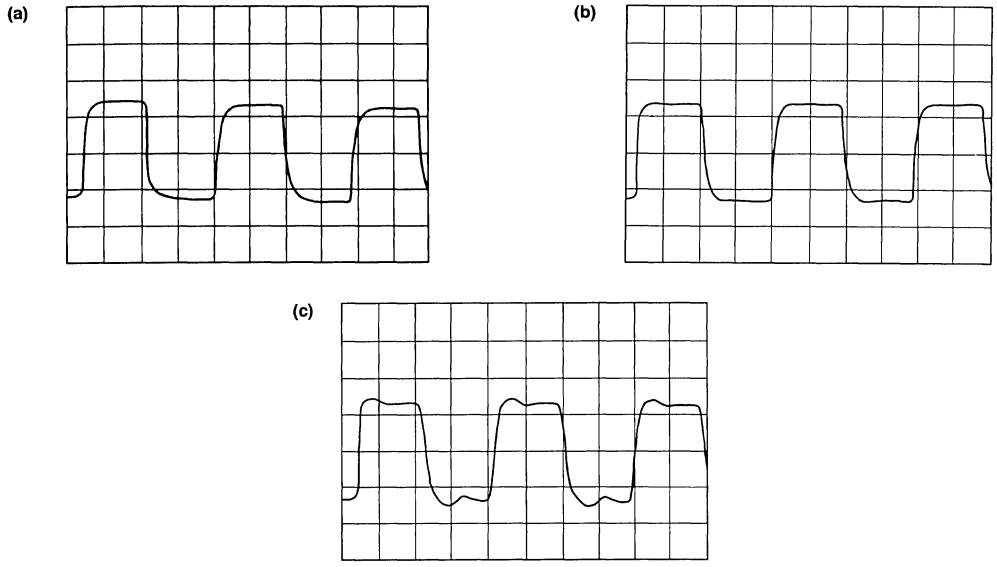
20 kHz Square Wave into a 1-Ohm Resistor in Series with a 1-Microfarad Capacitor; a) Small-Signal (1 V/div); b) Full-Power (Input Bandlimited to 200 kHz). Top Trace 20 V/div, Bottom Trace Is Output Current at 20 A/div. Timebase is 10 μs/div.
Figure 18

Table 1 summarizes overall performance of the amplifier.

Table 1
Summary of MOSFET Power Amplifier Performance

POWER OUTPUT (R_l = 8Ω)	50 W
TOTAL HARMONIC DISTORTION (20–20 kHz)	<0.001%
SMPTE IM DISTORTION	0.00013%
DYNAMIC INTERMODULATION DISTORTION (DIM-30) (DIM-100)	 <0.006%* 0.014%
INTERFACE INTERMODULATION DISTORTION (IIM)	0.0001%
PHASE INTERMODULATION DISTORTION (PIM)	<0.1 ns
SLEW RATE	>300 V/μs
RISE TIME	100 ns
DAMPING FACTOR (20–20 kHz)	>5000
S/N ("A" WTD, re 1 WATT)	108 dB

*Below Measurement Floor



500 kHz Square Wave Response; a) Small-Signal, 8-Ohm Load (1 V/div); b) Small-Signal 1-Ohm and 1-μF Series Load (1 V/div); c) Full-Power, 8-Ohm Load (20 V/div.). Timebase is 0.5 μs/div.
Figure 19

Conclusion

Power MOSFETs are capable of exceptional performance when used in combination with good drive circuitry and simple error correction circuitry. Their ability to operate without complex and unreliable safe-area limiting circuitry makes them especially useful for demanding audio applications. Compared with bipolar transistors, the major disadvantage of MOSFETs (and source of distortion) seems to be the lower transconductance, but this can be dealt with effectively by means of a simple error correction circuit. Although a MOSFET power amplifier can still be expected to cost a little more, the improved characteristics seem to justify the small premium in applications where performance is important.

Editors Note:

This paper is intended to illustrate design techniques and performance achievable, and not as a construction project.

References

[1] M. J. Hawksford, *"Distortion Correction in Audio Power Amplifiers,"* 65th Convention of the Audio Eng. Soc., preprint #1574, February 1980.

[2] International Rectifier HEXFET Databook, International Rectifier Corporation, Copyright 1981.

[3] T. Holman, *"New Factors in Power Amplifier Design,"* J. Audio Eng. Soc., Vol. 29, No. 7/8, pp. 517–522, July/August 1981.

[4] R. R. Cordell, *"Another View of TIM," Audio,* Vol. 64, Nos. 2 & 3, February and March 1980.

[5] W. G. Jung, M. L. Stephens, C. C. Todd, *"An Overview of SID and TIM," Audio,* Vol. 63, Nos. 6–8, June–August 1979.

[6] P. Garde, *"Transient Distortion in Feedback Amplifiers,"* J. Audio Eng. Soc., Vol. 26, No. 5, pp. 314–321, May 1978.

[7] E. M. Cherry, *"Transient Intermodulation Distortion; Part I–Hard Nonlinearity,"* IEEE Trans. Aconst., Speech, Sig. Proc., Vol. ASSP-29, pp. 137–146, April 1981.

[8] R. R. Cordell, *"A Fully In-band Multitone Test for Transient Intermodulation Distortion,"* J. Audio Eng. Soc., Vol. 29, No. 9, pp. 578–586.

[9] R. R. Cordell, *"Open-Loop Output Impedance and Interface Intermodulation Distortion in Audio Power Amplifiers,"* 64th Convention of the Audio Eng. Soc., preprint #1537, November 1979.

[10] R. R. Cordell, *"Phase Intermodulation Distortion-Instrumentation and Measurements,"* J. Audio Eng. Soc., Vol. 31, No. 3, pp. 114–124, March 1983.

[11] R. R. Cordell, *"Build a High-Performance THD Analyzer," Audio,* Vol. 65, Nos. 7–9, July–September 1981.

[12] E. Leinonen, M. Otala, J. Curl, *"A Method for Measuring Transient Intermodulation Distortion (TIM),"* J. Audio Eng. Soc., Vol. 25, No. 4, pp. 170–177, April 1977.