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phasing

Nowadays there are a great number of electronic sound effects. A favourite effect is 'Phasing' and in this article this is accomplished, somewhat unusually, by using a 'path filter'. This is a cheap alternative to the already well-known, charge-coupled analogue shift register or 'bucket brigade' memory.

Phasing occurs when a portion of a signal is delayed and then mixed with the original signal. In the middle of the audio spectrum delays of less than about 100 μs will produce no noticeable effect, whilst delays greater than about 30 ms will produce a distinct echo. A delay between these limits will give the required 'phasing' effect.

Of course, a fixed delay time will not have the same effect on signals of all frequencies. If, for example, a 1 kHz signal is delayed by exactly 1 ms and mixed at equal amplitude with the original, then the result will be a signal with twice the amplitude of the original, since the delayed signal has in fact been phase-shifted by 360°. For a 500 Hz signal, however, the situation is quite different. Here a 1 ms delay corresponds to a 180° phase shift, so if the delayed signal is mixed with the original signal the two will cancel, resulting in no signal. This cancellation will occur for all frequencies for which the delay time is an odd number of half-periods. For example with a delay time of 1 ms and a 1.5 kHz signal, the delayed signal is phase shifted by 540°, or 3 half cycles. At 2.5 kHz the delayed signal is phase shifted by 5 half-cycles.

As with the 1 kHz signal, all signals for which the delay time is an even number of half periods have their amplitude doubled. This is true for 2 kHz, 3 kHz, 4 kHz etc. The result is a series of peaks and nulls throughout the spectrum, as shown in figure 1. A circuit that produces this type of response is known as a 'comb filter', because of the unusual shape of the response curve.

Practical Realisation

Early attempts at phasing often used tape recorders running slightly out of synchronism, but this entails a number of difficulties, not least of which being that the sound is not 'live', and consequently the musician cannot adjust the sound during the performance.

There are numerous methods of achieving 'live' phasing.

Electrical delay lines are impractical for the relatively long delay times required. Electromechanical delay lines can be used to give the required delay, but their delay times are fixed by their mechanical dimensions. All-pass LC or RC phase-shift networks may also be used, but these have the disadvantage that the phase shift cannot easily be varied over a wide range. An obvious solution would be to use an analogue shift register such as the TCA590, but these devices are rather expensive.

A cheap alternative is the path filter, the principle of which is shown in figure 2. S1–S7 are closed and opened successively at a high rate, i.e. S1 is closed, then S2 is closed while S1 is opened, then S3 is closed while S2 is opened and so on. This cycle is repeated continuously. When a particular switch is closed, the associated capacitor can charge from the input voltage through the input resistor R. The voltage on each capacitor is dependent on the time constant RC (which is fixed if all the capacitors have the same value) the time for which each switch remains closed (which is also fixed) and the instantaneous level of the input signal.

It is therefore apparent that after a cycle of the switch sequence the voltages on the capacitors are a sample replica of the input waveform during that period (albeit slightly distorted due to the non-linear charging of the capacitors).

If successive cycles of the input waveform and the switching cycle occur in the same phase relationship, then the voltage on each capacitor will eventually become equal to the input voltage at a particular point along the waveform. No further charging of the capacitors will occur, and the input signal will be available at the output. This is true for the frequency at which one cycle of the input frequency is equal to the switching cycle time, and also for multiples of that frequency.

At other frequencies the signal is heavily attenuated. Consider what happens when a half-cycle of the input waveform is equal to the switch cycle time. Imagine that on the positive half-cycle the peak of the input waveform is stored on C4 in figure 2. During the negative half-cycle S4 will be closed at the trough of the waveform. The net voltage on C4 will be zero. This is true for the other capacitors, so the output signal is zero. This will also occur at all frequencies

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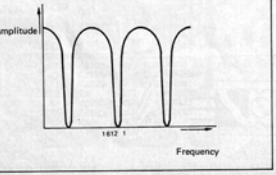

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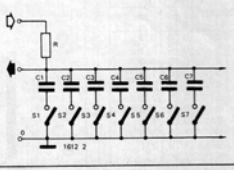


where an odd number of half-cycles is equal to the switch cycle time.
In practice, of course, the switching is accomplished electronically, for example by a ring counter. The result is a comb filter whose rejection frequencies can be varied by varying the clock frequency of the ring counter. The Q-factor can be altered by the single input resistor, R. Distortion of the output signal may be reduced by increasing the number of 'paths', i.e. the number of capacitors.
A practical realisation of a 40-path filter is shown in figure 3. A 7490 decade counter and a 7474 dual D-flip-flop form a divide-by-40 counter. The outputs of the 7474 are decoded by ten 7401 packages, each of which switches four capacitors, making 40 in all. The outputs of the 7490 are decoded by a 74141 BCD-to-decimal decoder/driver and used to switch the supplies to the 7401's via PNP transistors. The capacitors are thus arranged in a 4 x 10 matrix, and are switched as follows:
At the start of a cycle the outputs of the 7474 are all '0' so the capacitors connected to pin 4 of each 7401 are switched in sequence as the 7490 counts from 0 to 9 and the supplies to each 7401 package are switched in turn. When the count reaches 10 output E of the 7474 becomes '1'.
The capacitors connected to pin 13 of the 7401's are switched as the 7490 counts the second decade, and so on. The Q-control is provided by the 50 k potentiometer. The signal source must have a low output impedance and the output of the filter must be connected to a high impedance load.

Applications

This filter has a very narrow bandwidth, with the Q-control at maximum typically less than a semitone. Various effects can be obtained with the circuit. If a narrow pulse waveform is fed in, chimes or percussion effects can be produced at the output, depending on the control frequency. Aircraft noises and other engine noises can also be simulated by filtering out harmonics of complex tones.
The phasing effect occurs when a clock frequency is used which is higher than the upper limit of the audio spectrum (say 20 to 100 kHz). The Q-control must be set in a fairly high position.
The path filter may also be used with an electronic organ or synthesizer, to produce strange effects. A particularly unusual sound can be obtained by feeding the clock input of the filter from the signal outputs of an electronic organ (squarewave outputs from dividers, before filtering) and by feeding a noise signal into the signal input. The results are, to say the least, unlike any organ in existence.
The circuit as described does have its limitations. It will not operate effectively below the frequency whose half-cycle is the same length as the counter cycle. Lowering the clock frequency to compensate for this introduces problems with noise due to the clock frequency and the switching of the supplies to the 7401's. This is aggravated by differences in the characteristics of the 7401's and of the transistors. Increasing the number of stages so that a higher clock frequency may be used will overcome many of these problems.

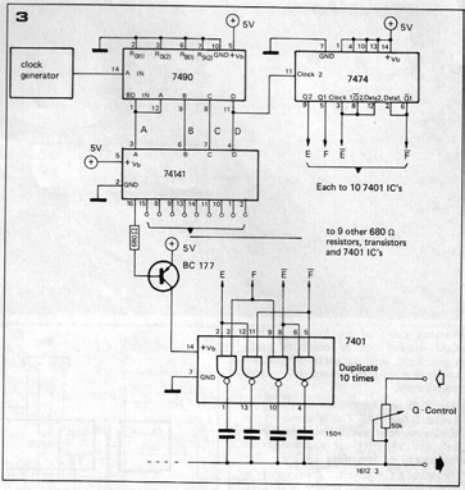
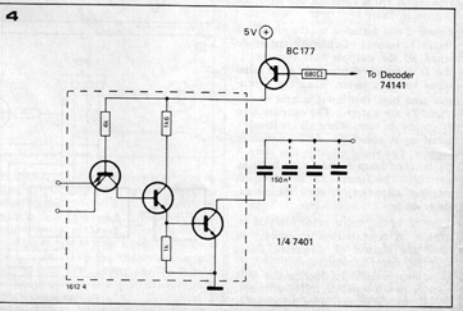


Figure 1. Frequency response of a comb filter. Frequencies phase-shifted by odd multiples of 180° are almost completely rejected.

Figure 2. Principle of a path filter. All capacitors have the same value and the number of capacitors may be optionally increased almost indefinitely.

Figure 3. Circuit for a practical path filter. The 7401 and the associated supply switching transistor are duplicated 10 times. Each 7401 is connected to the outputs of the 7474 as shown.

Figure 4. Showing the internal circuitry of one gate in a 7401 package, and how each capacitor is connected.



disco lights

Various kinds of psychedelic flashing light display can be generated easily using logic shift registers. Several circuits are discussed here of varying complexity.

The shift register chosen for this application is the 7495. This is a four-bit parallel/serial load, parallel/serial out, shift-left, shift right register, and was chosen because of its versatility.

The circuit for generating a type of display commonly used is given in figure 1. Four lamps light in sequence until all are lit, then all are extinguished simultaneously. The circuit operates as follows: The outputs A to D of the shift register are initially at '0' so the mode control input (pin 6) is low. In this mode serial data is entered at pin 1 and is shifted one place right on each clock pulse. Since the serial input is held high by the 1 k resistor, outputs A to D successively go high until all are high. When output D goes high the mode control goes high with it and the shift register is now in the parallel load, shift left mode. The parallel inputs A to D are grounded so that '0's are entered and subsequently appear on the outputs. The cycle then repeats. A truth table for the sequence is given in Table 1.

Figure 2 is a variation on the circuit of figure 1. Instead of changing the mode when all the outputs have become '1' the D output is connected to the serial input via an inverter. When the D output goes high this input is held low so that '0's are entered. The outputs A to D go low in turn. When all are low the serial input goes high and the sequence repeats. The visual effect is that lamp A lights, then lamp B and so on until all are lit. The lamps then extinguish starting with lamp A until all are extinguished.

Table 2 is the truth table for this sequence. A reset button is provided to clear the register of unwanted states that may occur at switch-on.

It is also possible to operate the shift register in the serial in, shift left mode. To do this it is necessary to connect

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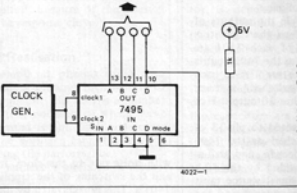

Table 1

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	0	0	0

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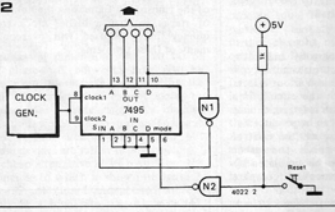


Table 2

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

3

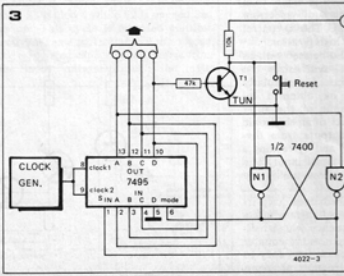


Table 3

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0
8	0	0	0	0

Figures 1-5. These five basic circuits show the versatility of the 7495. Each circuit gives a different output sequence.

Tables 1-5. These tables show the output sequences of the corresponding circuits

Figure 6. One way of isolating the control circuitry from the triac is to use transformers. The input to this circuit is TTL compatible.

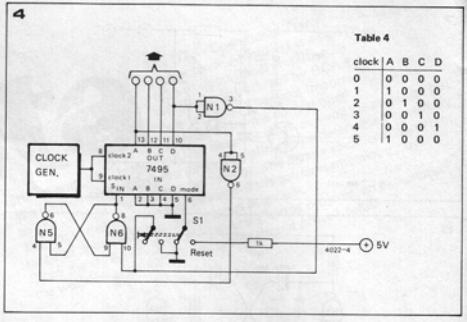


Table 4

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

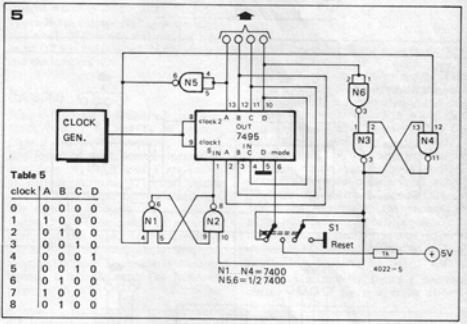
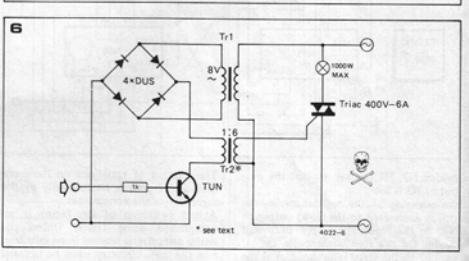


Table 5

clock	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	1	0
6	0	1	0	0
7	1	0	0	0
8	0	1	0	0



each output to the preceding input (D to C, C to B, B to A). Serial data is then entered at the D input and is shifted left on each clock pulse.

This may be used to make a display where the lamps light in the order A to D, then extinguish in the order D to A, as in figure 3. This circuit operates as follows: the flip-flop N1, N2 is initially set so that the serial input is high and the mode control is low.

'1's are thus entered at the serial input and appear successively at the outputs A to D. When output D becomes high T1 is turned on and the flip-flop is reset. The mode control input becomes '1', reversing the shift direction. Since the D input is grounded the data entered is '0', so the outputs go low starting with the D output. When all the outputs are low the flip-flop is set and the sequence repeats. The truth table is given in table 3.

The circuits so far discussed are similar in that after four clock pulses all lamps are lit. It is, however a simple matter to devise a circuit where the lamps light in sequence but only one at a time, by circulating a single '1' through the shift register.

In the circuit of figure 4 the lamps light in the sequence A to D, with only one lamp at a time being lit. When lamp D extinguishes lamp A lights and the sequence repeats (table 4). The circuit operates as follows: on switching on the A to D outputs will set randomly so that more than one output may be high. This would mean that a number of '1's would be circulating, whereas only a single '1' is required. For this reason a reset button is provided. When S1 is depressed the flip-flop comprising N5 and N6 is set, taking the serial input high. At the same time the mode control is taken high by the other half of S1, so that on the next clock pulse the register shifts the '0's from the grounded A to D inputs to the corresponding outputs, clearing the register.

When the switch is released the register is in the serial-in, shift right mode, so on the next clock pulse the '1' present on the serial input will appear at output A. The output of N2 will go low, resetting the flip-flop N5, N6 so that the serial input is low. On each successive clock pulse the '1' on the A output is shifted one place to the right until it appears at output D. When this occurs the output of N1 goes low, setting the flip-flop. A '1' now appears at the serial input, and the process repeats.

Figure 5 shows a variation on this circuit, in which a '1' travels back and forth from one end of the register to the other (table 5). The circuit is initially reset by pressing S1. This sets the flip-flop N1, N2 so that a '1' appears at the serial input. It also puts the register in the shift-left mode, so that the '0' on the grounded D input is shifted left, clearing the register. The flip-flop com-

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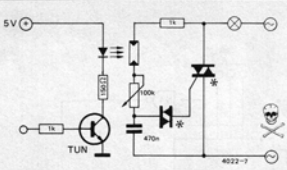

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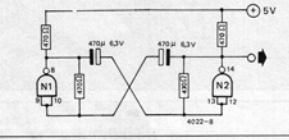

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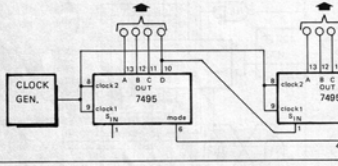

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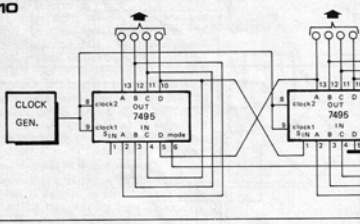

Figure 7. A more elegant solution is to use opto-isolation.

Figure 8. Two NAND gates (or inverters) can be connected as an astable multivibrator. This provides a simple clock generator circuit to drive the 7495.

Figure 9. If four outputs are considered insufficient, circuits 1, 2 and 4 can be extended ad infinitum in this way.

Figure 10. Circuits 3 and 5 can also be readily extended to give any number of additional outputs.

prising N3, N4 is reset, so that the output of N3 is low.

On releasing S1 the register mode control is connected to the (low) output of N3, so the register is in the shift-right mode. On the first clock pulse the '1' applied to the serial input appears at the A output. It is inverted and resets the flip-flop N1, N2 so that no more '1's are entered. The '1' which is in the register is shifted right on each successive clock pulse until it reaches the D output. Flip-flop N3, N4 is then set, reversing the shift direction. When the '1' again reaches the A output flip-flop N3, N4 is reset and the shift direction again reverses, and so on.

The number of variations on these circuits is, of course, limited only by the ingenuity of the constructor.

Actual switching of the lamps is accomplished using triacs. Unless the entire circuitry is housed in an insulated box the logic circuitry must be isolated from the mains. This may be accomplished by either transformer or optical isolation of the control circuitry from the triac, and suitable circuits are given in figures 6 and 7.

In figure 6 the secondary voltage of Tr1 is full-wave rectified and applied to the collector of the transistor via the primary of Tr2. When the transistor is turned on by one of the outputs of the register, current flows through the primary of Tr2 and the current induced in the secondary triggers the triac. The choice of transformers is not critical. Tr1 can be a small bell transformer, whilst Tr2 should have a ratio of about 1 : 6 and can be a miniature type since only a small current flows through it. Of course Tr1 and the bridge rectifier are required only once in the circuit, but the transistor, Tr2 and the triac must be repeated for every output from the shift register. With this circuit triggering of the triac is not optimum. Phasing of the transformers is important, so if the circuit does not work first time reverse the polarity of one of the windings.

A more elegant solution is to use opto-isolation, as in the circuit of figure 7. This is simply a conventional triac dimmer with the main potentiometer replaced by a light-dependent resistor housed in a light-tight enclosure with a LED. When the transistor is turned on by an output of the shift register the LED lights and the illumination causes the resistance of the LDR to fall. The triggering point of the triac is thus advanced and the lamp lights.

The base current of the transistor in both these circuits is about 3 mA, so they can easily be driven by the outputs of the shift register. The choice of diac and triac for both these switches depends on the maximum load to be switched.

A simple clock generator circuit is given in figure 8. This is simply two NAND-gates or inverters connected as an astable multivibrator. A variable frequency pulse generator could also be used so that the travelling speed of the light pattern could be altered. Figures 9 and 10 show how the discolights may be extended with several shift registers. Figure 9 is intended for extension of figures 1, 2, and 4, and figure 10 for the extension of figures 3 and 5.