Audio Delay-line SYSTEMS AND CIRCUITS PART 4

by Ray Marston

Ray Marston looks at the Holtek HT8955A low-cost digital delay line IC in the final installment of this 4-part series.

Earlier episodes of this 4-part series explained audio delay line basic principles, described the operation of modern analogue 'bucket brigade' delay line (BBD) ICs, presented a selection of practical BBD analogue delay line circuits, and explained the operation of modern digital delay line systems. This month's episode rounds off the series by explaining the operation of the Holtek HT8955A low-cost digital delay line IC and showing some practical ways of using the device.

The Holtek HT8955A Delay Line IC

The Holtek HT8955A is a low-cost but fairly sophisticated 24-pin IC that, when used in conjunction with an external dynamic RAM, acts as a complete 10-bit digital delay line system that – when operated at a 25kHz sampling clock rate – can generate delays of up to 200ms when using a 64k-bit DRAM or 800ms when using a 256k-bit DRAM. The IC is a CMOS type designed to operate from 5V supply lines, and incorporates a 10-bit ADC, 10-bit DAC and full control and DRAM-interfacing circuitry, plus a built-in analogue pre-amplifier. The device is intended for use in popular applications such as cheap voice echo units, low-cost Karaoke systems, and simple sound effects generators, etc.

Figures 1, 2 and Table 1 show the internal block diagram of the HT8955A, together with its outline and pin notation details, and Table 2 lists its claimed basic operating specification.

Note in Table 2, that the manufacturer's claims regarding the unit's S/N ratio and THD are in fact suspiciously optimistic for a mere 10-bit unit, and may not be attained in reality. In actual fact, the HT8955A functions as an excellent 'cheapo' delay line IC that gives exactly the kind of performance that would be expected from such a unit. Its output signals are noisy and badly distorted, but its range of delay times is excellent. In short, the IC offers an excellent low-cost introduction to the practicalities of modern digital delay line usage. The IC's basic operation is as follows:

The HT8955A has two built-in oscillators, a 'fast' one (controlled via pins 6 and 7) that controls – via the unit's timebase generator – the main ADC and DAC circuitry, and a 'slow' one (controlled via pins 8 and 9) that controls the system's Address register and thus exercises control over the delay line's actual delay time. The IC's analogue input signals are applied to the built-in pre-amplifier via pin 2 and are then passed on to the IC's ADC, which sequentially samples them and converts each sample into a 10-bit digital word, which is made available – when required – in serial form on a bidirectional data bus connected to pin 21, ready to be passed on to the external dynamic RAM (DRAM). The stored 10-bit data words of the DRAM are – when required – accessed (via a shift register) by the IC's DAC via the pin 21 data bus and are then made available, in time-delayed analogue form, on pin 4 of the IC.

The most complex part of the HT8955A IC is the section that controls the flow of data bits to and from the external DRAM. Each one of these individual bits (from the IC's ADC or to its DAC) is clocked into (or from) a unique address in the DRAM via the

Pin No.	Pin Name	Description
1	BIAS	Bias of internal pre-amp; connect to decoupler 'C'
2	IN	Audio signal input pin (inverting) to pre-amp
3	PREO	Pre-amp output pin
4	OUT	Delayed audio signal (from DAC) output pin
5	SEL	Delay-time select pin (open = 64k-bit DRAM size, +5V = 256k-bit DRAM size)
6	OSC1	'Fast' system oscillator input (timing) pin
7	OSC2	'Fast' system oscillator output (timing) pin
8	OSC3	'Slow' delay time oscillator input (timing) pin
9	OSC4	'Slow' delay time oscillator output (timing) pin
10	GND	Power supply ground (0V)
11	A6	Connect to external DRAM 'A6' Address pin
12	A7	Connect to external DRAM 'A7' Address pin
13	A5	Connect to external DRAM 'A5' Address pin
14	A4	Connect to external DRAM 'A4' Address pin
15	A3	Connect to external DRAM 'A3' Address pin
16	A2	Connect to external DRAM 'A2' Address pin
17	A1	Connect to external DRAM 'A1' Address pin
18	A0	Connect to external DRAM 'A0' Address pin
19	RASB	Connect to external DRAM 'RASB' Control pin
20	WRB	Connect to external DRAM 'WRB' Control pin
21	DATA	Data I/O pin to and from the external DRAM
22	A8	Connect to external DRAM 'A8' Address pin
23	CASB	Connect to external DRAM 'CASB' Control pin
24	+5V	Connect to positive (+5V) supply rail

Table 1. Table listing the HT8955A's pin descriptions.

Characteristic	Test Condition	Min.	Typ.	Max.	Unit
Operating voltage	–	4·5	5·0	5·5	V
Operating current	No load	–	2·5	8·0	mA
Pre-amp open-loop voltage gain (Av)	RL > 100kΩ	–	2,000	–	V/V
Input voltage range, with +5V supply	–	1·5	–	3·5	V
Maximum output volts	RL > 470kΩ	1·0	1·5	–	V
Maximum delay time, with 64k-bit DRAM	SEL = o/c 25kHz sampling	150	200	–	ms
Maximum delay time, with 256k-bit DRAM	SEL = +5V 25kHz sampling	600	800	–	ms
Signal-to-noise (S/N) ratio	Vout = 1V @ 400Hz, Bandwidth = 10kHz	–	55	–	dB
Total harmonic distortion (THD)	Vout = 1V @ 400Hz, Bandwidth = 7kHz	–	0·5	–	%

Table 2. Table detailing the basic working specification of the HT8955A IC.

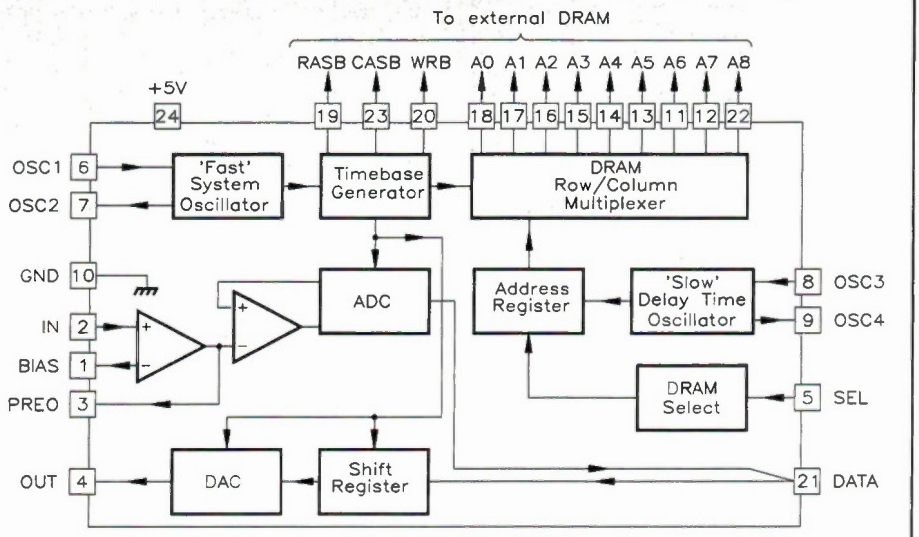


Figure 1. Functional block diagram of the Holtek HT8955A digital delay line IC.

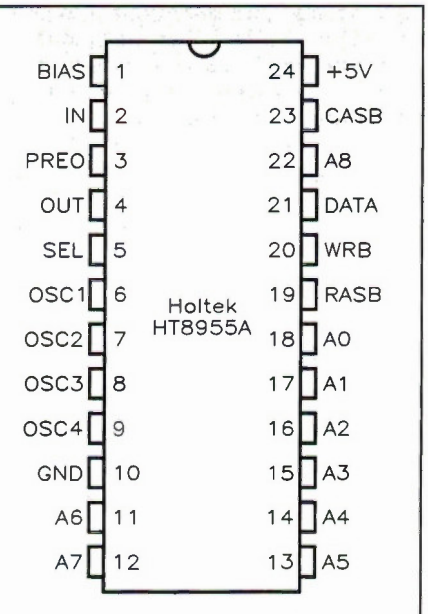


Figure 2. Outline and pin notations of the HT8955A IC.

IC's Address register and Row/Column Multiplexer, which can select any one of up to 262,144 addresses in a 256k-bit DRAM. This operation requires the use of an 18-bit address code, and this is applied to the DRAM in the form of one 9-bit (A0 to A8) row word (controlled via the Row Address Select or 'RASB' pin) followed by one 9-bit (A0 to A8) column word (controlled via the Column Address Select or 'CASB' pin). The direction of the data flow (to or from the DRAM) is controlled via the IC's Write/Read or 'WRB' pin. The actual data (from the ADC or to the DAC) takes the form of a 10-bit word that flows from or to the pin-21 DATA terminal of the HT8955A in serial form (one bit at a time). Each one of these 10-bit words thus occupies a 'field' of 10-bits of DRAM space.

Thus, in each 'slow' operating cycle of the HT8955A, the IC goes through the following operating sequence. First, it executes an ADC conversion operation, then opens up a new 10-bit DRAM field and accesses each individual part of its 10-bit data word, sequentially transferring each existing bit to the IC's DAC and replacing it with a corresponding new bit from the ADC. At the end of the sequence, the 'old' 10-bit data word has appeared in time-delayed analogue form at the IC's pin-4 output terminal, and has been replaced in the DRAM field with a new 10-bit data word derived from the IC's pin-2 analogue input terminal. The IC then moves on to the next operating sequence, during which it carries out similar operations on the DRAM's next multi-bit data field, and so on.

Basic Usage Data

The Holtek HT8955A is designed to be very easy to use, and is specifically intended for use with 4164 (64k-bit) or 41256 (256k-bit) dynamic RAM ICs. These ICs are 16-pin types, with very similar pin functions, as shown in Figures 3 & 4, which show the normal pin notations modified to conform with those used on the HT8955A IC. The only significant difference between the two DRAMs – from the user's point of view – is that the 41256 uses a basic 9-bit (A0 to A8) address system, with the A8 bit going to pin-1, and the 4164 uses a basic 8-bit (A0 to A7) address system, with the IC's pin-1 terminal internally unconnected. These facts enable the HT8955A and either type of DRAM to be used in the 'universal' basic delay-line circuit of Figure 5.

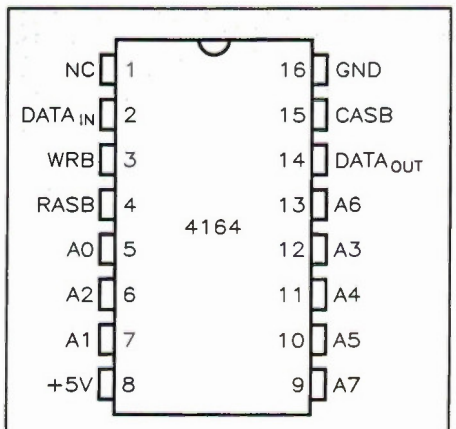


Figure 3. Outline and pin notations of the 4164 64k-bit dynamic RAM IC.

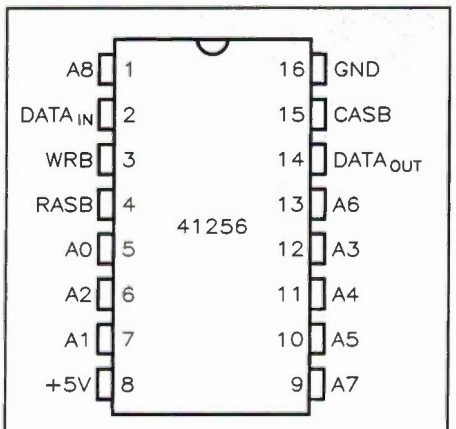


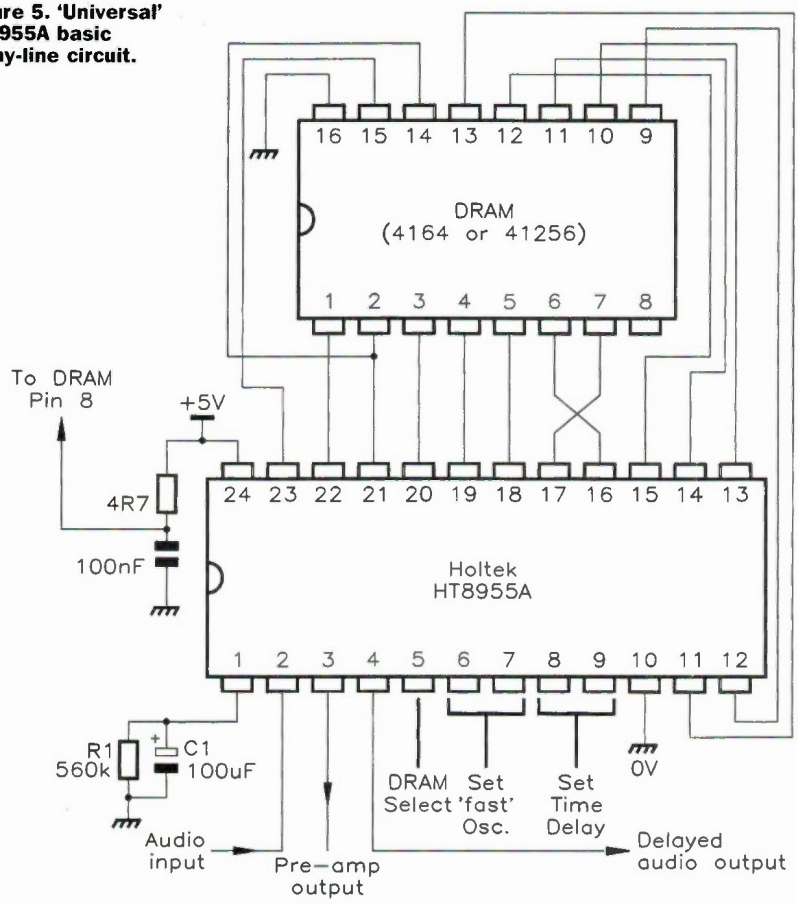
Figure 4. Outline and pin notations of the 41256 256k-bit dynamic RAM IC.

The basic Figure 5 circuit must be powered from a well-regulated 5V supply, and consumes up to 45mA when used with a 4164 DRAM or up to 70mA with a 41256 DRAM. If a 4164 DRAM is used, pin-5 of the HT8955A must be left unused, and if a 41256 DRAM is used, pin-5 must be tied to ground. To use this basic circuit in practical applications, the user must first connect pin-5 in the appropriate mode, connect a resistor between pins 6 & 7 to set the IC's 'fast' oscillator frequency, and connect a fixed and a variable resistor between pins 8 & 9 to set the desired 'delay' time of the system. C1 is used to decouple the internal pre-amp's built-in bias network, and R1 is an optional biasing resistor who's function is explained in the next few paragraphs. To use the pre-amp, an appropriate feedback network must be connected between pins 2 and 3 (the pre-amp's input and output pins), and an audio input signal applied to pin 2 will then produce a time-delayed audio output signal on pin 4.

The best way to learn about the HT8955A is to use it in a simple test circuit, and Figure 6 shows the connections needed to make the 'universal' HT8955A circuit act as a basic test unit that uses a 64k-bit (4164) DRAM, and Figure 7 shows the alternative connections for use with a 256k-bit (41256) DRAM. Note in these circuits, that the pin 6-7 resistor sets the frequency of the IC's 'fast' oscillator, the pin 8-9 components control the 'slow' oscillator, and the pin 5 connection selects '64k-bit' or '256k-bit' DRAM operation. In both cases, the IC's internal pre-amp is used as an audio amplifier that gives ×2 voltage gain and has its upper roll-off frequency set at 5kHz by the 100kΩ//330pF pin 2-3 R and C component values; the roll-off frequency is inversely proportional to the C value, and can be doubled by reducing the C value to 165pF.

To use the Figure 6 & 7 circuits, simply connect an audio signal (from an A.F. signal generator or from an entertainment source) to the circuit's input and then monitor (with an oscilloscope or a Hi-Fi system) the circuit's three audio output points, first at the pin-3 pre-amp output, then at the pin-4 'Delay OUT' point, and finally at the 'Delay output' point at the junction of the 10kΩ resistor and 3n3F capacitor. During these tests, increase the input signal amplitude until clipping occurs on the Delay output, then see if the performance can be improved significantly by fitting various

Figure 5. 'Universal' HT8955A basic delay-line circuit.



values (not less than 100kΩ) of R1 between pin-1 and either ground or the +5V supply rail. During these tests, you will probably note that the delay outputs are rather noisy and have a very limited useful dynamic range, and that the performance can be adversely affected by poor circuit layout.

When you have finished with the Figure 6 or 7 test circuits, you can move on and convert them into simple low-cost echo/reverb units by using the basic connections shown in Figure 8. This particular diagram shows the connections for use with a 256k-bit (41256) DRAM, but those for use with a 64k-bit (4164) DRAM are very similar. In both cases, the IC's internal pre-amp is used as a 1st-order low-pass filter with a 5kHz break frequency, and also as an audio mixer that gives ×2 voltage gain to the audio input signal and a ×0·17 to ×1·2 voltage gain to a 'reverb' feedback signal from the delay line's pin-4 output. Consequently, the output of the pre-amp consists of the original audio input signal plus 'reverberating echo' signals from the delay line output, and is made available via a 20kΩ volume control. The echo/reverb sounds are particularly impressive when used with voice inputs. Figure 9 shows a simplified equivalent functional diagram of the low-cost echo/reverb circuit, together with its basic waveforms.

Figures 10 to 12 shows three useful ancillary circuits that can be used in conjunction with any HT8955A delay line system. The Figure 10 circuit is that of a simple voltage regulator that can be used to supply the IC's +5V

Figure 6. The 'universal' HT8955A circuit wired as a basic test unit with a 64k-bit (4164) DRAM.

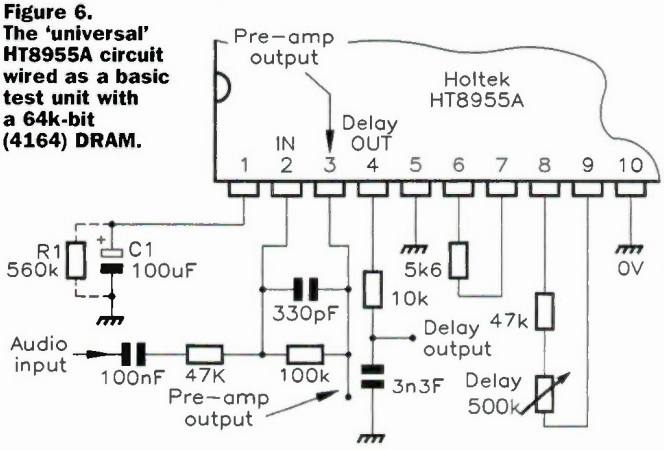


Figure 7. The 'universal' HT8955A circuit wired as a basic test unit with a 256k-bit (41256) DRAM.

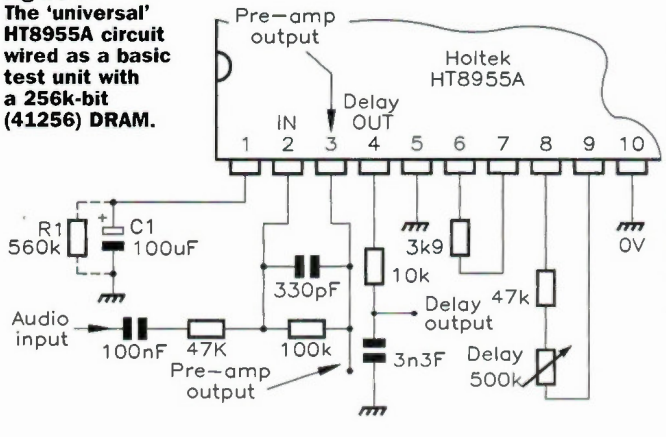


Figure 8. The 'universal' HT8955A circuit adapted as a low-cost echo/reverb unit with a 256k-bit (41256) DRAM.

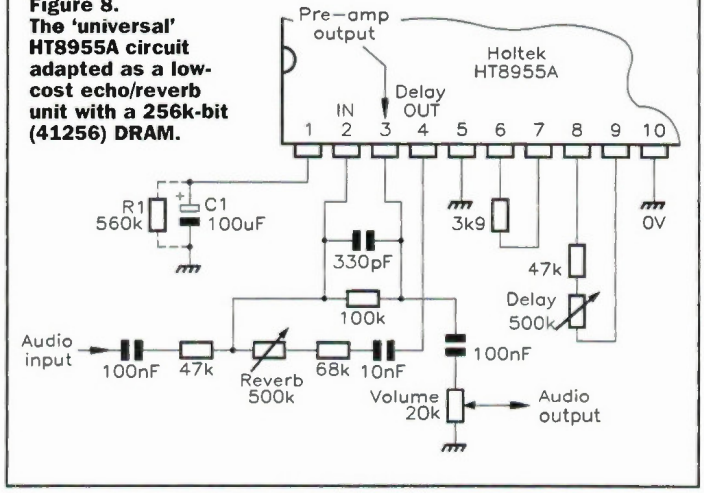
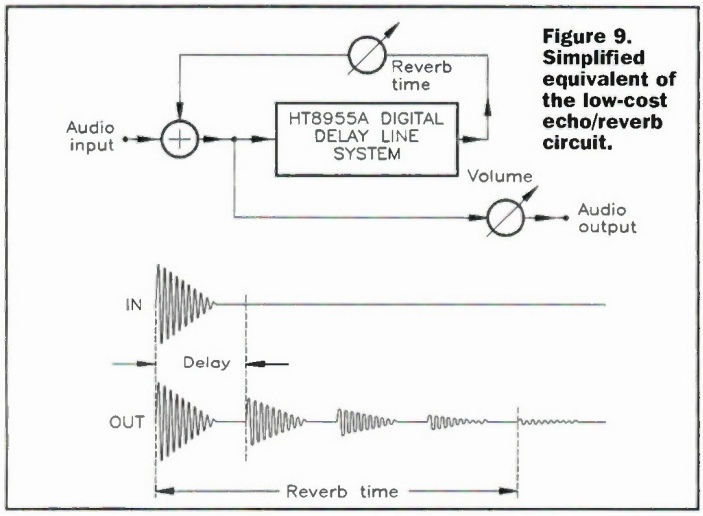


Figure 9. Simplified equivalent of the low-cost echo/reverb circuit.



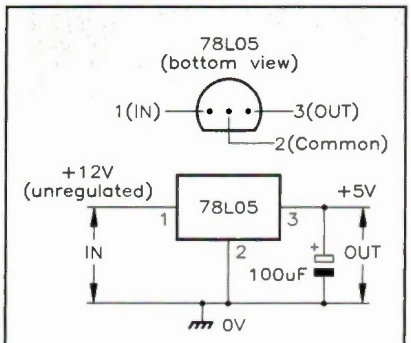


Figure 10. Simple +5V, 0-100mA regulated power supply circuit.

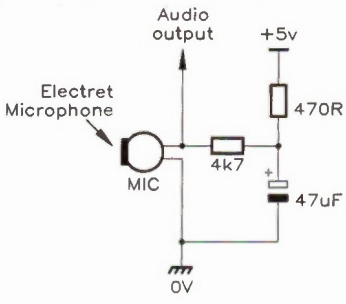


Figure 11. Way of powering an electret microphone from the +5V supply.

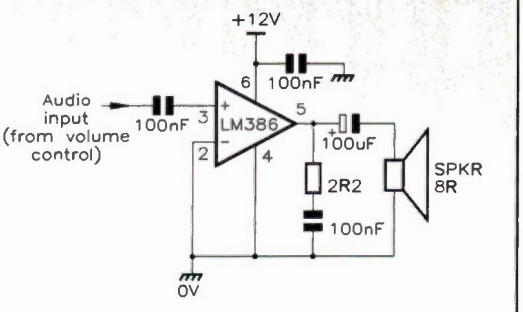


Figure 12. Low-cost power amplifier that can generate several hundred milliwatts in an 8Ω speaker.

regulated supply (at load currents up to 100mA); the circuit is powered from an unregulated input of about +12V, and is designed around a 78L05 IC that is housed in a 3-pin TO-92 plastic package and normally uses the pin connections shown in the diagram. Note, however, that a few manufacturer's versions of this IC have their IN and OUT connections reversed, so if this circuit fails to work, try swapping the IC's IN and OUT connections.

Figure 11 shows a simple way of connecting an electret microphone directly to the input of the Figure 8 circuit and powering it from the circuit's +5V supply. This type of microphone has a built-in FET amplifier, and in the diagram, the 4k7Ω resistor is used as the FET's drain load, thus making the microphone's output directly available.

Finally, Figure 12 shows a simple low-cost power amplifier that can be powered from an unregulated +12V supply (which is also used for powering the HT8955A system's +5V voltage regulator) and can be driven directly from the delay-line's volume control, and which can generate an output of several hundred milliwatts in an 8Ω speaker. The IC used is an LM386 type, which is housed in an 8-pin plastic package.

A Karaoke Circuit

A major application area of the HT8955A is in simple Karaoke systems, in which the voices of one or more amateur singers are fed through an echo-reverb unit and are mixed with an unmodified music signal. To conclude this look at the HT8955A delay-line IC, Figure 13 shows how the 'universal' HT8955A circuit of Figure 5 can be adapted as a low-cost Karaoke unit with a 256k-bit (41256) DRAM, and Figure 14 shows – in block diagram form – the Karaoke unit's equivalent circuit.

The Karaoke unit can accept voice inputs from two dynamic (moving coil) microphones, plus a single 'line input' music signal. Each microphone input has its own volume control, and the outputs of these are mixed together in IC1, which gives a ×100 voltage gain to low-frequency signals; the 68pF capacitor wired across the 470kΩ resistor causes the gain to fall off at a 6dB/octave rate above 5kHz. IC1's output is tapped off in two directions; one output signal is fed to the input of the HT8955A's pre-amp, where it is mixed with part of the delay line's output to give a 'reverb' effect, and the other is fed to the input of IC2, where it is mixed with 'line input' music signal and with a fraction of the delay line's output to give a final composite audio output signal.

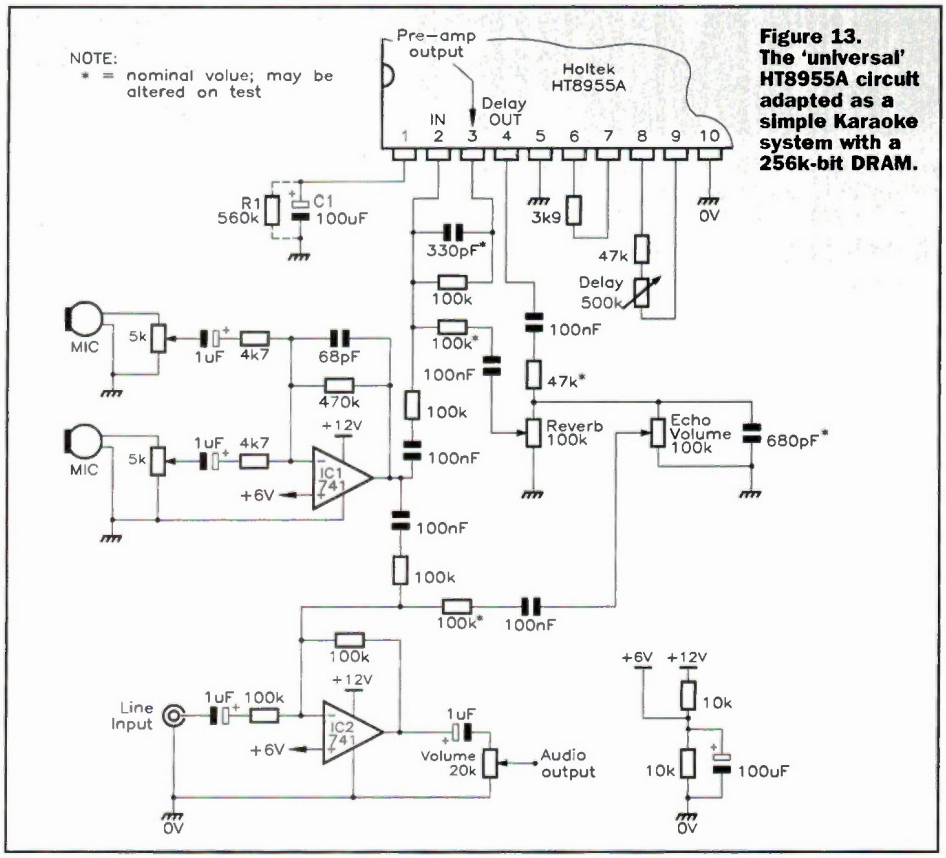


Figure 13. The 'universal' HT8955A circuit adapted as a simple Karaoke system with a 256k-bit DRAM.

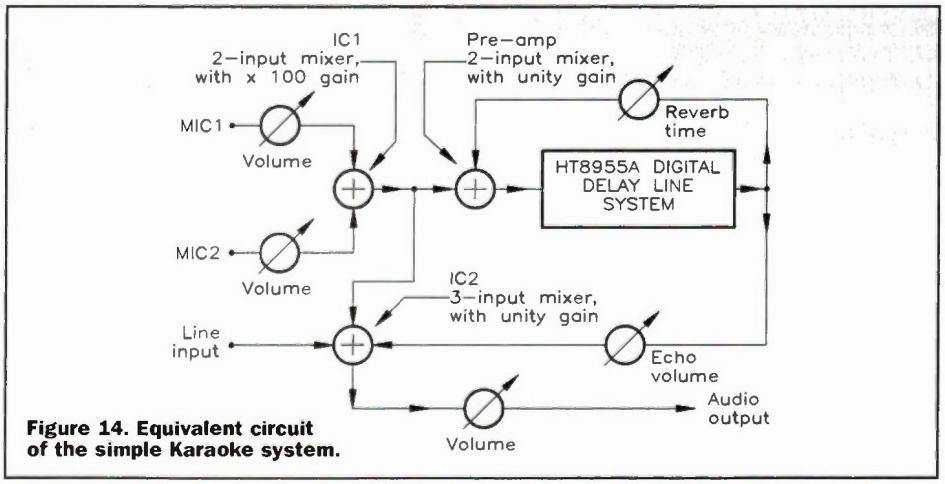


Figure 14. Equivalent circuit of the simple Karaoke system.

Note in Figure 13, that the non-inverting input pin of each 741 op-amp is biased at half of the op-amps +12V supply voltage via a decoupled divider made of two 10kΩ resistors. Also note that the values of the components marked with an asterisk (*) may be altered on test to give a modified circuit performance, to suit individual preferences. Thus, the values of the three marked resistors affect the voltage gain in various parts of the circuit, and the values of the two marked capacitors affect the frequency response. The circuit thus offers plenty of scope for experiment. ELECTRONICS