

IEEE 1394 LINK Layer Controller (MD8412)

General Descriptions

The MD8412 is a link layer controller for high-speed serial buses, designed in accordance with the IEEE draft standard, IEEE 1394 - 1995. It involves all necessary functions for the link layer, and also functions to relieve the burden of the system for isochronous transfer. Therefore, it is suitable for being incorporated in equipment on the side of peripheral terminals.

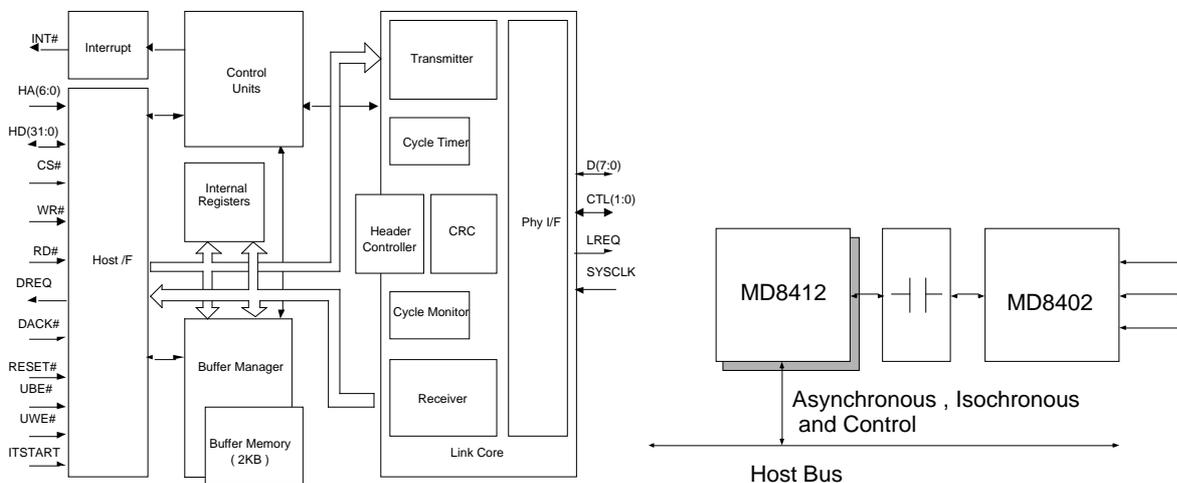
Features

- Packing for transmission and unpacking for reception, according to IEEE 1394 - 1995
- Cycle master support
- Parity generation and error detection by 32-bit CRC
- Detection of dropped cycle start messages
- Support of both AC and DC coupling connections with PHY Interface
- 3-speed support of 100/200/400Mb/sec.
- Control of the No. of transfers in each cycle during isochronous transfer
- Automatic insertion of a header in isochronous packet during transmission and automatic header separation and routing during reception
- Support of outbound retry sequence
- Feasibility of selecting a host-bus width from 8/16/32-bit, enabling easy connection with a general-purpose MPU/microcomputer
- Support of both big and little-endians during selection of host bus 16/32-bit
- Support of control signals toward LPS (Link Power Status) of PHY (MD8402)

Applications

- Digital camera
- Electronic musical instruments
- Various storages
- Digital VTR
- Scanner
- Digital audio
- Printer

Internal block diagram



Package Outline

100 pin LQFP

Power Voltage

5.0 volts

Functional outlines

Host interface

The host interface is composed of asynchronous buses in a width of SRAM-style 8/16/32-bit. Since DMA control support functions are provided inside, DREQ signals can be generated according to the state of a buffer, enabling high-speed data transfer.

Bus width changeover of 8/16/32 can be controlled by a signal of UWE#, UBE#, A1, or A0. It is possible to change register and buffer access operation. All registers can be directly accessed from the host. In DMA transfer, internal buffer selection is effected to enable gaining access to the selected buffer.

PHY interface

An interface is available, which enables direct connection with the PHY chip to process a physical layer according to IEEE 1394 1995. Either 100Mbps or 200Mbps is acceptable for the PHY chip to be connected.

In the IEEE1394 Draft, the connection mode for the PHY and LINK chips is classified to the following two kinds:

- DC connection
- AC connection

This IC supports both kinds of connections.

Transmitter

The transmitter reads out data from an asynchronous transmission buffer or an isochronous transmission buffer in the MD8412, and sends out a PHY interface packet through formatting into each packet format defined by IEEE 1394 - 1995. If the cycle master bit is '1' and the node using the MD8412 is a route, then a cycle start packet is also sent out to indicate the head of the isochronous cycle.

Receiver

The receiver receives a packet from the PHY interface and identifies if this packet is the one to be acquired by the node of MD8412. If it is found as an asynchronous packet, it is identified with a node address of MD8412. If it is an isochronous packet, it is identified with a preset channel number. If a packet is headed to this node, routing is effected toward the asynchronous reception buffer or the isochronous reception buffer by writing the data therein. For a broadcast packet and the snoop mode, no judgment is effected and data are written in their buffer.

Built-in buffer

The MD8412 incorporates a buffer in 512 x 32(bit) configuration with a capacity of 2K-byte in total. This is a temporary buffer intended for data rate absorption between transmitter and host bus. The host performs data access to this buffer.

The MD8412 controls this buffer by dividing it into a maximum of 4 areas. Two of the divided areas are used at random for asynchronous transmission and reception. The remaining two areas depend on isochronous modal setting. Each buffer size is designated at the register. Status information, such as full or empty in the buffer, can be known at the host in the divided unit.

Isochronous transfer functions

The MD8412 possesses isochronous functions. It incorporates a cycle timer so that a cycle start packet can be transmitted in the unit of 125 μ sec when the node seizing the MD8412 is of the cycle master. Its trigger is an 8KHz signal entered through the CYCLEIN pin, obtained as a result of generation of a clock signal of 49.152MHz, coming from the PHY chip.

When the above-mentioned node is not of the cycle master, synchronism with the cycle master is secured through compensation of the cycle master within the MD8412, based on the value of that packet, each time a cycle start packet is received from another cycle master node.

The MD8412 is provided with two types of isochronous modes. One is a mode intended to gain access to the host with a packet image. The other is a mode for host access with an image of data stream.

The user determines the mode, according to the nature of data source to be handled in the isochronous transfer mode.