



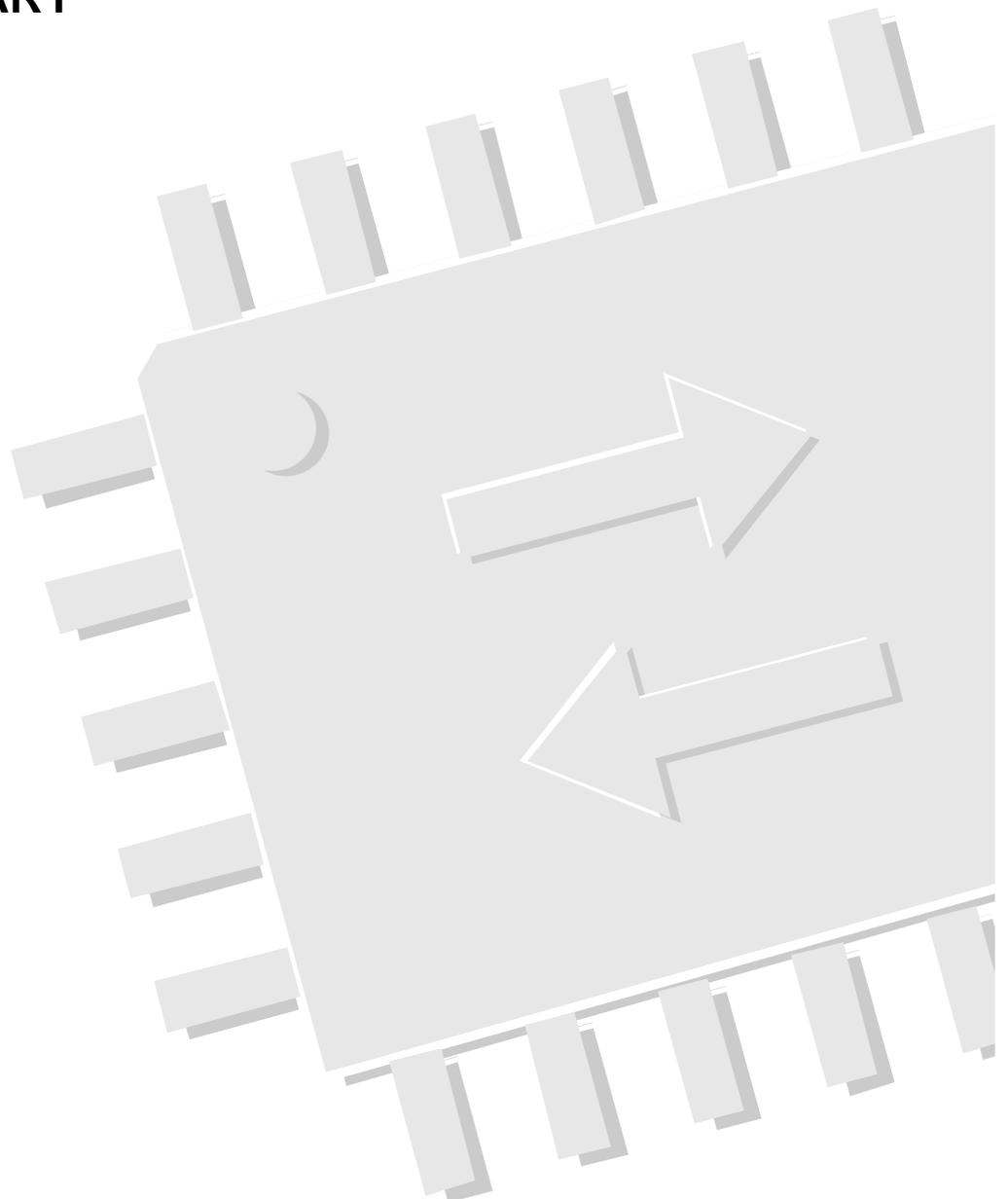
FUJIFILM MICRODEVICES CO., LTD.

# LINK (IEEE 1394)

## MD8430

User's Manual

**PRELIMINARY**



## Revice History

rev. No.	date	comment
0.91	1998/10/20	First revision of English manual

## explanatory notes

MSB/LSB	: Left MSB / Right LSB	
Negative Logic	: # is added at last of the signal name.	
Description of numeric	: The Binary	****b or ****
	The Decimal	****
	The Hexadecimal	****h or 0x****
Description of table	: Hatched and No named area is reserved. These reserved bits should be 0.	
Glossary	: Byte	8 bit data
	Word	16 bit data
	Quadlet	32 bit data
	Octlet	64 bit data

## Related Documents

IEEE P1394 Draft 8.0v1 Standard for a High Performance Serial Bus  
 IEEE Std 1212-1991 Command and Status Register architecture

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## 1 Introduction

The MD8430 is a link-layer controller of the high-speed serial bus, conforming to IEEE draft standard 1394-1995. The isochronous packet offers maximum transfer performance by gaining access to the outside through an exclusive bus. In addition to the various functions necessary for the link layer, the MD8430 is provided with the responder processing functions for the transaction layer. Therefore, it is capable of automatic transmission of a response packet for the request packet.

The internal register reads out the serial ROM for automatic setting. As a result, it is possible to make processing without any intervention of the host CPU in the case of applications that call for response transactions only.

### 1.1 Features

- Packing during transmission and unpacking during reception, conforming to IEEE1394-1995.
- Cycle Master support.
- Parity generation by 32-bit CRC and error detection.
- Detection of a dropped cycle start message.
- DC and AC connections supported by the PHY-chip nterface.
- Controlling the number of transfer actions in each cycle during isochronous transfer.
- Automatic insertion of a header during isochronous packet transmission, and automatic separation of a header during reception.
- Full support of retry protocol.
- Exclusive data bus for isochronous transmission and reception.
- Supporting the bus time register.
- Enabling the connection with a PHY chip of 100, 200, or 400M/bps.
- Automatic transmission of a response packet in regard to the request packet.
- Automatic setting up of an internal register by the serial ROM.
- Function of SelfID packet analysis.
- DMA controller incorporated for send/receive data transfer, to be performed in conjunction with responder processing.
- Responder transactions processed without the host CPU.

### 1.2 Applications

Digital camera                      Printer                                      Scanner  
Other devices to be controlled

1.3 Internal Block Diagram

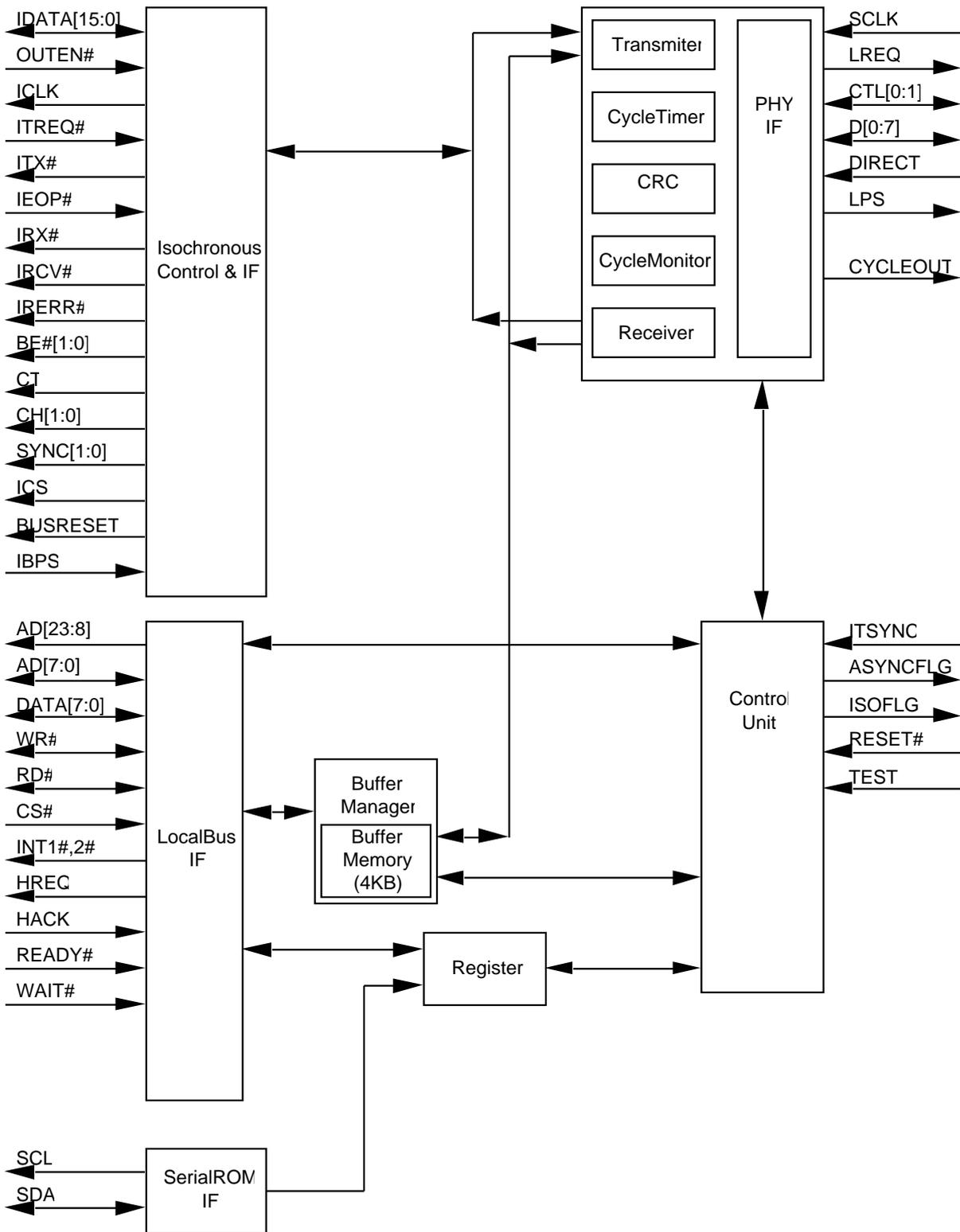


Figure 1.3.1 Internal block diagram

## 1.4 Operation Mode

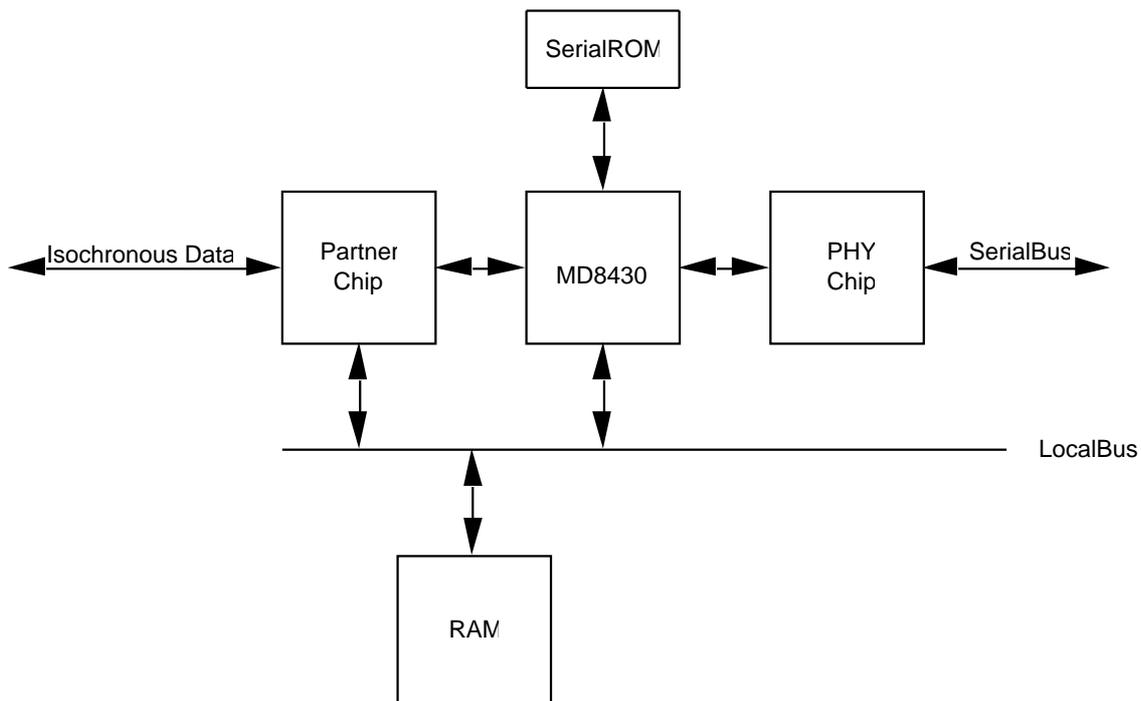


Figure 1.4.2 Operation without Host CPU (Support by Responder only)

## 1.5 Outline Functions

### 1.5.1 Serial ROM interface

This is an interface for a 2-wire type serial ROM (MN24C16FM8 by Fairchild, Inc., or equivalent). It is used to store information to set up the register in the MD8430 and also information about the ROM area in the CSR space. The serial ROM is read after hardware reset in order to set up the register in the MD8430.

### 1.5.2 Local Bus Interface

The local bus is operated in the two types of operation modes, the idle cycle and the DMA cycle.

#### 1) Idle cycle

The local bus is generally operated in the mode of idle cycle. This mode is used to gain access to a register in the MD8430. The interface is composed of an 8-bit SRAM-like asynchronous bus. Data access is effected by the Big Endian system.

#### 2) DMA cycle

The MD8430 uses its internal DMA controller to transfer send/receive data in conjunction with Responder processing. At that time, the local bus operates in the mode of DMA cycle. The address generated by the DMA controller consists of 24 bits. The MD8430 asks the host CPU for bus release. After the host CPU has confirmed the release of the bus, data exchange is effected with a device over the local bus by DMA transfer.

After the completion of DMA transfer, the local bus is released and the idle cycle is recovered.

Data access is effected by the Big Endian system.

### 1.5.3 Responder Transaction

A response packet is automatically transmitted in response to the received request packet. Its operation differs according to the type of the received packet.

#### 1) Reception of read request and lock request

Response data are DMA-transferred from a device on the local bus to the MD8430, and the response packet is automatically transmitted to the serial bus.

#### 2) Write request reception

A response packet is automatically transmitted to the serial bus. Pay load of the received packet is DMA-transferred to the device on the local bus.

### 1.5.4 Requester Transaction

This LSI can not handle requester transactions.

### 1.5.5 SelfID Analysis

The node numbers of the root node and the isochronous\_resource\_manager node is detected by analyzing the received Self\_ID packet, and the detected numbers are set in the register.

### 1.5.6 PHY Interface

There is an interface intended to enable direct coupling with the PHY chip that processes the physical layer in accordance with the IEEE1394 Standard. The PHY chip used for the connection is of 100, 200, or 400Mbps.

In the IEEE1394 Draft, the following two types of connection modes are defined for the PHY and LINK chips:

- DC connection
- AC connection

In this IC, both connection modes are supported.

### 1.5.7 Transmitter

The transmitter reads out data from the asynchronous transmission buffer in the MD8430, or from the isochronous transmission data bus. The read data are arranged into various packet formats defined in IEEE1394. The formatted packets are sent to the PHY interface. When the CycleMaster bit is 1 and the node using the MD8430 is root, a CycleMaster packet for showing the head of the isochronous cycle is sent out.

### 1.5.8 Receiver

The receiver receives a packet from the PHY interface and identifies whether the received packet is the one to be acquired. If it is found to be an asynchronous packet, this judgment is made with the node address of the MD8430. If it is an isochronous packet, such a judgment is conducted with the preset channel number. When the packet is found to be addressed to this node, writing is effected in the asynchronous reception buffer and data output is performed toward the isochronous data bus.

No judgment is conducted in the case of a broadcast packet and the snoop mode. In this case, writing is effected in the asynchronous reception buffer and data output is performed toward the isochronous data bus.

### 1.5.9 Built-in Buffer

The MD8430 incorporates two buffers in 512 (word) x 32 (bit)+20 x 32(bit) configuration with a total capacity of 2128bytes. Each buffer is used for the asynchronous transmission and reception. This buffer is a temporary buffer used to absorb the data rate between the transmitter/receiver and the host bus.

### 1.5.10 Isochronous Transfer Function

The MD8430 is provided with isochronous functions. It incorporates a cycle timer. When the node using the MD8430 is of the CycleMaster, it is possible to transmit a CycleStart packet in the unit of 125msec. The trigger to be used may be produced from the 49.152MHz clock input from the PHY chip, or an 8kHz signal input from the CYCLEIN pin may be used. If the node is not for the CycleMaster, synchronism with the CycleMaster is secured by making compensation for the internal CycleTimer of the MD8430, each time a CycleStart packet is received from another CycleStart node, using the value in that packet.

The MD8430 has two types of isochronous modes, an access mode by the host using a packet image and another access mode using an image of data itself. (Details described later) The user may be required to determine the mode according to the nature of data source handled in the isochronous transfer mode. For the isochronous packet access in conjunction with the outside, synchronous transfer is conducted by use of an exclusive isochronous data bus. Data control with the outside in that case is carried out by the MD8430 functioning as the master.

1.6 Transmission/Reception Data Flow

Fig. 1.6.1 and Fig. 1.6.2 show the data flows to be observed during Responder processing.

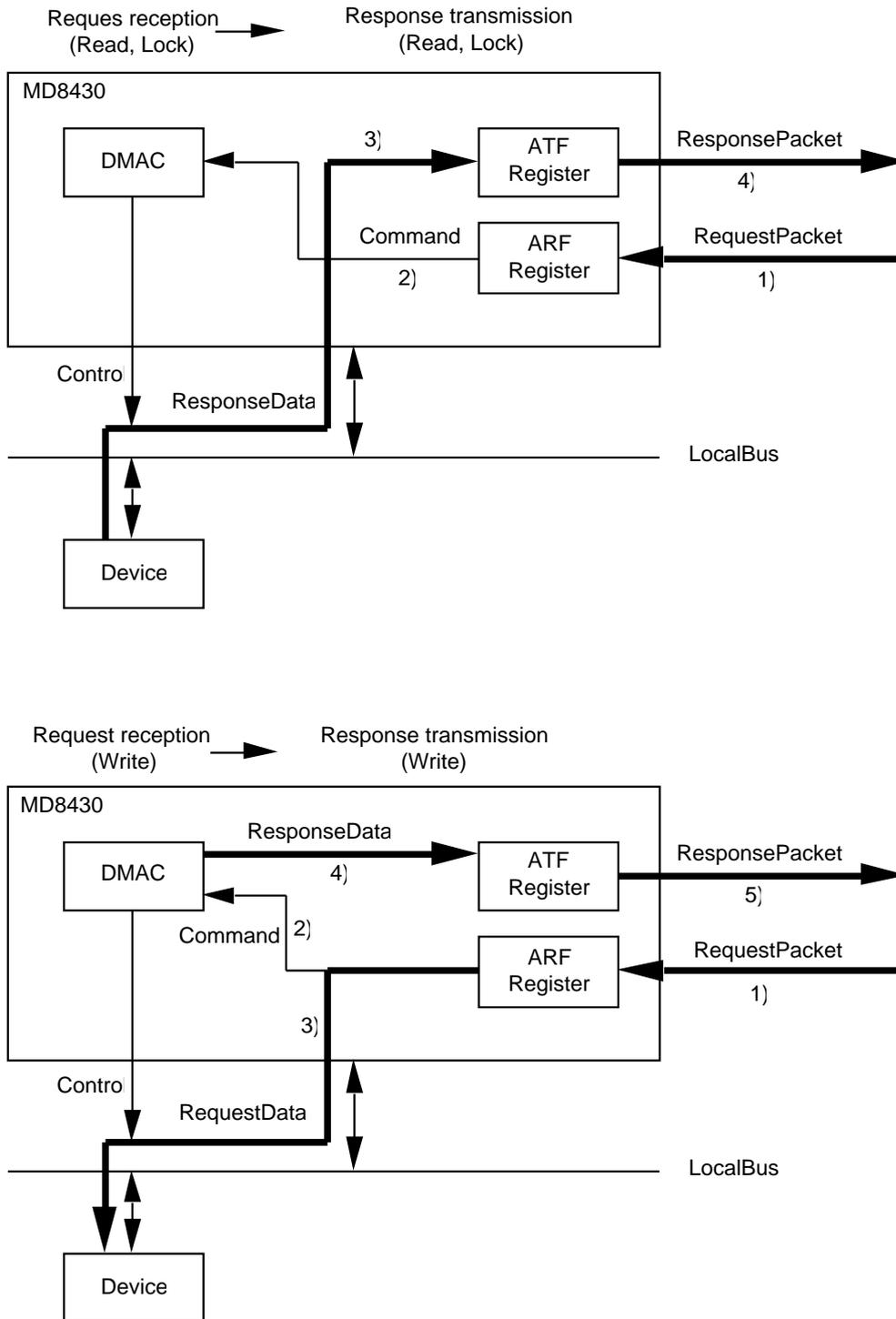
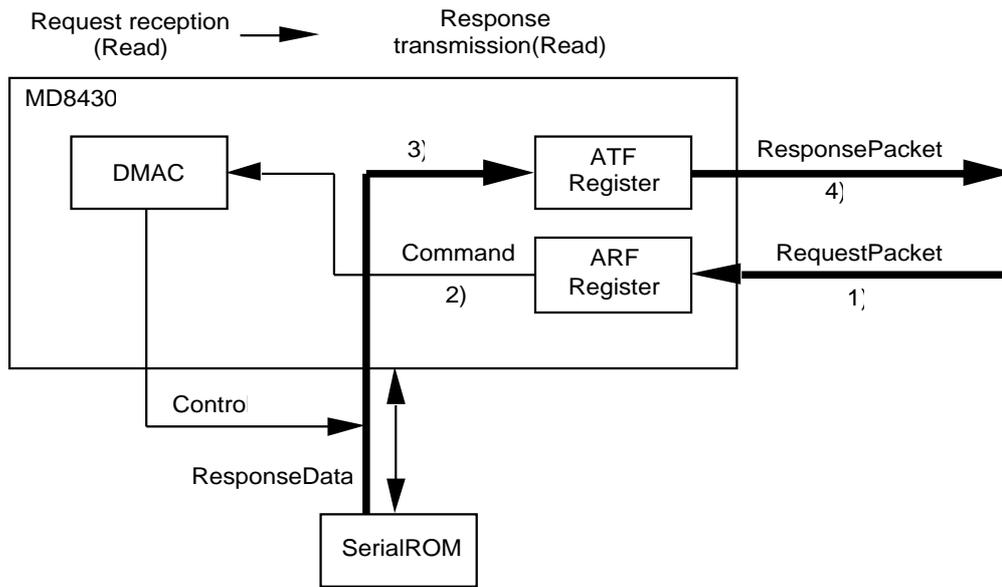


Figure 1.6.1 Data Flow during Responder Processing (Access to the Local Bus)



SerialROM reagon is Read Only.

MD8430 returns a Responce Packet of Type\_Error for Write, Lock Request to this region.

Figure 1.6.1 Data Flow during Responder Processing (Access to Serial ROM)

## 2 I/O Terminal Descriptions

Table 2.1 I/O Terminals

Signal name	Type	Pin No.	No. of Pins	Contents															
PHY Interface																			
SCLK	I	90	1	Master clock: A clock signal of 49.152MHz supplied from the PHY chip. The MD8430 uses this clock as a master clock signal. Usually connected to this signal pin of the PHY chip.															
LREQ	O	92	1	Link request: Used for register access in the PHY chip and when making a request to use a serial bus. Usually connected to this signal pin of the PHY chip.															
CTL[0:1]	I/O	88, 87	2	An interface control signal toward the PHY chip. Usually connected to this signal pin of the PHY chip.															
D[0:7]	I/O	85, 84, 82, 81, 79, 78, 76, 75	8	PHY-LINK data bus. This is a data bus for data transmission and reception with the PHY chip. D[0:1] is used for packet transmission and reception at 100Mbps, D[0:3] at 200Mbps, and D[0:7] at 400Mbps.															
DIREC	I	95	1	PHY I/F select signal: A selection signal to determine whether a connection with the PHY should be made in the DC or AC mode. 0 : AC connection 1 : DC connection															
LPS	O	94	1	Link power status: An LPS signal toward the PHY. According to the register setting, an output is generated in any of the following combinations. <table border="1" data-bbox="715 1010 1310 1283"> <thead> <tr> <th>DIREC Pin</th> <th>LPSOn bit</th> <th>LPS output</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Clock Out about 2MHz</td> </tr> </tbody> </table>	DIREC Pin	LPSOn bit	LPS output	1	0	0	1	1	1	0	0	0	0	1	Clock Out about 2MHz
DIREC Pin	LPSOn bit	LPS output																	
1	0	0																	
1	1	1																	
0	0	0																	
0	1	Clock Out about 2MHz																	
SerialROM Interface																			
SCL	O	100	1	Serial ROM clock: A clock output is generated for serial ROM access. A CLK signal is frequency-divided to obtain an output. The frequency division ratio is selected at the DIV terminal.															
SDA	I/O	101	1	Serial ROM data I/O: A data I/O terminal toward the Serial ROM.															

Table 2.1 I/O Terminals(Cont.)

Signal name	Type	Pin No.	No. of Pins	Contents
Local data bus				
AD[23:8]	O	3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 17, 18, 19, 20	16	Local address: DMA cycle: A local address output is generated.
AD[7:0]	I/O	21, 22, 24, 25, 26, 27, 28, 29	8	Local address: Idle cycle: An address for internal register selection. DMA cycle: A local address output is generated.
DATA[7:0]	I/O	116, 115, 114, 113, 111, 110, 109, 108	8	Local data bus: Idle cycle: A data bus for internal register access. DMA cycle: A bus for transfer.
WR#	I/O	128	1	Write enable: Idle cycle: Asserted when writing in the internal register. DMA cycle: A write signal is output to the objective device for DMA transfer.
RD#	I/O	1	1	Read enable: Idle cycle: Asserted when reading from the internal register. DMA cycle: A read signal is output to the objective device for DMA transfer.
CS#	I	127	1	Chip select: A chip select signal for the MD8430.
HREQ	O	124	1	Bus hold request: Bus release is requested to the host CPU.
HACK	I	123	1	Bus hold acknowledge: Indicates that the host CPU has accepted HREQ and released the bus.
READY#	I	121	1	DMA transfer ready: Asserted when DMA transfer is possible. DMA transfer is not performed when it is negated.
WAIT#	I	120	1	DMA transfer wait: While it is asserted, the duration of WR# and RD# output is extended.
INT1#	O	118	1	Interrupt signal 1: An interrupt signal used for notification to the host. When a request arises in the interrupt register, this signal is asserted. The selection of this request can be set up with the register.
INT2#	O	119	1	Interrupt signal 2: An interrupt signal used for notification to the host. When a request arises in the interrupt register, this signal is asserted. The selection of this request can be set up with the register.

Table 2.1 I/O Terminals(Cont.)

Signal name	Type	Pin No.	No. of Pins	Contents
Isochronous bus interface				
ICLK	O	43	1	Isochronous bus master clock: A master clock for each isochronous interface signal to be output by the MD8430. An output of 24.576MHz is generated to count the cycle timer from the outside.
ITREQ#	I	66	1	Isochronous transmission request: This signal is asserted when the outside makes a transmission request for an isochronous packet. It is kept asserted during the transmission of multiple packets in a certain isochronous cycle. Once it is negated, however, the packets caused thereafter are identified as a transmission request for the next cycle.
ITX#	O	64	1	Isochronous transmission data enable: If there is a transmission request, the MD8430 uses this signal to accomplish this data request from the outside. The outside is required to handle these data, without fail, in synchronization with this signal.
IEOP#	I	65	1	Isochronous transmission packet last data signal: With the last data (at 16 bits) of a packet during transmission, this signal is asserted from the outside in synchronization with ITX#. The MD8430 uses this signal to identify the last data of each packet.
IRX#	O	41	1	Isochronous reception data enable: If there is a packet received from the PHY, the MD8430 generates a packet data output on the IDATA bus in synchronization with this signal.
IRCV#	O	40	1	Isochronous packet reception enable: Indicates that the received packet is output on the IDATA bus.
IRERR#	O	39	1	Isochronous packet error flag: Asserted in the case of a CRC or data error in the received isochronous packet.
IDATA [15:0]	I/O	45, 46, 47, 48, 49, 51, 52, 53, 54, 56, 57, 58, 59, 61, 62, 63	16	Isochronous data bus: An exclusive bus for isochronous data access. The CycleTimer value in the CycleStart packet is also output from this bus.
CH[1:0]	O	31, 32	2	Isochronous reception packet channel status: While the isochronous reception packet is output, a channel identification number of that packet is output.
CT	O	67	1	CycleTimer enable: Indicates that the CycleTimer value in the packet is output on the IDATA bus while the CycleStart packet is transmitted in the root mode or received in the non-root mode.
BE#[1:0]	O	33, 34	2	Byte enable: Indicates that the effective data of isochronous reception are output, to the upper 8 bits and the lower 8 bits of the IDATA bus, respectively. BE#[1] denotes IDATA[15:8] and BE#[0] denotes IDATA[7:0].
OUTEN	I	42	1	ISO bus enable signal: The IDATA bus assumes the output condition during data reception while enable and IRCV# of this signal are asserted.
SYN [1:0]	O	36, 37	2	In the case of coincidence with the value that has been set with the Sync bit in the received isochronous packet, the following codes are output: 01: Coincidence with StartSync 10: Coincidence with StopSync 11: Between Start and Stop 00: Other than the above

Table 2.1 I/O Terminals(Cont.)

Signal name	Type	Pin No.	No. of Pins	Contents
BUSRESET	O	38	1	When BusReset occurs, a pulse of 25MHz is output.
ICS	O	68	1	A timing output is generated during transmission or reception of the CycleStart packet.
Others				
CYCLEOUT	O	72	1	IsoCycle output: This is a CycleClock output generated by counting with the CycleTimer in the MD8430.
ITSYNC	I	97	1	Sync control signal/ Iso transmission control: This is a transmission control signal for auto-mode transmission or for sync field setting in the header during auto-mode transmission.
IBPS	I	98	1	Isochronous bus format changeover: Used to select an I/O format of the isochronous bus. (L: MD8414 mode, H: 400Mbps mode)
ASYNCFI	O	71	1	Asynchronous flag: Asserted when an asynchronous packet is transmitted to the PHY or an asynchronous packet is received from the PHY. It is effective as a trigger signal for packet transmission or reception.
ISOFLG	O	70	1	Isochronous flag: Asserted when an isochronous packet is transmitted to the PHY or an isochronous packet is received from the PHY. It is effective as a trigger signal for packet transmission or reception.
RESET#	I	96	1	Reset: A system reset signal for the MD8430.
Test				
TEST[6:0]	I	102,103 104,105, 106,107, 126	7	Used to set up the MD8430 in the test mode. It is usually opened.
Power supply				
Vdd		9, 23, 35, 50, 60, 74, 80, 86, 91, 99, 112, 122,125	13	3.3V Power supply.
Vss		2, 16, 30, 44, 55, 69, 73, 77, 83, 89, 93, 117	12	GND

Please fill 0 for all reserved bits(drown mesh). MD8430 can not work correctly if all reserved bit are not 0.  
Some registers does not have an initial value. It means the register is set by Config ROM.

### 3 Control Registers

#### 3.1 Version Register

##### 3.1.1 Version Register

address 00h

Initial value set at shipment

This register indicates the version number of the MD8430. It is effective in controlling the IEEE 1394-LINK chip with software in the future.

7	6	5	4	3	2	1	0
Version[15:8]							

Bit 7-0 Version[15:8]: Version number (RO, Initial value: 00h)

##### 3.1.2 Version Register

address 01h

Initial value set at shipment

7	6	5	4	3	2	1	0
Version[7:0]							

Bit 7-0 Version[7:0]: Version number (RO, Initial value: 03h)

### 3.2 Revision Registers

#### 3.2.1 Revision Register

address 02h

Initial value set at shipment

This register indicates the revision number of the MD8430. The value begins with 0 and increases each time revision is made. It is effective in controlling the IEEE 1394-LINK chip with software in the future.

7	6	5	4	3	2	1	0
Revision[15:8]							

Bit 7-0 Revision[15:8]: Revision number (RO, Initial value: set at shipment)

## 3.2.2 Revision Register

address 03h  
Initial value set at shipment

7	6	5	4	3	2	1	0
Revision[7:0]							

Bit 7-0 Revision [7:0]: Revision number (RO, Initial value: set at shipment)

## 3.3 Control Registers

## 3.3.1 Control Register

address 04h

This register is used to set up the configuration of each operation in the MD8430. Usually, this register is set after the setting has been made for the LPSON bit shortly after the closure of the power switch, in order to determine the configuration of the MD8430.

7	6	5	4	3	2	1	0
				CSEn	IActive	AActive	LPSON

Bit 3 CSEn: CycleStartPacket output enable bit (RW)

0: The CycleTime data in the CycleStart packet are not output to the IDATA bus.

1: The CycleTime data in the CycleStart packet are output to the IDATA bus.

When a CycleStart packet is transmitted or received, only CycleTime data in that packet are output to the IDATA bus if this bit has been set at 1.

Bit 2 IActive: ISOFLG terminal control bit (RW)

0: The asserting condition of the ISOFLG terminal is set up as during transmission, and during reception of a channel set in the Isochronous Receive Configuration Register.

1: The asserting condition of the ISOFLG terminal is set up as during transmission, and during reception of all isochronous packets. This bit is used to determine the asserting condition of the ISOFLG terminal, and is effective as a trigger signal for isochronous packet transmission and reception.

Bit 1 AActive: ASYNCFLG terminal control bit (RW)

0: The asserting condition of the ASYNCFLG terminal is set up as during transmission, and during reception of an Async packet addressed to this node.

1: The asserting condition of the ASYNCFLG terminal is set up as during transmission, and during reception of all asynchronous packets. This bit is used to determine the asserting condition of the ASYNCFLG terminal, and is effective as a trigger signal for asynchronous packet transmission and reception.

Bit 0 LPSON: LinkPowerStatus On bit (RW)

This bit is used to control the LPS signal to be supplied to the PHY chip. According to the condition at the DIRECT terminal, contents of the output are different.

DIREC pin input	LPSON bit	LPS Output
1	0	0
1	1	1
0	0	0
0	1	Clock Out about 2MHz

## 3.3.2 Control Register

address 05h

7	6	5	4	3	2	1	0
ITZero	ITSyncMode	IsoMode[1:0]		MultiSpeed	CycleSource	CycleMaster	CycleTimer En

- Bit 7 ITZero: IsochronousZeroLengthPacket bit (RW)  
 0: No transmission is performed for a cycle without any transmission request during isochronous transmission in the auto-mode.  
 1: Transmission of the Length=0 packet is performed for a cycle without any transmission request during isochronous transmission in the auto-mode.  
 This bit is used to select whether packet transmission is not performed without transmission data for a cycle (the cycle where ITREQ# is not asserted) during isochronous transmission in the auto-mode, or a Length=0 packet is automatically transmitted.
- Bit 6 ITSyncMode: ITSYNC pin function selection bit (RW)  
 0: Functions as a setting pin for the Sync field in the header while the ITSYNC pin is used for transmission in the auto-mode.  
 1: Functions as a transmission control pin while the ITSYNC pin is used for transmission in the auto-mode.
- Bit 5-4 IsoMode: Isochronous Mode bit (RW)  
 00: Isochronous transmission/reception mode in normal mode. A maximum of 4 channels can be received.  
 01: Isochronous transmission/reception mode in normal mode. Isochronous snoop reception is performed.  
 10: Isochronous transmission/reception mode in auto-mode. A maximum of 4 channels can be received.  
 11: Isochronous transmission/reception mode in auto-mode. Isochronous snoop reception is performed.  
 If LSB setting is 0 during reception, isochronous reception is effected for a maximum of 4 channels by the received channel setting register in the case of coincidence with the set value. If it is 1 similarly, all isochronous packets available on the bus are received irrespective of the set register value, and these data outputs are sent to the IDATA bus. If more than 4 channels are received, such a condition is set up.
- Bit 3 MultiSpeed: MultiSpeed bit (RW)  
 1: The isochronous packet is transmitted by the multi-speed concatenation specified by IEEE 1394.A.  
 0: The CycleTimer is actuated at 24.576MHz obtained by dividing the 49.152MHz clock fed from the PHY chip, in order to control the isochronous cycle.
- Bit 2 CycleSource: CycleSource bit (RW)  
 1: The CycleTimer is updated at the rising point of the signal input from the CYCLE terminal, in order to control the isochronous cycle.  
 The update origin of the internal CycleTimer, in charge of isochronous time control, is set up.
- Bit 1 CycleMaster: CycleMaster bit (RW)  
 0: Receiving a CycleStart packet from another root node, the CycleTimer is controlled. Set at 0 for a node that cannot be a root node in general.  
 1: When this bit is 1, a CycleStart packet is generated each time the CycleTimer of the MD8430 counts 125mSec.  
 If the root bit is 0 even though this bit is set, no CycleStart packet is generated.
- Bit 0 CycleTimerEn: CycleTimerEnable bit (RW)  
 0: The CycleTimer is disabled.  
 1: The CycleTimer is enabled.

## 3.3.3 Control Register

address 07h

7	6	5	4	3	2	1	0
HReqLow	HAckLow	DMAEn				ReceiveEn	TransmitEn

- Bit 7      HReqLow: HREQ LowActive bit (RW)  
 0: The HREQ terminal is set at HighActive.  
 1: The HREQ terminal is set at LowActive.
- Bit 6      HAckLow: HACK LowActive bit (RW)  
 0: The HACK terminal is set at HighActive.  
 1: The HACK terminal is set at LowActive.
- Bit 5      DMAEn: DMA Enable bit (RW)  
 0: DMA for response data transfer is disabled.  
 1: DMA for response data transfer is enabled.  
 When the host performs lock processing for the device on the local bus, this bit is set at 0 in order to lock the access attempted from another node.
- Bit 4      Host: Host select bit (RW)  
 0: When a packet, which bears no relation to the response processing object, is received, such a packet is removed from the ARF buffer.  
 1: When a packet, which bears no relation to the response processing object, is received, such information is sent to the host so that the host can proceed to the latter processing.
- Bit 1      ReceiveEn: Receiver Enable bit (RW)  
 0: The receiver is disabled. The following reception only is effected:  
     - SelfID packet.  
 1: The receiver is enabled. The following reception is effected:  
     - Asynchronous packet addressed to this node.  
     - Isochronous packet of the specified channel.  
     - Reception in the snoop mode.
- Bit 0      TransmitEn: Transmitter Enable bit (RW)  
 0: The transmitter is disabled. No transmission is performed.  
 1: The transmitter is enabled. The following transmission is performed:  
     - Asynchronous packet.  
     - CycleStart packet when the CycleMaster bit is enabled.  
     - Isochronous packet.

### 3.4 Node Identification Register

#### 3.4.1 Node Identification Register

address 08h

Initial value 00h

7	6	5	4	3	2	1	0
IDValid	Root						

**Bit 7** IDValid: IDValid bit (RO, Initial value: 0b)  
 0: Only the packet is received, for which the BusNumber value is 3FFh and the NodeNumber value is 3Fh. Other packets are rejected.  
 1: Only the packet is received, which has been set in the above-mentioned register under the conditions below and addressed in the address space of IEEE1212.

- Both BusNumber and NodeNumber coincide with the values set in the register.
- BusNumber coincides with the register setting value, and the NodeNumber value is 3Fh.
- The BusNumber value is 3FFh and NodeNumber coincides with the register setting value.
- The BusNumber value is 3FFh and the NodeNumber value is 3Fh.

When BusReset occurs, this bit is reset to 0.

If the SelfID phase is finished and NodeNumber is defined, this bit is reset at 1.

Even when Reg0 is read from the PHY, this bit is updated.

**Bit 6** Root: Root bit (RO, Initial value: 0b)  
 0: The connected PHY is not the root.  
 1: The connected PHY is the root.  
 When BusReset occurs, this bit is reset to 0.  
 If the SelfID phase is finished and the connected PHY is the root, this bit is reset at 1.  
 Even when Reg0 is read from the PHY, this bit is updated.

#### 3.4.2 Node Identification Register

address 0Ah

7	6	5	4	3	2	1	0
BusNumber[9:2]							

**Bit 7-0** BusNumber[9:2]: BusNumber bit (RW)  
 This value is used to set up the BusNumber of 10 bits defined in the IEEE1212 space. During transmission, this value is used in the source\_ID region of the header region. According to BusNumber of destination\_ID of the received packet, this packet is received if its BusNumber coincides with this value, and rejected in otherwise case.

## 3.4.3 Node Identification Register

address 0Bh

Initial value Upper 2bit is set from ConfigRom. Lower 6 bits are 3Fh

7	6	5	4	3	2	1	0
BusNumber[1:0]		NodeNumbe[5:0]					

Bit 7-6 BusNumber[1:0]: BusNumber bit (RW)

Bit 5-0 NodeNumber: NodeNumber bit (RO, Initial value: 3Fh)

This value is used to set up the NodeNumber of 6 bits defined in the IEEE1212 space. During transmission, this value is used in the source\_ID region of the header region. According to NodeNumber of destination\_ID of the receiving packet, this packet is received if its NodeNumber coincides with this value, and rejected in otherwise case.

When BusReset occurs, this bit is set at 3Fh.

If the SelfID phase is finished and NodeNumber is defined, the NodeNumber is set up.

Even when Reg0 is read from the PHY, this bit is updated.

## 3.5 Packet Control Register

address 15h

7	6	5	4	3	2	1	0
	StrictIso		EnSnoop				

Bit 6 StrictIso: Iso packet transmit condition select bit (RW)

0: The isochronous packet receiving condition is not limited to post-transmission/reception of a CycleStart packet.

1: The isochronous packet receiving condition is limited to post-transmission/reception of a CycleStart packet.

Bit 4 EnSnoop: Enable Snoop bit (RW, Initial value: 0b)

0: Only the packet mapped to this node address is received.

1: The snoop mode is assumed.

The snoop mode is set up to receive all packets entered from the PHY. When an asynchronous packet is received, no Acknowledge packet is returned. All the packets received in this mode are output from the IDATA bus. No transmission is possible in this mode.

### 3.6 Diagnostic Status Register

#### 3.6.1 Diagnostic Status Register

address 19h

7	6	5	4	3	2	1	0
							Config

Bit0 Config:Configuration Status bit(RO)

This bit "1" indicate that MD8430 is doing configuration. MD8430 forbit to other registers during this bit is 1.

### 3.7 ATRetry Register

#### 3.7.1 ATRetry Register

address 21h

Initial value Upper 4 bit are 0h, Lower 4 bit are set from Config ROM.

7	6	5	4	3	2	1	0
RetryCount[3:0]				MaxRetryCountLimit[3:0]			

Bit 7-4 RetryCount: Retry Count bit (RW, Initial value: 0h)

While the MD8430stays in the single phase retry, the present number of retries is indicated.

Bit 3-0 MaxREtryLimit: Maximum Retry Count Limit bit (RW)

This bit is used to set up the number of retries to be conducted for the Busy Acknowledge from the destination node. The retry phase related to this count value falls on the single phase. If the retry phase is not finished within this set value, RetryTimeMax is asserted to complete the retry phase. Since then, the packet data in the ATF buffer are canceled. The maximum setting value is 15.

In the case of 0 setting, the MD8430 does not perform single phase retry.

If the Acknowledge packet cannot be received normally in the retry phase, this retry is suspended at that time point and the packet data in the ATF buffer are abolished.

## 3.7.3 ATRetry Register

address 24h

This bit is used to set up the number of retries to be conducted for the Busy Acknowledge from the destination node.

The retry phase related to this count value falls on the dual phase. If the retry phase is not finished within this set value, RetryTimeMax is asserted to complete the retry phase. Since then, the packet data in the ATF buffer are canceled. The maximum setting value is 8 seconds.

In the case of 0 setting, the MD8430 does not perform dual phase retry.

If the Acknowledge packet cannot be received normally in the retry phase, this retry is suspended at that time point and the packet data in the ATF buffer are abolished.

7	6	5	4	3	2	1	0
MaxRetrySecondLimit[2:0]			MaxRetryCycleLimit[12:8]				

Bit 7-5 MaxREtrySecondLimit: Maximum Second Limit bit (RW)  
This region covers the specified value in the unit of Second.

Bit 4-0 MaxRetryCycleLimit[12:8]: Maximum Retry Cycle Limit bit (RW)  
This region covers the specified value in the unit of Cycle. It is effective within the range of 0 to 7999.

## 3.7.4 ATRetry Register

address 25h

7	6	5	4	3	2	1	0
MaxRetryCycleLimit[7:0]							

Bit7-0 MaxRetryCycleLimit[7:0]: Maximum RetryCycletLimit bit(RW)  
Recommended value is 200(C8h). It means 25msec.

## 3.7.5 ATRetry Register

address 26h

Initial value 00h

7	6	5	4	3	2	1	0
RetrySecond[2:0]			RetryCycle[12:8]				

Bit 7-5 RetrySecond: Retry Second bit (RO, Initial value: 0h)  
While the MD8430 performs dual phase retry, the lapse time of present retry is shown in the unit of seconds.

Bitr 4-0 RetryCycle[12:8]: Retry Cycle bit (RO, Initial value: 00h)  
While the MD8430 performs dual phase retry, the lapse time of present retry is shown in the unit of cycle.

## 3.7.6 ATRetry Register

address 27h  
Initial value 00h

7	6	5	4	3	2	1	0
RetryCycle[7:0]							

Bit 7-0 RetryCycle[7:0]: Retry Cycle bit (RO, Initial value: 00h)

## 3.8 Cycle Timer Register

## 3.8.1 Cycle Timer Register

address 28h

The present CycleTimer value is indicated. This register is split into three regions. If the node using the MD8430 is for the CycleMaster, this register value is inserted during the transmission of a CycleStart packet. If it is not the case, the CycleTimer value in the CycleStart packet is loaded in this register to update the CycleTimer.

User can load any value in this register from ConfigROM. The load timing is between hardware reset and the end of diagnostics. When this node is not cycle master, this register is changed by cycle start packet from cycle master immediately. Usually, 0 is written on ConfigROM for this initial value.

7	6	5	4	3	2	1	0
CycleSecond[6:0]							CycleCount [12]

Bit 7-1 CycleSecond: Cycle Second bit (RW)  
This region starts counting up when the CycleCount register carries, in order to count seconds. It operates with Modulo128.

Bit 0 Cycle Count[12]: Cycle Count bit (RW)  
This region starts counting up when the CycleField register carries, in order to count isochronous cycles. It operates with Modulo8000.

## 3.8.2 Cycle Timer Register

address 29h

7	6	5	4	3	2	1	0
CycleCount[11:4]							

Bit 7-0 CycleCount[11:4] Cycle Count bit (RW)

## 3.8.3 Cycle Timer Register

address 2Ah

7	6	5	4	3	2	1	0
CycleCount[3:0]				CycleOffset[11:8]			

Bit 7-4 CycleCount[3:0]: Cycle Count bit (RW)

Bit 3-0 CycleOffset[11:8]: Cycle Offset bit (RW)

This region starts counting up with the 24.576MHz clock. It operates with Modulo3072.

## 3.8.4 Cycle Timer Register

address 2Bh

7	6	5	4	3	2	1	0
CycleOffset[7:0]							

Bit 7-0 CycleOffset[7:0]: Cycle Offset bit (RW)

## 3.9 Bus Timer Register

## 3.9.1 Bus Timer Register

address 2Ch

This is a timer register that is used to count BusTime. Counting up is forwarded each time the CycleCount timer of the CycleTime register carries up.

User can load any value in this register from ConfigROM. The load timing is between hardware reset and the end of diagnostics. When this node is not cycle master, this register is changed by cycle start packet from cycle master immediately. Usually, 0 is written on ConfigROM for this initial value.

7	6	5	4	3	2	1	0
SecondCountHi[24:17]							

Bit 7-0 SecondCountHi[24:17]: Bus TimerH bit (RW)

## 3.9.2 Bus Timer Register

address 2Dh

7	6	5	4	3	2	1	0
SecondCountHi[16:9]							

Bit 7-0 SecondCountHi[16:9]: Bus TimerH bit (RW)

## 3.9.3 Bus Timer Register

address 2Eh

7	6	5	4	3	2	1	0
SecondCountHi[8:1]							

Bit 7-0 SecondCountHi[8:1]: Bus TimeH bit (RW)

## 3.9.4 Bus Timer Register

address 2Fh

7	6	5	4	3	2	1	0
Second CountHi[0]	SecondCountLo[6:0]						

Bit 7 SecondCountHi[0]: Bus TimeH bit (RW)

Bit 6-0 SecondCountLo: Bus TimeH bit (RO, Initial value: 00h)  
Same value as CycleSecond.

### 3.10 Isochronous Transmit Configuration Register

#### 3.10.1 Isochronous Transmit Configuration Register

address 30h

When the isochronous transmission mode is AUTO, this register group is used to set up how the MD8430 handles the packet. In the case of Iso-AUTO mode, the transmission-enabled channel is limited to only one.

7	6	5	4	3	2	1	0
Tag[1:0]		Channel[5:0]					

Bit 7-6 Tag: Tag bit (RW)  
This value is used in the tag field of the isochronous packet header.

Bit 5-0 Channel: Channel bit (RW)  
This value is used in the channel field of the isochronous packet header.

#### 3.10.2 Isochronous Transmit Configuration Register

address 31h

7	6	5	4	3	2	1	0
						Speed[1:0]	

Bit 1-0 Speed: Speed bit (RW)  
00: Transmission by 100Mbps  
01: Transmission by 200Mbps  
10: Transmission by 400Mbps  
The transfer speed for transmission is set up.

#### 3.10.3 Isochronous Transmit Configuration Register

address 32h

7	6	5	4	3	2	1	0
Sync[3:0]				StartSync[3:0]			

Bit 7-4 Sync: Sync bit (RW)  
When SyncEn is set at 0, this value is used in the sy-field of the isochronous packet header.  
When SyncEn is set at 1, this value is used in the sy-field of the isochronous packet header, other than the StartSync packet at the ITSYNC terminal or the one specified by the StopSync packet.

Bit 3-0 StartSync: Start Sync bit (RW)  
When SyncEn is set at 1 and the ITSYNC terminal is asserted, this value is used in the sy-field of the isochronous packet header that is transmitted shortly thereafter.

## 3.10.4 Isochronous Transmit Configuration Register

address 33h

7	6	5	4	3	2	1	0
StopSync							SyncEn

Bit 7-4 StopSync: Stop Sync bit (RW)  
 When SyncEn is set at 1 and the ITSYNC terminal is negated, this value is used in the sy-field of the isochronous packet header that is transmitted shortly thereafter.

Bit 0 SyncEn: Sync Enable bit (RW)  
 0: Irrespective of the ITSYNC signal, contents of the Sync register are used any time in the sy-region of the isochronous packet header.  
 1: According to the ITSYNC signal, the sy-field value is determined in the transmitting isochronous packet header.  
 The StartSync value is used in the transmission packet shortly after ITSYNC assertion, the Sync value is used thereafter, and the StopSync value is used in the transmission packet shortly after ITSYNC negation.  
 If ITSYNC is negated, the following condition is assumed as a result of ITZero setting:  
 ITZero=0 : No transmission.  
 ITZero=1 : Conforming to SyncEn setting.

## 3.10.5 Isochronous Transmit Configuration Register

address 34h

7	6	5	4	3	2	1	0
ITLength[15:8]							

Bit 7-0 ITLength[15:8]: Isochronous Transmit Length bit (RW)  
 The transmission packet length is set in this register. This value is used in the data\_length field of the isochronous packet header.

## 3.10.6 Isochronous Transmit Configuration Register

address 35h

7	6	5	4	3	2	1	0
ITLength[7:0]							

Bit 7-0 ITLength[7:0]: Isochronous Transmit Length bit (RW)

## 3.11 Isochronous Receive Configuration Register1, 2, 3, 4

## 3.11.1 Isochronous Receive Configuration Register1, 2, 3, 4

address 38h(1), 3C(h2), 40h(3), 44h(4)

In cases other than snoop reception of the isochronous packet, this register group is used for the MD8430 to set up the type of a packet and the method of reception. In cases other than snoop reception mode, the number of channels capable of reception is 4.

A maximum of 4 types of receiving channel numbers, which have been set up here, are output from the CH[1:0] terminal as the following identification numbers:

Isochronous Receive Configuration 1: CH[1:0] = 00

Isochronous Receive Configuration 2: CH[1:0] = 01

Isochronous Receive Configuration 3: CH[1:0] = 10

Isochronous Receive Configuration 4: CH[1:0] = 11

7	6	5	4	3	2	1	0
Tag[1:0]		Channel[5:0]					

Bit 7-6 Tag: Tag bit (RW, Initial value: 00b)  
The receiving isochronous tag number is set up. The setting range is 0 to 3.

Bit 5-0 Channel: Channel bit (RW, Initial value 00h)  
The receiving isochronous channel is set up. The setting range is 0 to 63.

## 3.11.2 Isochronous Receive Configuration Register1, 2, 3, 4

address 3Ah(1), 3E(h2), 42h(3), 46h(4)

7	6	5	4	3	2	1	0
				StartSync[3:0]			

Bit 3-0 StartSync: Start Sync bit (RW, Initial value: 0h)  
When SyncEn is set at 1, reception control is effected according to this bit and the sy-field value of the isochronous packet header. Reception is started with the packet for which the sy-field of the packet of the preset channel number has coincided with the value of this register.

## 3.11.3 Isochronous Receive Configuration Register1, 2, 3, 4

address 3Bh(1), 3F(h2), 43h(3), 47h(4)

7	6	5	4	3	2	1	0
StopSync[3:0]						IsoRxEn	SyncEn

- Bit 7-4 StopSync: StopSync bit (RW, Initial value: 0h)  
 When SyncEn is set at 1, reception control is effected according to this bit and the sy-field value of the isochronous packet header. Once packet reception is started with StartSync and the sy-field of the isochronous packet header with the preset channel number receives a packet that coincides with the value of this register, reception of successive packets is stopped.  
 If receiving operation is suspended with the IsoRxEn bit prior to the reception of this value, reception is not performed any more until StartSync comes again.
- Bit 1 IsoRxEn: Isochronous Receive Enable bit (RW, Initial value: 0b)  
 0: Isochronous reception disabled.  
 1: Isochronous reception enabled.  
 Setting is made to determine if isochronous reception should be effective or not.
- Bit 0 SyncEn: Sync Enable bit (RW, Initial value: 0b)  
 0: Packet reception is effected regardless of the contents of StartSync and StopSync.  
 1: Packet reception is controlled with the preset channel number, StartSync, and StopSync.

### 3.12 Interrupt Register

#### 3.12.1 Interrupt Register

address 54h

Initial value 00h

The interrupt factor is known by reading this register. 1 indicates that the interrupt factor is arisen. The interrupt factor is cleared by writing 1.

7	6	5	4	3	2	1	0
TxRspDone	RxReqDone	RxDone	ARFRrej		IDValid	STO	RetryLimit

- Bit 7 TxRspDone: Transmit Response Done bit (RW, Initial value: 0b)  
Set at 1 when response packet transmission is finished and the returned Acknowledge packet is received. Also set at 1 in the retry phase when retry is finished or even when AckErr is set on the way.
- Bit 6 RxReqDone: Receive Request Done bit (RW, Initial value: 0b)  
Set at 1 when request packet reception is finished and DMA transfer of the pay load is completed.
- Bit 5 DxDone: Receive Done bit (RW, Initial value: 0b)  
Set at 1 when a packet other than the object of response processing has been received.
- Bit 4 ARFRrej: ARF Reject bit (RW, Initial value: 0b)  
Set at 1 when the MD8430 performs asynchronous reception or data are not stored in the ARF buffer.
- Bit 3 ATFAck: ATFAck bit (RW, Initial value: 0b)  
Acknowledge to ATFReq.
- Bit 2 IDValid: IDValid bit (RW, Initial value: 0b)  
Set at 1 when NodeID has been defined.
- Bit 1 STO: Split Time Out Detect bit (RW, Initial value: 0b)  
Set at 1 when STStart is issued and the count value is delivered to the SplitTimeLimit register.
- Bit 0 RetryLimit: Retry Limit Detect bit (RW, Initial value: 0b)  
Set at 1 when the MD8430 performs operation in the retry phase and that retry phase is not finished even after exceeding the limit value.

#### 3.12.2 Interrupt Register

address 55h

Initial value 00h

7	6	5	4	3	2	1	0
ATxEnd			ARxEnd		ITFNoTx		

- Bit 7 ATxEnd: Asynchronous Transmit End bit (RW, Initial value: 0b)  
Set at 1 when the MD8430 performs asynchronous transmission and the returned Acknowledge packet is received upon completion of transmission operation. Also set at 1 in retry operation when this retry phase is finished or when AckErr is set on the way.
- Bit 4 ARxEnd: Asynchronous Receive End bit (RW, Initial value: 0b)

Set at 1 when the MD8430 performs asynchronous reception or data are stored in the ARF buffer.

- Bit 2      ATFNoTx: Isochronous No Transmit bit (RW, Initial value: 0b)  
 Set at 1 when the MD8430 performs isochronous transmission in the AUTO mode and under the following conditions:
- When transmission is not conducted after reception and transmission of a CycleStart packet when ITZero=0.
  - When a packet of Length=0 is transmitted after reception and transmission of a CycleStart packet when ITZero=1.

### 3.12.3 Interrupt Register

address      56h  
 Initial value   00h

7	6	5	4	3	2	1	0
PhyInt	BusReset		PhyReg Rcvd	AckErr	TCodeErr	HdrErr	SentRej

- Bit 7      PhyInt: PhyInterrupt bit (RW, Initial value: 0b)  
 Set at 1 when an interrupt factor comes from the PHY connected to the MD8430.
- Bit 6      BusReset: Bus Reset bit (RW, Initial value: 0b)  
 Set at 1 when the PHY assumes the bus reset mode.
- Bit 4      PhyReqRcvd: Phy Register Received bit (RW, Initial value: 0b)  
 Set at 1 when data from the PHY are stored in RegData.
- Bit 3      AckErr: AckError bit (RW, Initial value: 0b)  
 Set at 1 when an Acknowledge packet cannot be received normally, which is returned from the destination node to the transmitted Asynchronous packet.
- Bit 2      TCodeErr: TCodeError bit (RW, Initial value: 0b)  
 Set at 1 when a code not supported by the MD8430 is set in the TCode region in the packet header during packet transmission.
- Bit 1      HdrErr: Header Error bit (RW, Initial value: 0b)  
 Set at 1 when a packet with a header containing an error is received during packet reception.
- Bit 0      SentRej: Sent Reject bit (RW, Initial value: 0b)  
 Set at 1 when the receiving buffer has no empty region for the packet capacity during asynchronous packet reception and the MD8430 returns a busy Acknowledge packet to that source node as a result of failure in packet reception.

### 3.12.4 Interrupt Register

address      57h  
 Initial value   00h

7	6	5	4	3	2	1	0
Cycle Seconds	CycleStart	CycleDone	CycleLost	CmdReset			

- Bit 7      CycleSecond: Cycle Second bit (RW, Initial value: 0b)  
Set at 1 when the CycleTimer of the MD8430 has counted 1 second.
- Bit 6      CycleStart: Cycle Start bit (RW, Initial value: 0b)  
Set at 1 when a new isochronous cycle is started.
- Bit 5      CycleDone: Cycle Done bit (RW, Initial value: 0b)  
Set at 1 when a certain isochronous cycle is completed.
- Bit 4      CycleLost: Cycle Lost bit (RW, Initial value: 0b)  
Set at 1 when a certain CycleStart packet is received to update the internal CycleTimer under the condition that the MD8430 node is not of the CycleTimer, and when the next CycleStart packet cannot be received for 250msec with that CycleTimer.
- Bit 3      CmdReset: Command Reset bit (RW, Initial value: 0b)  
Set at 1 when a packet addressed to the reset region in the CSR space has been received.

### 3.13 Interrupt Mask Register1

address      58h, 59h, 5Ah, 5Bh

Each interrupt causing factor in the interrupt register is masked by this register if it is necessary to avoid reflection of this factor on the INT1# signal. The allocation of this register is the same as that of the interrupt register. Each bit is masked by 1 setting.

### 3.14 Interrupt Mask Register2

address      5Ch, 5Dh, 5Eh, 5Fh

Each interrupt causing factor in the interrupt register is masked by this register if it is necessary to avoid reflection of this factor on the INT2# signal. The allocation of this register is the same as that of the interrupt register. Each bit is masked by 1 setting.

### 3.15 Split TimeOut Limit Register

#### 3.15.1 Split TimeOut Limit Register

address      60h

If a transaction falls into a split transaction, this register is used to control time-out. The counter starts when the STStart bit is 1 and stops with 0. When there is coincidence with the value set in this register during counting, Split time-out is delivered to the host by STO interrupt. This counter counts up every 125u. The setting value is less than 8 seconds.

7	6	5	4	3	2	1	0
SplitTimeLimit[15:8]							

Bit 7-0      SplitTimeLimit[15:8]: SplitTimeOutLimit bit (RW)

## 3.15.2 Split TimeLimit Register

address 61h

7	6	5	4	3	2	1	0
SplitTimeLimit[7:0]							

Bit 7-0 SplitTimeLimit[7:0]: SplitTimeOutLimit bit (RW)

## 3.16 Split Time Register

## 3.16.1 Split Time Register

address 62h

Initial value 00h

If a transaction falls into a split transaction, this register is used to control time-out. The counter starts when the STStart bit is 1 and stops with 0. At that time, the lapse time output is generated.

7	6	5	4	3	2	1	0
SplitTime[15:8]							

Bit 7-0 SplitTime[15:8]: SplitTime bit (RO, Initial value: 00h)

## 3.16.2 Split Time Register

address 63h

Initial value 00h

7	6	5	4	3	2	1	0
SplitTime[7:0]							

Bit 7-0 SplitTime[7:0]: SplitTime bit (RO, Initial value: 00h)

## 3.17 Split Time Start Register

address 65h

Initial value 00h

7	6	5	4	3	2	1	0
							STStart

Bit 0 STStart: SplitTimerStart bit (RW, Initial value: 0b)  
 0: Maintaining the Split Timer in the cleared state.  
 1: Starting the counter of the Split Timer. Restored to initial conditions with 0.  
 When STO interrupt arises, the STStart bit is automatically reset to 0.

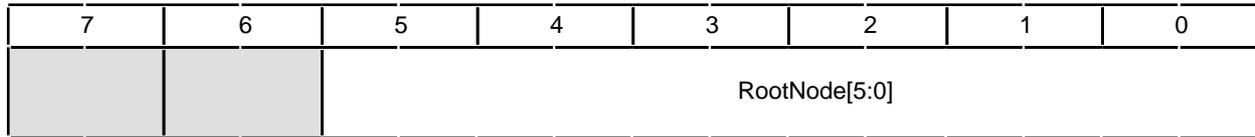
This timer is usable as programable timer(max 8seconds).

## 3.18 RootNode Register

address 6Eh

Initial value 3Fh

After completion of the Self\_ID phase, node\_ID of the root node is set up.



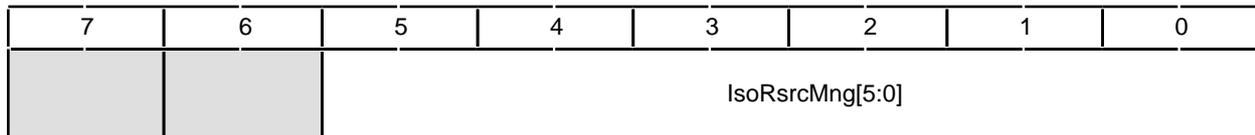
Bit 5-0 RootNode: RootNodeID bit (RO, Initial value: 3Fh)  
Indicates node\_ID of the root node.

## 3.19 IsoRsrcMng Register

address 6Fh

Initial value 3Fh

After completion of the Self\_ID phase, node\_ID of the isochronous\_resource\_manager node is set up.



Bit 5-0 IsoRsrcMng: Isochronous Resource Manager Node ID bit (RO, Initial value: 3Fh)  
Indicates node\_ID of the isochronous\_resource\_manager node.

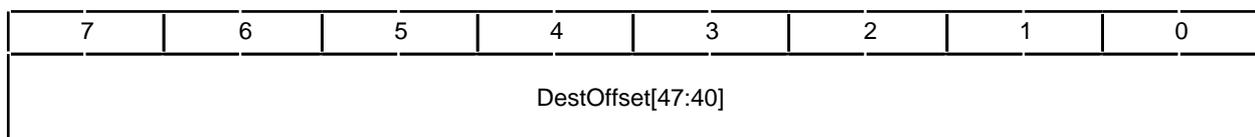
## 3.20 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

## 3.20.1 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 80h(1), 8Eh(2), 9Ch(3), AAh(4), B8h(5), C6h(6), D4h(7), E2h(8)

This is a conversion table to be used when a 48-bit address of IEEE1394 is converted into a 24-bit address of the local bus.  
The head address of the IEEE1394 address, being an object of conversion, is set up.

Payload of received packet which destination\_offset is between DestOffset and DestOffset+LSize-1 is transferred from LAdd of local address to LAdd+LSize-1



Bit 7-0 DestOffset[47:40]: destination\_offset bit (RW)

## 3.20.2 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 81h(1), 8Fh(2), 9Dh(3), ABh(4), B9h(5), C7h(6), D5h(7), E3h(8)



Bit 7-0 DestOffset[39:32]: destination\_offset bit (RW)

## 3.20.3 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 82h(1), 90h(2), 9Eh(3), ACh(4), BAh(5), C8h(6), D6h(7), E4h(8)

7	6	5	4	3	2	1	0
DestOffset[31:24]							

Bit 7-0 DestOffset[31:24]: destination\_offset bit (RW)

## 3.20.4 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 83h(1), 91h(2), 9Fh(3), ADh(4), BBh(5), C9h(6), D7h(7), E5h(8)

7	6	5	4	3	2	1	0
DestOffset[23:16]							

Bit 7-0 DestOffset[23:16]: destination\_offset bit (RW)

## 3.20.5 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 84h(1), 92h(2), A0h(3), AEh(4), BCh(5), CAh(6), D8h(7), E6h(8)

7	6	5	4	3	2	1	0
DestOffset[15:8]							

Bit 7-0 DestOffset[15:8]: destination\_offset bit (RW)

## 3.20.6 Destination Offset Register1, 2, 3, 4, 5, 6, 7, 8

address 85h(1), 93h(2), A1h(3), AFh(4), BDh(5), CBh(6), D9h(7), E7h(8)

7	6	5	4	3	2	1	0
DestOffset[7:2]							

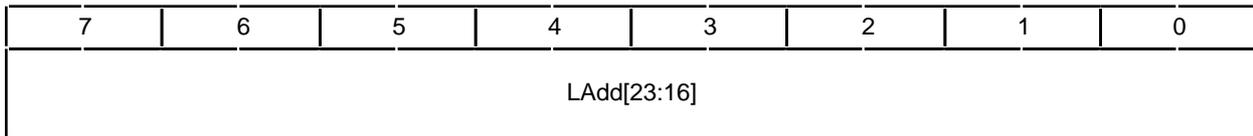
Bit 7-2 DestOffset[7:0]: destination\_offset bit (RW)

## 3.21 LocalAddress Register1, 2, 3, 4, 5, 6, 7, 8

## 3.21.1 LocalAddress Register1, 2, 3, 4, 5, 6, 7, 8

address 86h(1), 94h(2), A2h(3), B0h(4), BEh(5), CCh(6), DAh(7), E8h(8)

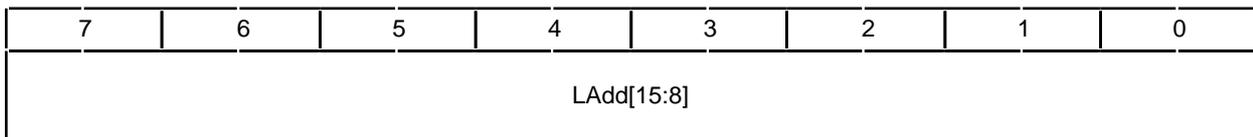
This is a conversion table to be used when a 48-bit address of IEEE1394 is converted into a 24-bit address of the local bus. The head address of the local address after conversion is set up.



Bit 7-0 LAddr[23:16]: Head address bit of the Local Address (RW)

### 3.21.2 LocalAddress Register1, 2, 3, 4, 5, 6, 7, 8

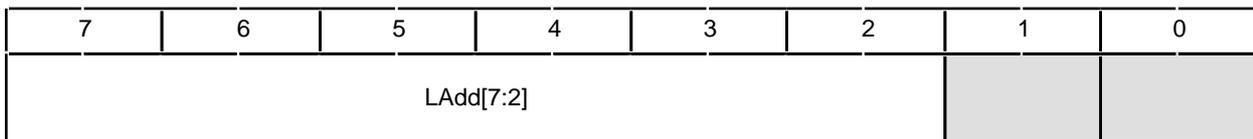
address 87h(1), 95h(2), A3h(3), B1h(4), BFh(5), CDh(6), DBh(7), E9h(8)



Bit 7-0 LAddr[15:8]: Head address bit of the Local Address (RW)

### 3.21.3 LocalAddress Register1, 2, 3, 4, 5, 6, 7, 8

address 88h(1), 96h(2), A4h(3), B2h(4), C0h(5), CEh(6), DCh(7), EAh(8)



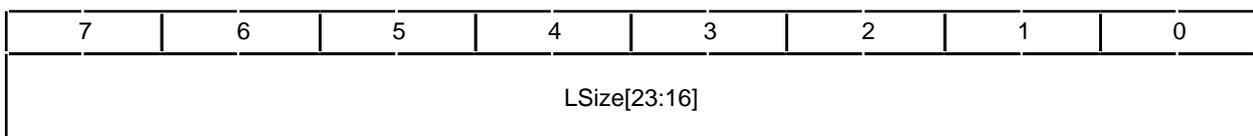
Bit 7-2 LAddr[7:0]: Head address bit of the Local Address (RW)

## 3.22 LocalSise Register1, 2, 3, 4, 5, 6, 7, 8

### 3.22.1 LocalSise Register1, 2, 3, 4, 5, 6, 7, 8

address 89h(1), 97h(2), A5h(3), B3h(4), C1h(5), CFh(6), DDh(7), EBh(8)

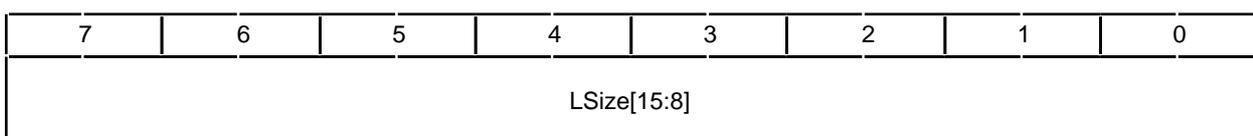
This is a conversion table to be used when a 48-bit address of IEEE1394 is converted into a 24-bit address of the local bus. The conversion range is set up.



Bit 7-0 LSize[23:16]: Conversion size bit (RW)

### 3.22.2 LocalSize Register1, 2, 3, 4, 5, 6, 7, 8

address 8Ah(1), 98h(2), A6h(3), B4h(4), C2h(5), D0h(6), DEh(7), ECh(8)



Bit 7-0 LSize[15:8]: Conversion size bit (RW)

## 3.22.3 LocalSize Register1, 2, 3, 4, 5, 6, 7, 8

address 8Bh(1), 99h(2), A7h(3), B5h(4), C3h(5), D1h(6), DFh(7), EDh(8)

7	6	5	4	3	2	1	0
LSize[7:2]							

Bit 7-2 LSize[7:2]: Conversion size bit (RW)

## 3.23 AccessFlag Register1, 2, 3, 4, 5, 6, 7, 8

address 8Ch(1), 9Ah(2), A8h(3), B6h(4), C4h(5), D2h(6), E0h(7), EEh(8)

This is a conversion table to be used when a 48-bit address of IEEE1394 is converted into a 24-bit address of the local bus. The right of access to the local address is set up.

7	6	5	4	3	2	1	0
ReadWait[1:0]		WriteWait[1:0]		Always 1	Read	Write	Lock

Bit 7-6 ReadWait: Read Wait bit (RW, Initial value: 3h)

The Wait cycle is set up, to be inserted in the read cycle of DMA transfer during automatic processing of Response.

00: NoWait, 01: 2Wait, 10: 4Wait, 11: 8Wait

Bit 5-4 WriteWaite: Write Wait bit (RW, Initial value: 3h)

The Wait cycle is set up, to be inserted in the write cycle of DMA transfer during automatic processing of Response.

00: NoWait, 01: 2Wait, 10: 4Wait, 11: 8Wait

Bit 3 Always 1. This bit should be set to 1.

Bit 2 Read: Read Access bit (RW, Initial value: 1b)

0: Setting the region where read processing is disabled.

1: Setting the region where read processing is enabled.

Bit 1 Write: Write Access bit (RW, Initial value: 1b)

0: Setting the region where write processing is disabled.

1: Setting the region where write processing is enabled.

Bit 0 Lock: Lock Access bit (RW, Initial value: 1b)

0: Setting the region where lock processing is disabled.

1: Setting the region where lock processing is enabled.

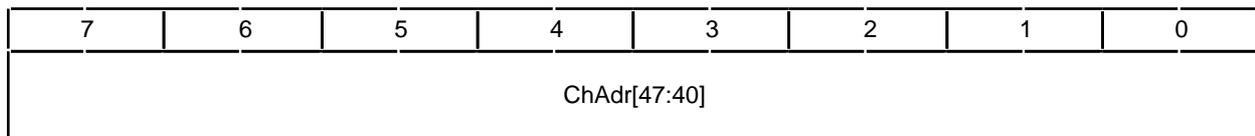
## 3.24 ChannelAddress Register

## 3.24.1 ChannelAddress Register

address F0h

Addresses are set up for the allocation of the receiving channel setting registers for isochronous packets and the isochronous auto-transmission length setting registers.

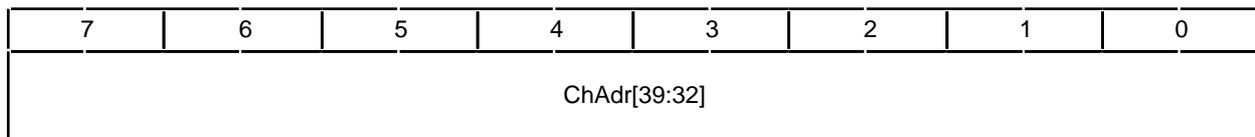
- ChAdr A packet to this address is reflected on isochronous receiving channel setting register 1 (38h).
- ChAdr+4 A packet to this address is reflected on isochronous receiving channel setting register 2 (3Ch).
- ChAdr+8 A packet to this address is reflected on isochronous receiving channel setting register 3 (40h).
- ChAdr+12 A packet to this address is reflected on isochronous receiving channel setting register 4 (44h).
- ChAdr+16 A packet to this address is reflected on isochronous auto transmission channel setting register (31h).
- ChAdr+20 A packet to this address is reflected on isochronous auto transmission length setting register (43h, 35h).



Bit 7-0 ChAdr[47:40]: Channel Address bit (RW)

## 3.24.2 ChannelAddress Register

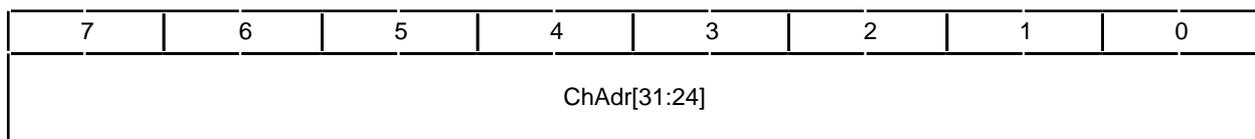
address F1h



Bit 7-0 ChAdr[39:32]: Channel Address bit (RW)

## 3.24.3 ChannelAddress Register

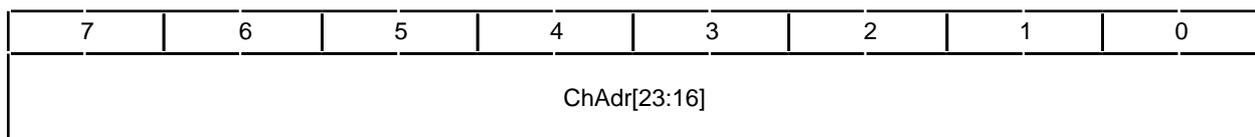
address F2h



Bit 7-0 ChAdr[31:24]: Channel Address bit (RW)

## 3.24.4 ChannelAddress Register

address F3h



Bit 7-0 ChAdr[23:16]: Channel Address bit (RW)

## 3.24.5 ChannelAddress Register

address F4h

7	6	5	4	3	2	1	0
ChAdr[15:8]							

Bit 7-0 ChAdr[15:8]: Channel Address bit (RW)

## 3.24.6 ChannelAddress Register

address F5h

7	6	5	4	3	2	1	0
ChAdr[7:2]						ChPos[1:0]	

Bit 7-2 ChAdr[7:2]: Channel Address bit (RW, Initial value: 0h)

Bit 1-0 ChPos[1:0]: Channel Position bit (RW, Initial value: 00b)

Setting up the location of the Byte where the receiving channel setting information is stored in the Quadlet data.

00: Stored in Data[31:24].

01: Stored in Data[23:16].

10: Stored in Data[15:8].

11: Stored in Data[7:0].

Transmission channel information is always stored in Data[7:0] and length setting information is always stored in Data[15:0].

## 3.25 SerialROM Register

## 3.25.1 SerialROM Register

address F6h

Initial value 00h

7	6	5	4	3	2	1	0
		RdDataValid	ROMR		ROMAddr[10:8]		

Bit 5 RdDataValid: Read Data Valid bit (RO, Initial value: 0b)

0: Normal state.

1: Indicates that data from Serial ROM are stored in ROMData after a read request has been issued.

When data from Serial ROM are stored in ROMData, 1 is set up. Reset to 0 since then if this register has been read out.

Bit 4 ROMRd: ROM Read bit (RW, Initial value: 0b)

0: Normal state.

1: Read request is issued.

A read request of Serial ROM is issued. After the request has been placed, this bit is reset to 0.

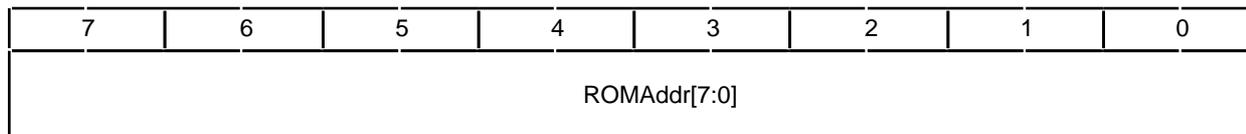
Bit 3-0 ROMAddr: ROM Address bit (RW, Initial value: 0h)

An address of the Serial ROM being accessed is set up.

## 3.25.2 SerialROM Register

address F7h

Initial value 00h

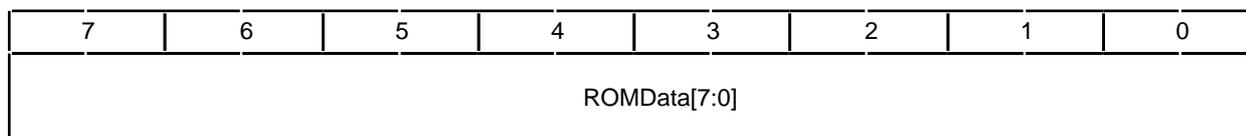


Bit 7-0 ROMAddr: ROM Address bit (RW, Initial value: 0h)  
An address of the Serial ROM being accessed is set up.

## 3.25.3 SerialROM Register

address F8h

Initial value 00h



Bit 7-0 ROMData: ROM Data bit (RW, Initial value: 00h)  
According to the read request, the data transferred from the Serial ROM are stored.

## 3.26 List of Register

Table 3.26.1 List of Register

Add	Register	7	6	5	4	3	2	1	0
00h	Version	Version[15:8]							
01h		Version[7:0]							
02h	Revision	Revision[15:8]							
03h		Revision[7:0]							
04h	Control					CSEn	IActive	AActive	LPSON
05h		ITZero	ITSync Mode	IsoMode[1:0]		Multi Speed	Cycle Source	Cycle Master	Cycle Timer En
06h									
07h		HRe Low	HACK Low	DMAEn				Receive En	Transmit En
08h	NodeIdentification	IDValid	Root						
09h									
0Ah		BusNumber[9:2]							
0Bh		BusNumber[1:0]	NodeNumbe[5:0]						
0Ch ~ 0Dh	Reserved								
0Eh ~ 14h	Reserved								
15h	PacketControl		StrictIso		EnSnoop				
16h ~ 17h	Reserved								

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0
18h	Reserved								
19h	DiagnosticStatus								Config
1Ah	Reserved								
1Bh	Reserved								
1Dh ~ 1Fh	Reserved								
20h	ATRetries								Retry Stop
21h		RetryCount[3:0]			MaxRetryCountLimit[3:0]				
22h ~ 23h	Reserved								
24h	ATRetries	MaxRetrySecondLimit[2:0]			MaxRetryCycleLimit[12:8]				
25h		MaxRetryCycleLimit[7:0]							
26h		RetrySecond[2:0]			RetryCycle[12:8]				
27h		RetryCycle[7:0]							
28h	CycleTimer	CycleSeconds[6:0]							Cycle Count [12]
29h		CycleCount[11:4]							
2Ah		CycleCount[3:0]			CycleOffset[11:8]				
2Bh		CycleOffset[7:0]							

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0
2Ch	BusTime	SecondCountHi[24:17]							
2Dh		SecondCountHi[16:9]							
2Eh		SecondCountHi[8:1]							
2Fh		Second CountHi [0]	SecondCountLo[6:0]						
30h	Isochronous Transmit Configuration	Tag[1:0]		Channel[5:0]					
31h								Speed[1:0]	
32h		Sync[3:0]			StartSync[3:0]				
33h		StopSync[3:0]						SyncEn	
34h		ITLength[15:8]							
35h		ITLength[7:0]							
36h ~ 37h	Reserved								
38h	Isochronous Receive Configuration-1	Tag[1:0]		Channel[5:0]					
39h									
3Ah						StartSync[3:0]			
3Bh		StopSync[3:0]						IsoRxEn	SyncEn
3Ch ~ 3Fh	Isochronous Receive Configuration-2	Same as above							
40h ~ 43h	Isochronous Receive Configuration-3	Same as above							
44h ~ 47h	Isochronous Receive Configuration-4	Same as above							

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0
50h ~ 53h	Reserved								
54h	Interrupt	TxRsp Done	RxReq Done	RxDone	ARFRej		IDValid	STO	Retry Limit
55h		ATxEnd			ARxEnd		ITFNoTx		
56h		PhyInt	Bus Reset		PhyReg Rcvd	AckErr	TCod Err	HdrErr	SentRej
57h		Cycle Seconds	Cycle Start	Cycle Done	Cycle Lost	Cmd Reset			
58h	InterruptMask1	TxRsp Done	RxReq Done	RxDone	ARFRej		IDValid	STO	Retry Limit
59h		ATXEnd			ARxEnd		ITFNoTx		
5Ah		PhyInt	Bus Reset		PhyReg Rcvd	AckErr	TCod Err	HdrErr	SentRej
5Bh		Cycle Seconds	Cycle Start	Cycle Done	Cycle Lost	Cmd Reset			

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0
5Ch Å` 5Fh	InterruptMask2	same as InterruptMask1							
60h	SplitTimeOut	SplitTimeOutLimit[15:8]							
61h		SplitTimeOutLimit[7:0]							
62h		SplitTime[15:8]							
63h		SplitTime[7:0]							
64h	Reserved								
65h	SplitTimerStart								STStart
66h Å` 6Dh	Reserved								
6Eh	RootNode			RootNode[5:0]					
6Fh	IsoRsrcMng			IsoRsrcMng[5:0]					
70h Å` 7Fh	Reserved								

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0	
80h	AddrExchange Table-1	DestinationOffset[47:40]								
81h		DestinationOffset[39:32]								
82h		DestinationOffset[31:24]								
83h		DestinationOffset[23:16]								
84h		DestinationOffset[15:8]								
85h		DestinationOffset[7:2]								
86h		LAdd[23:16]								
87h		LAdd[15:8]								
88h		Ladd[7:2]								
89h		LSize[23:16]								
8Ah		LSize[15:8]								
8Bh		LSize[7:2]								
8Ch			ReadWait[1:0]	WriteWait[1:0]	Always1	Read	Write	Lock		
8Dh		Reserved								
8Eh Å` 9Ah	AddrExchange Table-2	iØè,,								
9Bh	Reserved									
9Ch Å` A8h	AddrExchange Table-3	iØè,,								
A9h	Reserved									

Table 3.26.1 List of Register(continued)

Add	Register	7	6	5	4	3	2	1	0
AAh Å` B6h	AddresExchange Table-4	Same as above							
B7h	Reserved								
B8h Å` C4h	AddresExchange Table-5	Same as above							
C5h	Reserved								
C6h Å` D2h	AddresExchange Table-6	Same as above							
D3h	Reserved								
D4h Å` E0h	AddresExchange Table-7	Same as above							
E1h	Reserved								
E2h Å` EEh	AddresExchange Table-8	Same as above							
EFh	Reserved								
F0h	ChannelAddress	ChAdr[47:40]							
F1h		ChAdr[39:32]							
F2h		ChAdr[31:24]							
F3h		ChAdr[23:16]							
F4h		ChAdr[15:8]							
F5h		ChAdr[7:2]							ChPos[1:0]
F6h	SerialROM			RdData Valid	ROMR		ROMAddr[10:8]		
F7h		ROMAddr[7:0]							
F8h		ROMData[7:0]							

Caution!!) All reserved bits should be set to 0. MD8430 would be unstable if 1 is set for these regions.

4 Data Format

4.1 Asynchronous

MD8430 can return response packet only.

Status information of the response packet(rCode) is stored automatically by MD8430. Refer to Table 4.5.1 regarding the setting values.

How MD8430 select its rCode is described at [5.5.1 Read Request Receive].

4.2 Isochronous

4.2.1 Normal Transmit

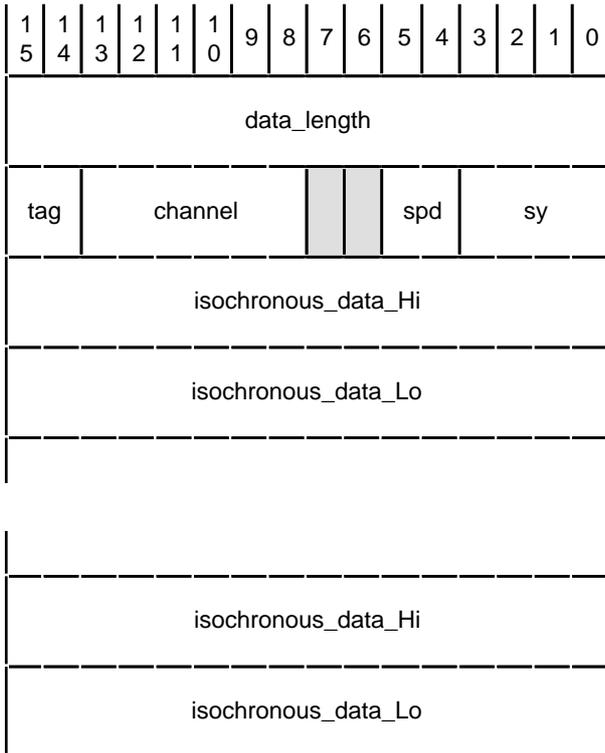


Figure 4.2.1.1 Normal Transmit

- data\_length:           The data length of isochronous\_data is set.
  
- tag:                    The isochronous transfer tag is set.
  
- channel:                The isochronous transfer channel is set.
  
- spd:                    Transfer speed is set. Refer to Table 4.6.6 regarding the setting values.
  
- sy:                     Sync of isochronous transfer is set.
  
- isochronous\_data:      Actual transfer data are set. If data\_length is not set with a value of a multiple of 4, it is necessary to fill it with 00h to complete the field in the Quadlet unit.

4.2.2 Normal Receive

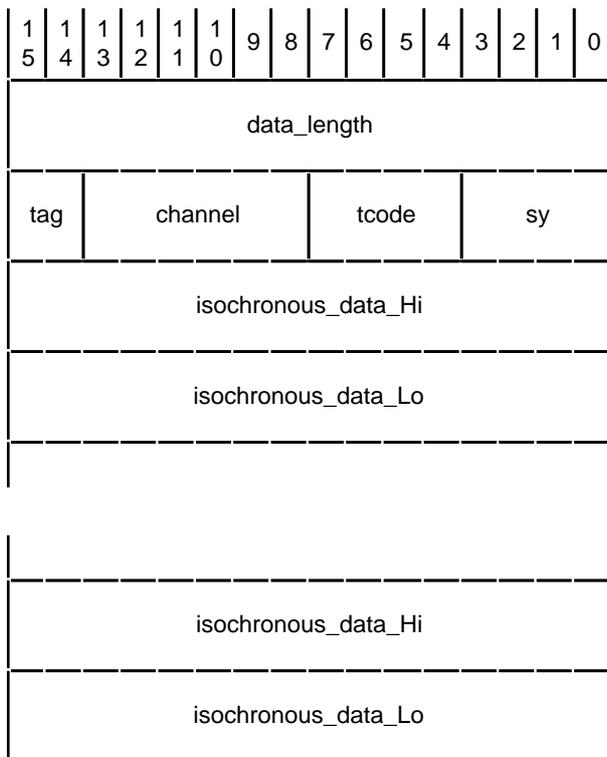


Figure 4.2.2.1 Normal Receive

- data\_length:           The data length of isochronous\_data is stored.
  
- tag:                    The isochronous transfer tag is stored.
  
- channel:                The isochronous transfer channel is stored.
  
- tcode:                  The tcode of Isochronous transfer is stored. The value is Ah.
  
- sy:                     Sync of isochronous transfer is stored.
  
- isochronous\_data:      Actual transfer data are stored.

## 4.2.3 Auto Transmit

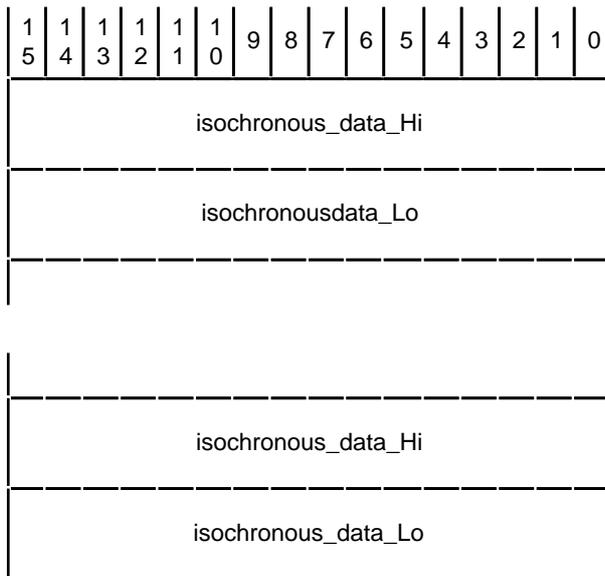


Figure 4.2.3.1 Auto Transmit

isochronous\_data: Actual transfer data are set. If data\_length is not set with a value of a multiple of 4, it is necessary to fill it with 00h to complete the field in the Quadlet unit.

## 4.2.4 Auto Receive

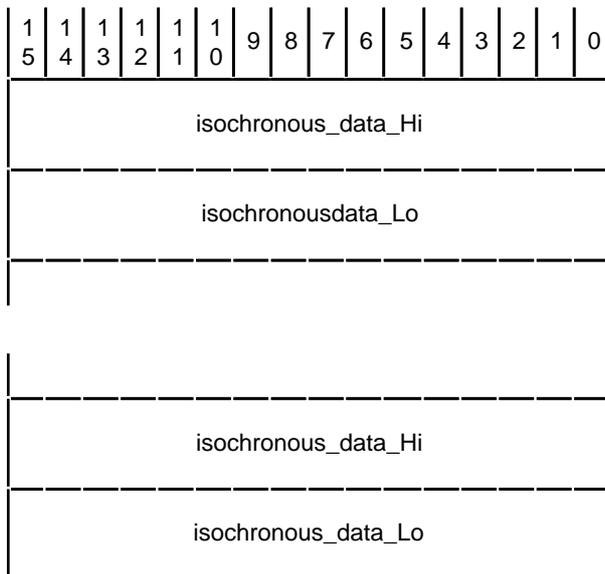


Figure 4.2.4.1 Auto Receive

Actual transfer data are stored.

4.3 Snoop

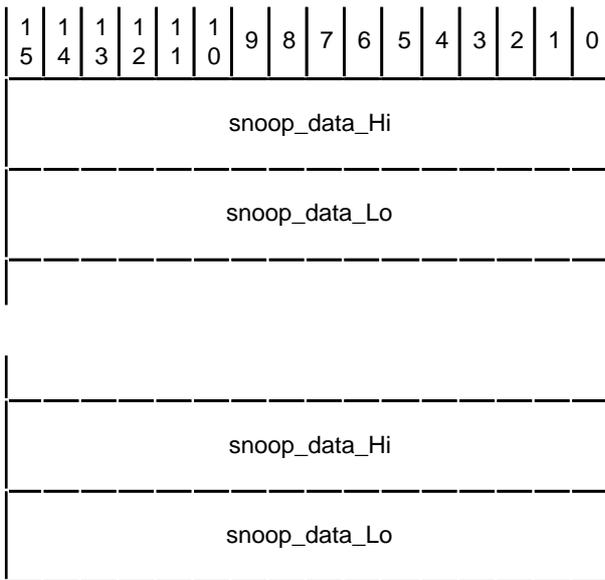


Figure 4.3.1 Snoop

snoop\_data: The snooped data is stored.

4.4 Max Data Length

IEEE1394-1995 defines maximum payload size for each conditions.

Table 4..4.4 Maximum Payload Size

Data rate	Maximum payload size ( byte )
100Mbps	512
200Mbps	1024
400Mbps	2048

MD8430 guarantee Asynchronous maximum payloadsize.

Table 4.4.5 data\_length for Isochronous packet

Data rate	Maximum payload size ( byte )	Bit Rate (bps)
100Mbps	1024	65,536,000
200Mbps	2048	131,072,000
400Mbps	4096	262,144,000

Because MD8430 does not have a FIFO for isochronous packet, MD8430 could be receive bigger packet than these size. However, all isochronous packet size should be smaller than full isochronous resource.

#### 4.5 Response Code

MD8430 generate its rCode as shown in table 4.5.1 automatically for received request packet.

How MD8430 select its rCode is described at [5.5.1 Read Request Receive].

Table 4.5.1 response code(rCode)

Code	Name
0000b	resp_complete
0001b	reserved
0010b	reserved
0011b	reserved
0100b	resp_conflict_error
0101b	resp_data_error
0110b	resp_type_error
0111b	resp_address_error
1XXXb	reserved

## 4.6 ROM Format

Table 4.6.1 ROM Format

Add	Register	7	6	5	4	3	2	1	0	Register	
000h	AddressExchange Table-1	DestinationOffset[47:40]								80h	
001h		DestinationOffset[39:32]								81h	
002h		DestinationOffset[31:24]								82h	
003h		DestinationOffset[23:16]								83h	
004h		DestinationOffset[15:8]								84h	
005h		DestinationOffset[7:2]									85h
006h		LAdd[23:16]								86h	
007h		LAdd[15:8]								87h	
008h		LAdd[7:2]									88h
009h		LSize[23:16]								89h	
00Ah		LSize[15:8]								8Ah	
00Bh		LSize[7:2]									8Bh
00Ch			ReadWait[1:0]	WriteWait[1:0]	Always1	Read	Write	Lock			8Ch
00Dh ∧ 019h	AddressExchange Table-2	The same as above								8Eh ∧ 9Ah	
01Ah ∧ 026h	AddressExchange Table-3	The same as above								9Ch ∧ A8h	
027h ∧ 033h	AddressExchange Table-4	The same as above								AAh ∧ B6h	

Table 4.6.1 ROM Format(continued)

Add	Register	7	6	5	4	3	2	1	0	Register
034h ~ 040h	AddressExchange Table-5	The same as above								B8h ~ C4h
041h ~ 04Dh	AddressExchange Table-6	The same as above								C6h ~ D2h
04Eh ~ 05Ah	AddressExchange Table-7	The same as above								D4h ~ E0h
05Bh ~ 067h	AddressExchange Table-8	The same as above								E2h ~ EEh
068h	ChannelAddress	ChAdr[47:40]								F0h
069h		ChAdr[39:32]								F1h
06Ah		ChAdr[31:24]								F2h
06Bh		ChAdr[23:16]								F3h
06Ch		ChAdr[15:8]								F4h
06Dh		ChAdr[7:2]						ChPos[1:0]		F5h
06Eh	Control					CSEn	IActive	AActive	LPSON	04h
06Fh		ITZero	ITSync Mode	IsoMode[1:0]		Multi Speed	Cycle Source	Cycle Master	Cycle TimerEn	05h
070h		HAck Low	HReq Low	DMAEn				Receive En	Transmit En	07h
071h	NodeIdentification	BusNumber[9:2]								0Ah
072h		BusNumber[1:0]								0Bh
073h	PacketControl		StrictIso		EnSnoop					15h

Table 4.6.1 ROM Format(continued)

Add	Register	7	6	5	4	3	2	1	0	Register	
074h	ATRetries					MaxRetryCountLimit[3:0]				21h	
075h		MaxRetrySecondLimit[3:0]			MaxRetryCycleLimit[12:8]					24h	
076h		MaxRetryCycleLimit[7:0]								25h	
077h	CycleTimer	CycleSeconds[7:0]								Cycle Count [12]	28h
078h		CycleCount[11:4]									29h
079h		CycleCount[3:0]				CycleOffset[11:8]					2Ah
07Ah		CycleOffset[7:0]								2Bh	
07Bh	BusTime	SecondCountHi[24:17]									2Ch
07Ch		SecondCountHi[16:9]									2Dh
07Dh		SecondCountHi[8:1]									2Eh
07Eh		Second CountHi [0]									2Fh
07Fh	Isochronous Transmil Configuration	Tag[1:0]		Channel[5:0]						30h	
080h								Speed[1:0]		31h	
081h		Sync[3:0]				StartSync[3:0]				32h	
082h		StopSync[3:0]							SyncEn		33h
083h		ITLength[15:8]									34h
084h		ITLength[7:0]									35h

Table 4.6.1 ROM Format(continued)

Add	Register	7	6	5	4	3	2	1	0	Register
085h	Isochronous Receive Configuration-1	Tag[1:0]		Channel[5:0]						38h
086h						StartSync[3:0]				3Ah
087h		StopSync[3:0]						IsoRxEn	SyncEn	3Bh
088h ~ 08Ah	Isochronous Receive Configuration-2	The same as above								3Ch ~ 3Fh
08Bh ~ 08Dh	Isochronous Receive Configuration-3	The same as above								40h ~ 43h
08Eh ~ 090h	Isochronous Receive Configuration-4	The same as above								44h ~ 47h
091h	BufferStatus and Control	DackEn	DreqEn		Select Dreq					50h
092h	InterruptMask1	TxRsp Done	RxReq Done	RxDone	ARFRej		IDValid	STO	Retry Limit	58h
093h		ATXEnd			ARxEnd		ITFNoTx			59h
094h		PhyInt	Bus Reset		PhyReg Rcvd	AckErr	TCode Err	HdrErr	SentRej	5Ah
095h		Cycle Seconds	Cycle Start	Cycle Done	Cycle Lost	Cmd Reset				5Bh
096h ~ 099h	InterruptMask2	The same as above								5Ch ~ 5Fh
09Ah	SplitTimeOut	SplitTimeOutLimit[15:8]								60h
09Bh		SplitTimeOutLimit[7:0]								61h
09Ch ~ 0FFh	Reserved									
100h ~ 4FFh	CSR ROM									

## 5 Functional Description

### 5.1 Serial ROM Interface

This is an interface to be used with the 2W type serial ROM (MN24C16FM8 by Fairchild Inc., or equivalent). The serial ROM is required to store information to set up the registers in the MD8430 and that of the ROM region in the CSR space.

After resetting, the serial ROM is read out to set up the internal registers. Even after setting, the host CPU enables to rewrite the internal registers. The clock SCL for serial ROM access is 400kHz.

### 5.2 Local Bus Interface

The local bus comes in the two types of operation modes, idle cycle and DMA cycle.

#### 5.2.1 Idle Cycle

Usual operation is effected in the idle cycle mode, which is used to gain access to a register in the MD8430. Timing of the local bus interface signal is of SRAM-like asynchronous transfer, and it is controlled by the respective signals of CS#, RD#, WR#, AD[7:0], and DATA[7:0]. Data access is effected by the Big Endian system.

##### 5.2.1.1 Register Access

Access to the register is done through the SRAM-like asynchronous bus as shown in Fig. 5.2.1.1.1.

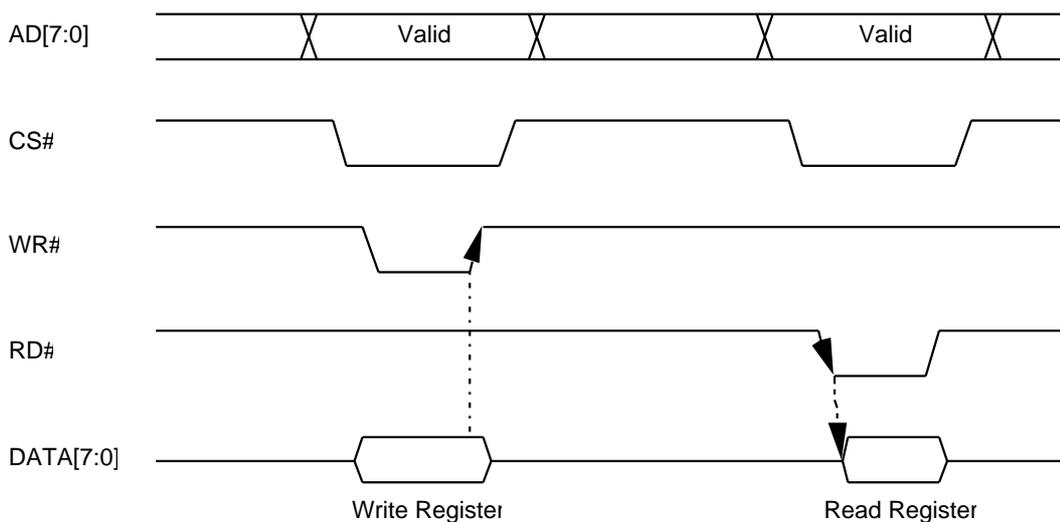


Figure 5.2.1.1.1 Register Access Timing

### 5.2.2 DMA cycle

The MD8430 manipulates its internal DMA controller to transfer send/receive data in conjunction with Response processing. Master clock is ICLK. At that time, the local bus operates in accordance with the DMA cycle. The address generated by the DMA controller consists of 24 bits. The MD8430 asserts HREQ to ask another bus master to release the bus. Another bus master places an announcement of bus release by asserting HACK.

If bus master is MD8430 only, HACK should be asserted always.

Regarding the device on the local bus being an object of DMA transfer, an announcement is placed by asserting READY# to indicate that data transfer is ready. If READY# is negated, DMA transfer is not carried out. The assertion period of HWR# and HRD# can be extended by asserting WAIT#. After the completion of DMA transfer, the local bus is released to normal in order to recover the idle cycle. Data access is effected by the Big Endian method.

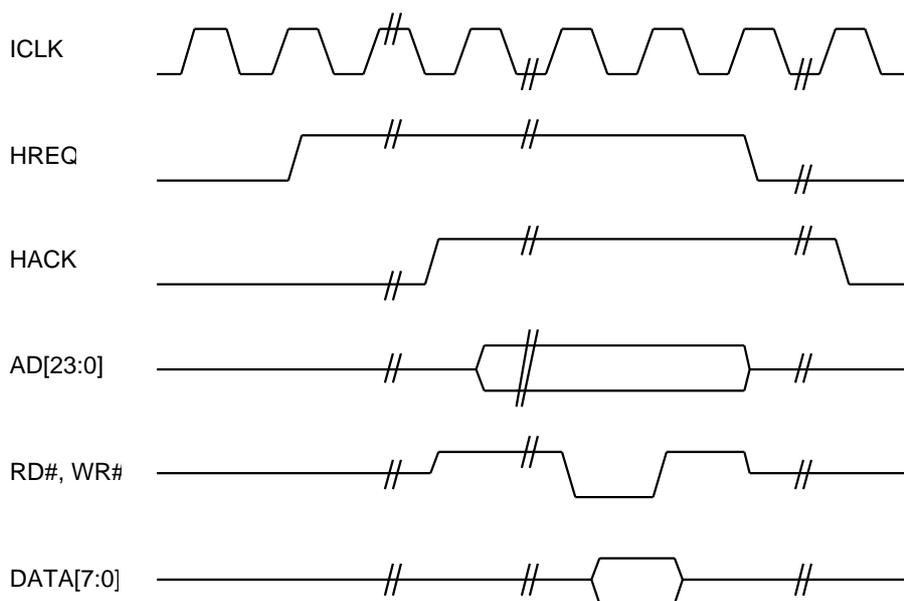


Figure 5.2.2.1 DMA Master Transfer Timing

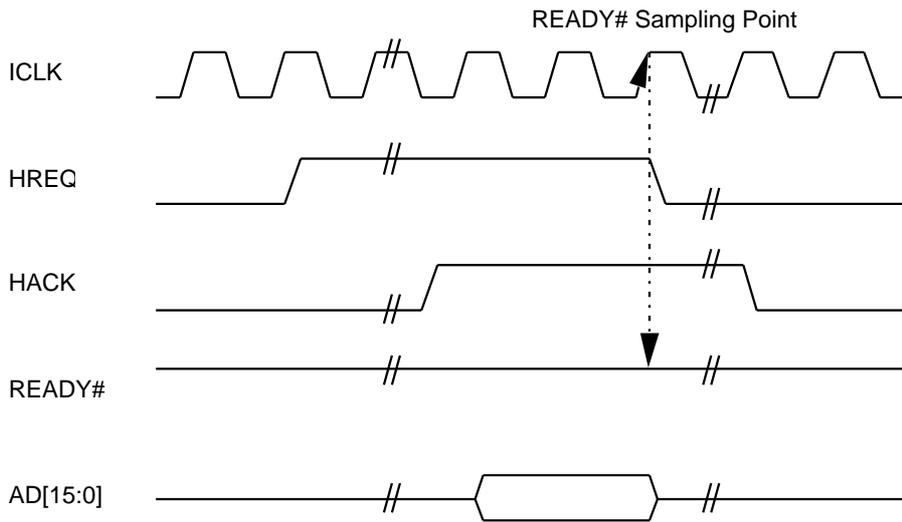


Figure 5.2.2.2 READY# Timing

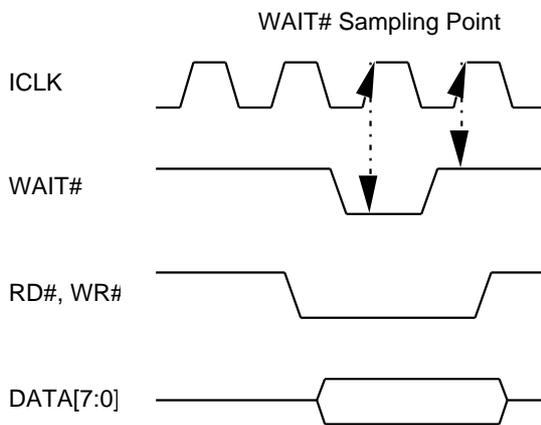


Figure 5.2.2.3 WAIT# Timing

### 5.2.3 Interrupt Processing

The MD8430 has the INT# terminal as a means of announcement of an interrupt factor to the host, defined in the Interrupt register and the InterruptMask register. The INT# signal is asserted in Active Low and in the form of OR of the interrupt factor that is not masked by the InterruptMask register. By setting up 1 in a bit in the Interrupt register, the corresponding bit is reset to 0 and the INT# terminal is negated.

### 5.3 PHY chip interface

The interface with the PHY chip is composed of the signals of SCLK, LREQ, D[0:7], and CTL[0:1]. For connections with PHY chips having various kinds of maximum transfer speeds, selection of 100Mbps, 200Mbps, and 400Mbps is performed with the D[0:7] signal. For a connection with the 100Mbps PHY chip, the D[0:1] signal is used to enable communication. For connections with the 200Mbps and 400Mbps PHY chips, the D[0:3] and D[0:7] signals are used, respectively.

#### 5.3.1 Connection Method

As a means of making a connection with the PHY chip, the MD8430 supports both AC and DC connection systems. For the DC connection, arrangements are made as shown in Fig. 5.3.1.1. The AC connection is made as shown in Fig. 5.3.1.2. Refer to the appendix regarding the circuit details for AC connection.

Caution!!) Connection method of Link and Phy should be same. (DC-DC or AC-AC)

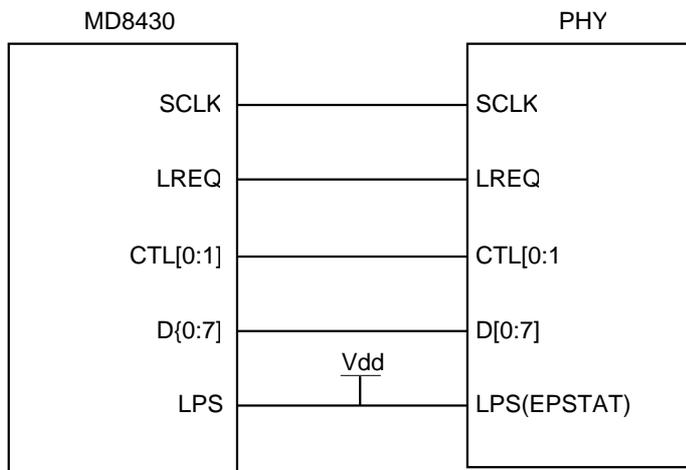


Figure 5.3.1.1 Connection Diagram of MD8430 and PHY chip (DC connection)

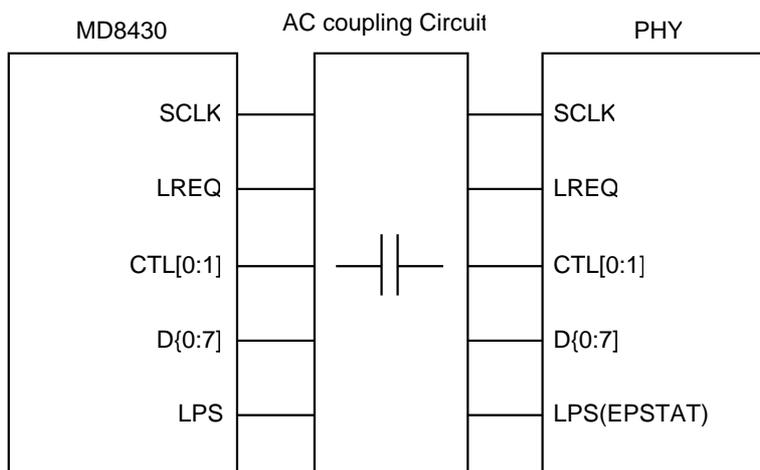


Figure 5.3.1.2 Connection Diagram of MD8430 and PHY chip (AC connection)

## 5.4 Response Address Conversion

A 48-bit address of IEEE1394 is converted into a 24-bit local address. The conversion table reads out and sets up the Serial ROM. This conversion table is composed of DestOffset for setting up the 48-bit address of IEEE1394, LAdd for setting up the local address after conversion, LSize for setting up the conversion size, and AccessFlag for setting up the right of access.

The payload of the receiving packet from DestOffset to DestOffset + Lsize-1 is transferred to the local address from LAdd to LAdd + LSize - 1.

## 5.5 Response Processing

### 5.5.1 Read Request Reception

In the case of a read request packet as a result of header reading, destination\_ID, tl, rt, tcode, pri, and rcode necessary for the generation of the response packet header are produced from the packet header in the following conditions:

Item	Contents	Condition
spd	spd of reception packet	
tl	tl of reception packet	
rt	2'b0	
tcode	4'b0010	tcode of reception packet is 4'b0000.
	4'b0010	tcode of reception packet is 4'b0001.
	4'b0110	tcode of reception packet is 4'b0100.
	4'b0111	tcode of reception packet is 4'b0101.
	4'b1011	tcode of reception packet is 4'b1001.
pri	4'b0	
destination_ID	source_ID of reception packet	
rcode	resp_complete	When destination is present and access is also permissible. When destination is a local address and READY#=Low.
	resp_conflict_error	READY#=High when destination is a local address.
	resp_type_error	When access to destination is prohibited. When extended_tcode is other than compare_swap. When destination is CSR and other than data_length=4.
	resp_address_error	When no destination is present.
data_length	data_length of reception packet	
	"0"	When rcode is other than resp_complete. (lock response excluded)
extended_tcode	extended_tcode of reception packet	

Only if the above rcode is resp\_complete, a payload is generated. Destination of response data is determined according to destination\_offset of the receiving packet and DMA transfer is effected toward the RFL register. When the transfer byte number is not a multiple of 4, 0 data is added to make it a multiple of 4 and then the resultant data are transferred to the ATF register. After the completion of transfer, ATGo is issued and transmitted to the serial bus. When TxEnd is detected, TxRspDone interrupt takes place.

### 5.5.2 Write Request Reception

In the case of a write request packet as a result of header reading, destination\_ID, tl, rt, tcode, pri, and rcode necessary for the generation of the response packet header are produced from the packet header. The conditions for generation are the same as those of 5.5.1 herein.

After the completion of header writing, response packet is transmitted to the serial bus. If the receiving packet is of Broadcast, transmission of a response packet is not conducted. Only if the above rcode is resp\_complete, a payload of the request packet is transferred after the examination of ack\_complete toward the response packet. Destination of request data to be stored is determined according to destination\_offset of the receiving packet and DMA transfer is effected. When rcode is in cases other than resp\_complete, payload is cleared.

Also, if MD8430 receive Quadlet Write Request, MD8430 does not write to local bus its payload data until reception of ack\_complete for the response packet. If MD8430 receive other than ack\_complete or ack\_busy, MD8430 cancel the transaction, and payload is cleared.

This function is usable when user would not like to receive twice request.

### 5.5.3 Lock Request Reception

In the case of a lock request packet as a result of header reading, destination\_ID, tl, rt, tcode, pri, and rcode necessary for the generation of the response packet header are produced from the packet header. The conditions for generation are the same as those of 5.5.1 herein.

When rcode is in cases other than resp\_complete, payload of request packet is cleared. Only if the above rcode is resp\_complete, a payload is generated.

Destination of response data is determined according to destination\_offset of the receiving packet and DMA transfer is effected toward the RFL register. When the transfer byte number is not a multiple of 4, 0 data is added to make it a multiple of 4 and then the resultant data are transferred to the internal asynchronous transfer register. After the completion of transfer, response packet is transmitted to the serial bus. When TxEnd is detected, TxRspDone interrupt takes place. After the examination of ack\_complete toward LockResponse, the processing specified by extended\_tcode is performed and RxReqDone interrupt takes place after the completion of this processing.

A resp\_type\_error is returned for other cases.

### 5.5.4 Packet Reception

Other than a packet for response action is cleared automatically.

## 5.6 Packet Transmission

### 5.6.1 Buffer

MD8430 has 2 memory buffers which size are  $512 \times 32 + 20 \times 32$  bit( 2128Byte). These are used for temporary buffer for response actions.

## 5.7 CSR Space

The CSR supported by the MD8430 is the following register:

## 5.7.1 NODE\_IDS

CSR offset : 008h

bus_id	offset_id	16'b0
--------	-----------	-------

Initial value

10'b1	Physical ID	16'b0
-------	-------------	-------

BusReset detection, Cmmand Reset Reception.

unchanged	unchanged	16'b0
-----------	-----------	-------

Read

last write	last update	16'b0
------------	-------------	-------

Write

stored	ignored	16'b0
--------	---------	-------

## 5.7.2 SPLIT\_TIMEOUT

CSR offset : 018h

29'b0		Split TimeOut Limit
SplitTimeOutLimit	19'b0	

Initial value

29'b0		0
800	19'b0	

BusReset detection, Cmmand Reset Reception.

29'b0		unch
unchanged	19'b0	

Read

29'b0		last w
last write	19'b0	

Write

ignored		stored
stored	ignored	

5.7.3 CYCLE\_TIME

CSR offset : 200h

second_count	cycle_count	cycle_offset
--------------	-------------	--------------

Initial value

0	0	0
---	---	---

BusReset detection, Cmmand Reset Reception.

unchanged	unchanged	unchanged
-----------	-----------	-----------

Read

last update	last update	last update
-------------	-------------	-------------

Write

node dependent	node dependent	node dependent
----------------	----------------	----------------

## 5.7.4 BUS\_TIME

CSR offset : 204h

second_count_hi	second_count_lo
-----------------	-----------------

Initial value

0	0
---	---

BusReset detection, Command Reset Reception.

unchanged	unchanged
-----------	-----------

Read

last write	last update
------------	-------------

Write

stored	ignored
--------	---------

## 5.7.5 BUSY\_TIMEOUT

CSR offset : 210h

4'b0	second_limit	cycle_limit	8'b0	retry_limit
------	--------------	-------------	------	-------------

Initial value

4'b0	0	200	8'b0	0
------	---	-----	------	---

Read

4'b0	last write	last write	8'b0	last write
------	------------	------------	------	------------

Write

ignored	stored	stored	ignored	stored
---------	--------	--------	---------	--------

### 5.7.6 COMMAND\_RESET

CSR offset : 00Ch

This is for Write Only, and any data are reflected on CommandReset of the interrupt register when a Write request is delivered to this address. Packets are abandoned. If CPU is not available, a reset request can be made from the outside by assigning INTA# or INTB# as a reset signal. In this case, however, Interrupt Clear is needed by performing register access. For this reason, it is recommended for unit resetting to perform mapping in the unit\_depend region of STATE\_SET or to the own address.

When a read request or a lock request is issued in this register region, an address error is returned after Ack\_Pending has been returned. To enable returning of the original type\_error, this address should be defined for Write Only in the Exchange Table

### 5.7.7 Processing of CSR space not supported

STATE\_CLEAR CSR offset : 000h

STATE\_SET CSR offset : 004h

STATE\_CLEAR and STATE\_SET, indispensable for IEEE1394-1995, are not supported for CSR. This area has considerable relation with external circuits and many optional sections are included. Therefore, mapping is arranged on external addresses as a read/write-enabled 64-bit space. Processing by logic circuits or local CPU should be performed.

The least minimal bit is linkoff of the STATE\_CLEAR.bus\_depend field. If 1 from STATE\_CLEAR is written here, it is necessary to cut off the power supply immediately for the parts (including the MD8430) other than the physical layer, working on power fed through the cable. This power supply can be started again after the physical layer has received a LinkOn packet and the LinkOn signal has been confirmed. However, this arrangement is limited to a system where the link layer operates with a cable power supply. If the system is designed so that only the physical layer works on the power fed from a cable, such a bit support is not required.

For the MD8430, the STATE\_CLEAR.gone bit becomes ready for transmission and reception immediately after bus reset. Therefore, setting should be kept at 0. The STATE\_CLEAR.lost bit can be generated from BusReset#. However, 0-fixing is acceptable as the transaction layer becomes available immediately after the release of bus reset. Other bits are optional. Necessary bits should be supported.

In the system without CPU, where power supply to the link layer is not from the cable and the node is not of the CycleMaster, this region may be mapped to the local bus that enables read and write. The condition is acceptable if this address has a ROM to return 0. In the case of a system that works on the power supply through a cable, GAL or the like should be arranged in place of the ROM so that a LinkOff signal can be used.

An example of a circuit, provided with the functions of LinkOn and LinkOff, is shown on the next page. Since the LinkOn signal stops when LPS is active, it is necessary to provide for a feature of self-holding. This can be realized by using an Enable signal of System's power circuit, and using linkOff to clear self-holding.

Link Off should be asserted as soon as possible when 0020h is written at STATE\_SET address.

STATE\_CLEAR address offset is FFFF0000000h. So, example of top 13 byte(1st exchange table) config data would be shown as bellow.

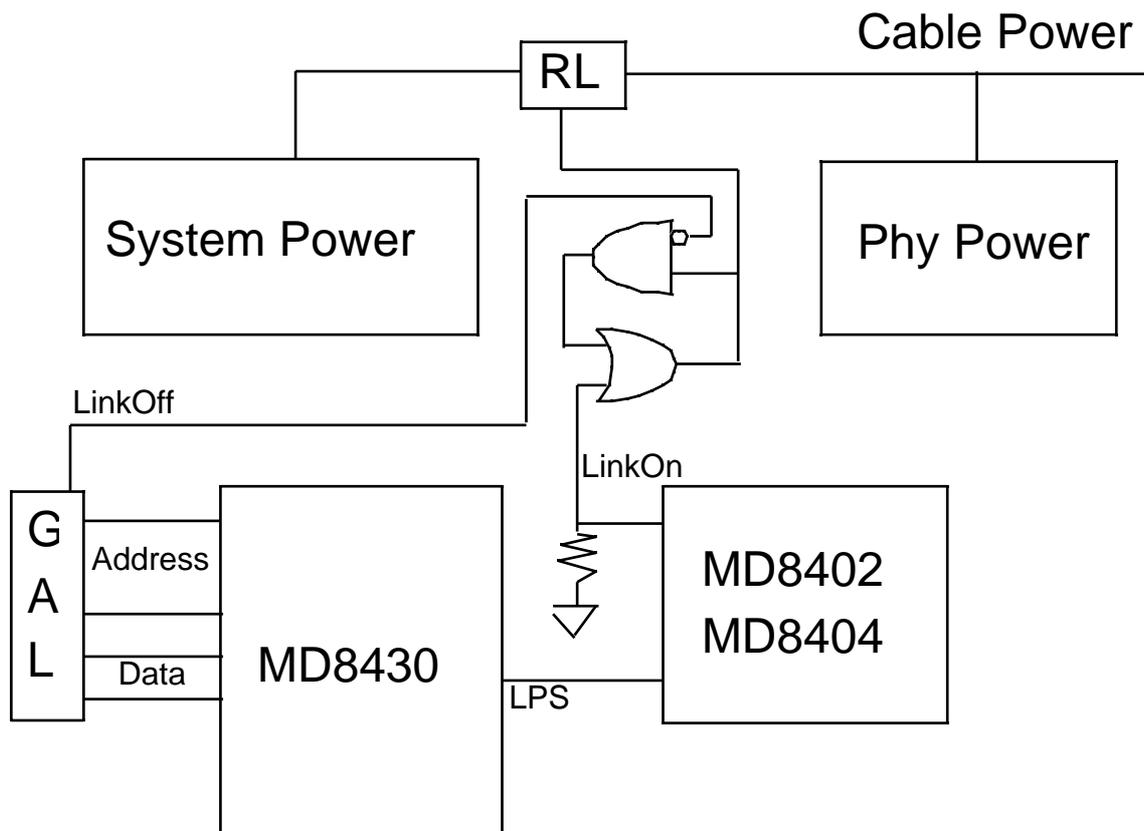
```
FF FF F0 00 00 00 80 00 00 00 00 03 0E
```

1st 6 byte show ISTATE\_CLEAR address offset defined by EEE1212. 2nd 3 byte show local address for this region. In this case address pin 23 and Pin 2 is asserted when STATE\_SET address is accessed. 3rd 3 byte show a size of this area.

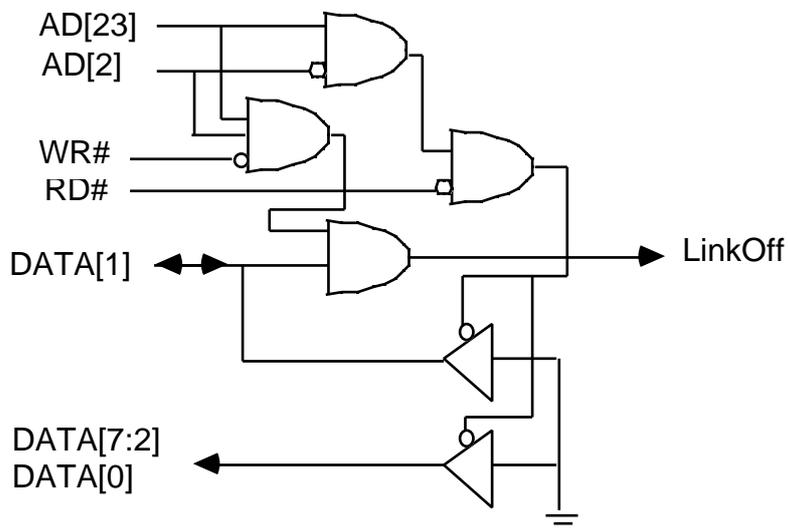
Because MD8430 has an error, this local size register require more 1 quadlet. In this case, required size is 3 quadlet for STATE\_CLEAR and STATE\_SET \*and\* more one quadlet for error.

Next circuit is based on above configuration.

### Example of Power Supply Designed for a System Working of Cable Power



Internal logic for GAL  
(Based on ConfigROM defined on 5.5.7)



#### 5.8 Exceptional Processing

1) When BusReset is generated.

All Response transactions are abandoned.

- 1) Before ReadResponse transmission -> ReadResponse transmission is abandoned.
- 2) Before LockResponse transmission -> LockResponse transmission is abandoned. Lock processing itself is also abandoned.
- 3) Before WriteResponse transmission -> WriteResponse transmission is abandoned. Write processing itself is also abandoned.

## 6 Exclusive isochronous bus

The MD8430 handles isochronous data with an external system via the exclusive bus of IDATA[15:0]. The MD8430 functions as a master at any time. It uses various control signals to perform synchronous data transfer, by requesting for a data input from the outside during transmission and a data output toward the outside during reception.

Since the MD8430 has no buffer for isochronous packets, the external system is always required to respond to each request for data input from the MD8430 during transmission. Also during reception, the external system is always required to acquire data at the output timing from the MD8430. During transmission, the control in the packet unit is conducted with the ITREQ# signal from the external system.

For both transmission and reception, the transfer rate of isochronous data in conjunction with the external system is a frequency of SCLK/8 if that packet is 100Mbps, SCLK/4 for 200Mbps, and SCLK/2 for 400Mbps. SCLK is a system clock of the MD8430 input from the PHY.

### 6.1 Isochronous Cycle Start Timing

The isochronous cycle is used at the intervals of 125msec. Because of asynchronous packet interrupt, however, actual transmission or reception of a CycleStart packet involves a jitter. As a signal that indicates the start of actual isochronous cycle, the MD8430 generates an ICS signal. The ICS signal is asserted for 4 clocks of ICLK.

Based on this ICS signal, a transmission request is placed in the unit of successive isochronous cycle. Even during reception, data are output if there is a receiving packet succeeding the ICS.

### 6.2 Transmission Request Processing

When the isochronous source of the external system makes a packet transmission request toward the MD8430, a transmission request is sent to the MD8430 with an ITREQ# signal. Upon the assertion of this ITREQ# signal, the MD8430 identifies that there is a packet transmission request from the outside. When this signal is negated, the MD8430 knows that the transmission request in that cycle has been finished.

While the ICS signal is asserted, a transmission request is placed by asserting the ITREQ# signal. As shown in Fig. 6.2.1/2, assertion of ITREQ# is decided with any one of ICLK1, 2, 3, 4 during ICS assertion. For an example of the figure, the assertion of ITREQ# signal is identified with ICLK2.

After one clock from the rising point of ICLK used to identify the ITREQ# assertion, the MD8430 sends out a data read-out request for 4 words (2 quadlets) toward the external system, using the ITX# signal. By this treatment, the MD8430 sends out a packet transmission request to the PHY, using the isochronous cycle started shortly after the ICS signal. After the time point when the using conditions of the serial bus have been obtained, the MD8430 sends out a data request to the external system by the use of the ITX# signal.

The transmission packet data on the IDATA bus are taken at the ICLK rising point during the period of ITX# assertion. In the case of the example in the figure, Iso-U(1) of the initial data is taken at the rising point of ICLK4.

At the end of the packet, IEOP# from the external system is asserted in conjunction with the ITX# timing when the last data of the packet are requested. Similarly as for the packet data take-out timing, the assertion of IEOP# is identified with the ICLK rising during ITX# assertion of the last data.

In the case of packet transmission only with the isochronous header and when the data pay load is 0, IEOP# is asserted at the second word of one Quadlet (for 2 words) of that header, in order to notify the MD8430 that the packet has no pay load. According to this notification, the MD8430 does not continue to read out any words after the second word, and performs packet transmission for the header only.

Handling during transmission is also the same in the case of isochronous normal mode or auto-mode. Only difference is that the contents of preceded data reading are the isochronous header in the normal mode and the first Quadlet of the pay load region, and that these contents are the first two Quadlets of the pay load region in the auto-mode.

Figures 6.2.1 and 6.2.2 are selected with the IBPS pins. When the IBPS pin is set at Low, the same timing as for the MD8430 is secured. In this case, the maximum rate is limited to 200Mbps, but the hardware developed for the MD8430 can be utilized immediately. If the IBPS is turned High, the maximum rate of 400Mbps becomes available.

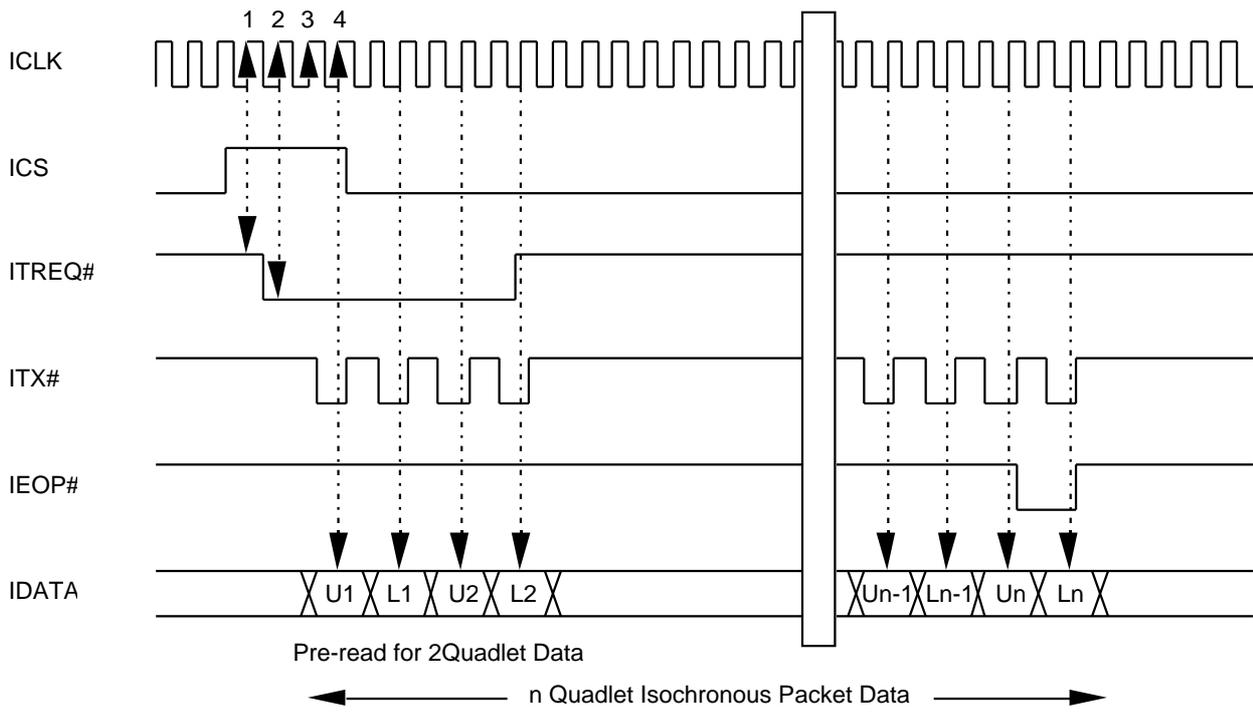


Figure 6.2.1 Isochronous Transmission Timing (IBPS=Low: MD8413 compatible mode)

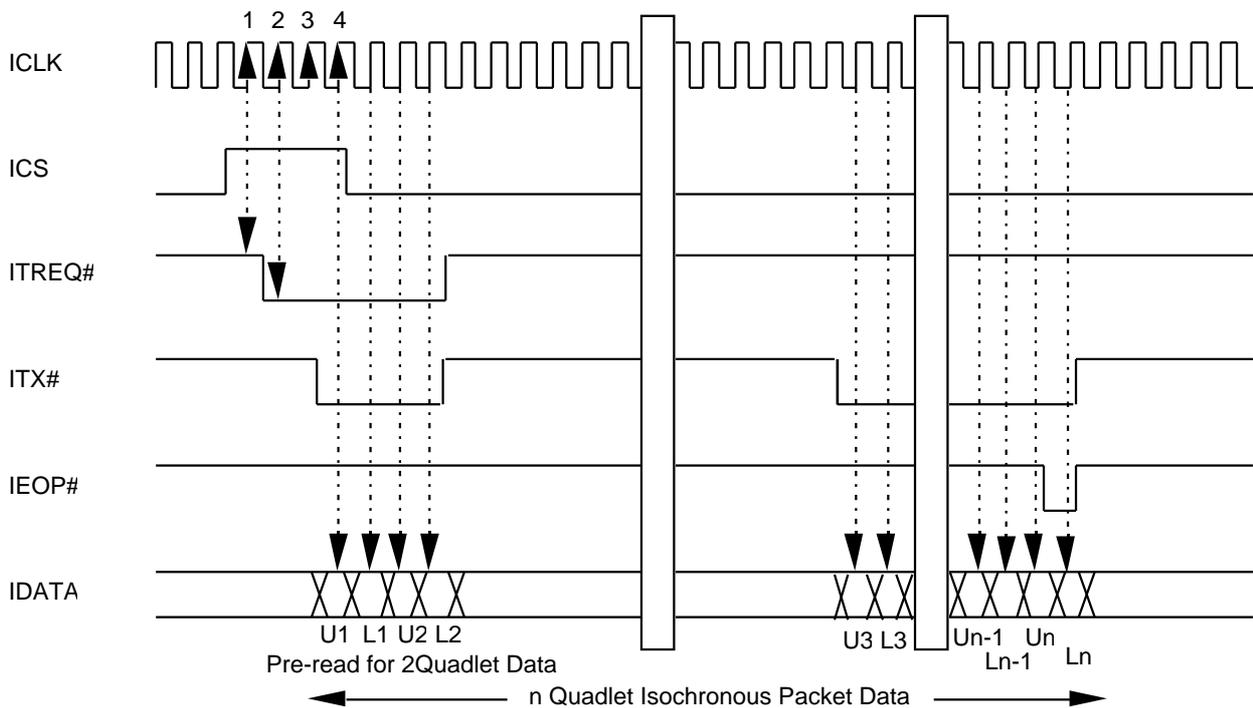


Figure 6.2.2 Isochronous Transmission Timing (IBPS=High: 400Mbps mode)

6.3 Multi-Channel Transmission Processing

Figures 6.3.1 and 2 show the example of multi-channel transmission (for multiple packets) performed in a certain isochronous transmission. As shown in the figure, the MD8430 identifies that there is the next transmission packet because ITREQ# is asserted during the assertion period of the first IEOP# (Isochronous Packet Data (1)). When the MD8430 identifies this condition, pre-reading of the next packet data is performed with the timing of the figure (period of Pre-read for Isochronous Packet Data (2)). After pre-reading in the same manner as described in 6.2, a request for the packet data is sent to the external system, succeeding the time point when the using conditions of serial bus have been acquired. In the example of the figure, two packets are transmitted and packet transmission is finished within the time period for the Isochronous Cycle (N). Thus, ITREQ# is negated with IEOP# of Isochronous Packet Data (2) to complete this cycle.

As described above, ITREQ# is kept asserted during multiple packet transmission. Such transmission is finished by negating the ITREQ# with IEOP# of the last packet to be transmitted.

Even though ITREQ# is once asserted during the assertion period of IEOP# in the Isochronous Cycle and it is asserted once more again, the MD8430 identifies that transmission of that cycle has been finished at the time point of ITREQ# negation and therefore it completes the cycle. If this assertion is maintained till the next appearance of ICS, it is recognized as a request for the transmission of the next Isochronous Cycle.

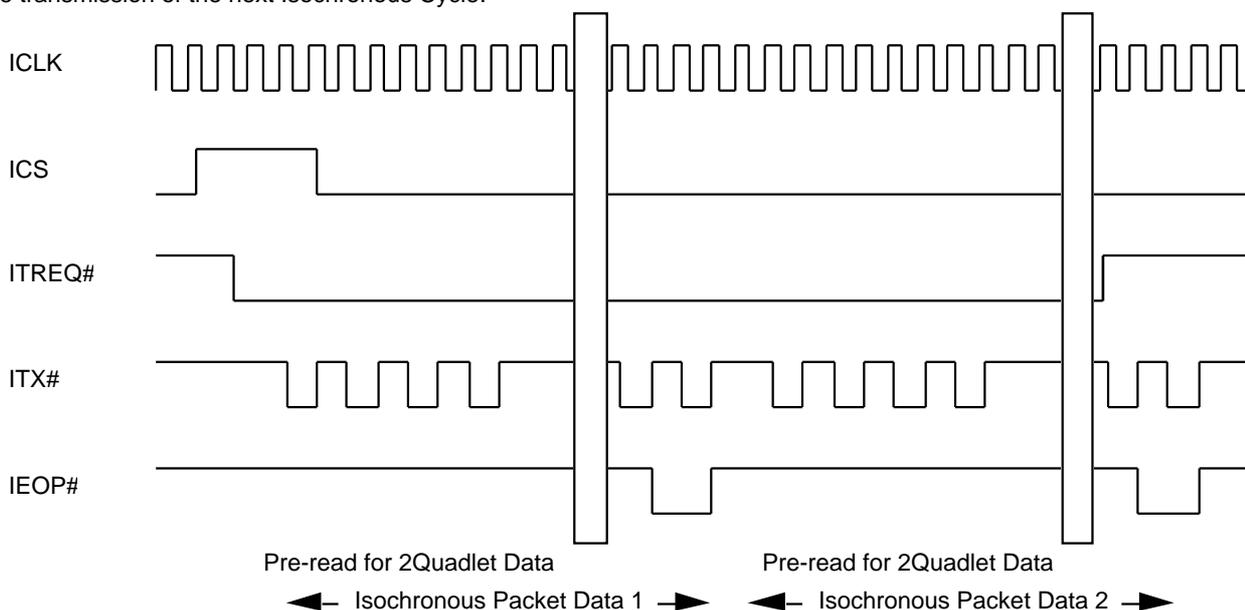


Figure 6.3.1 Multi-Channel Isochronous Transmission Timing (IBPS=Low: MD8413 compatible mode)

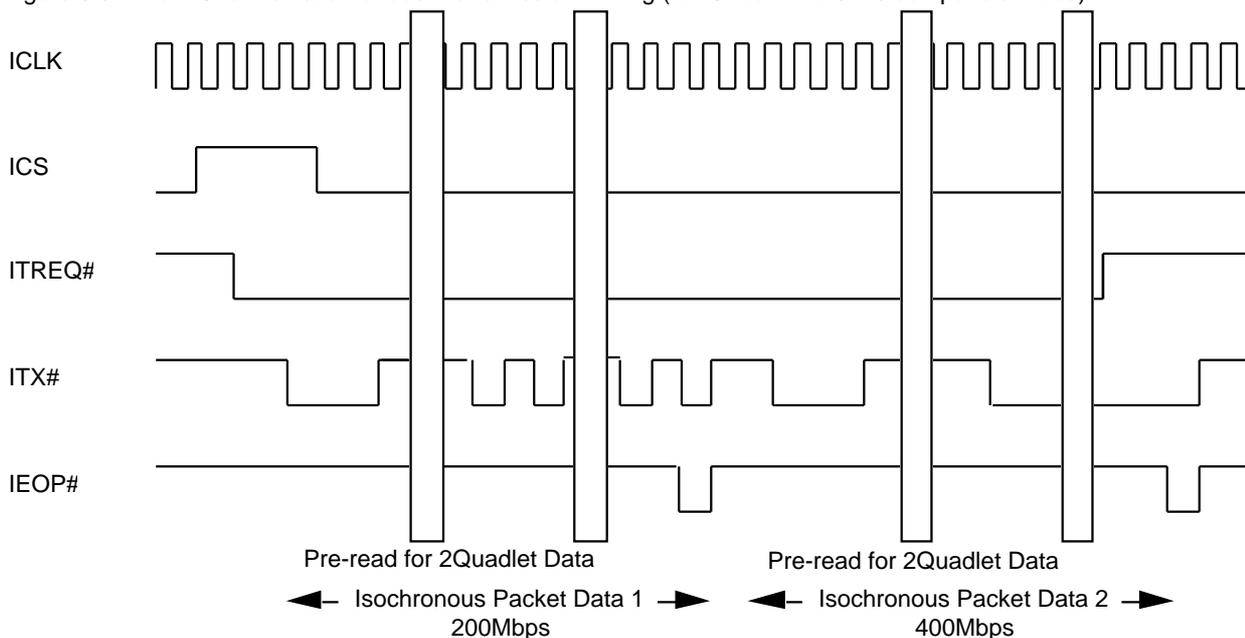


Figure 6.3.2 Multi-Channel Isochronous Transmission Timing (IBPS=High: 400Mbps mode)

#### 6.4 Reception Processing

Reception of the Isochronous Packet is started under the condition that setting has been made in the IsoMode of the Control Register and the Isochronous Receive Configuration Register after the transmission of a CycleStart packet for the root, or after the reception of a CycleStart packet for the non-root. The announcement of reception start is sent to the external system by asserting the IRCV#. This IRCV# is kept asserted until reception of that packet is finished. During the period of IRCV# assertion, the both-way IDATA bus stays in the output state.

After IRCV# assertion, an output of isochronous reception packet data is placed on the IDATA bus in synchronization with the IRX# assertion. After IRCV# assertion, the MD8430 maintains a continuous output of reception data. Therefore, the external system is required to be capable of obtaining such data, without fail.

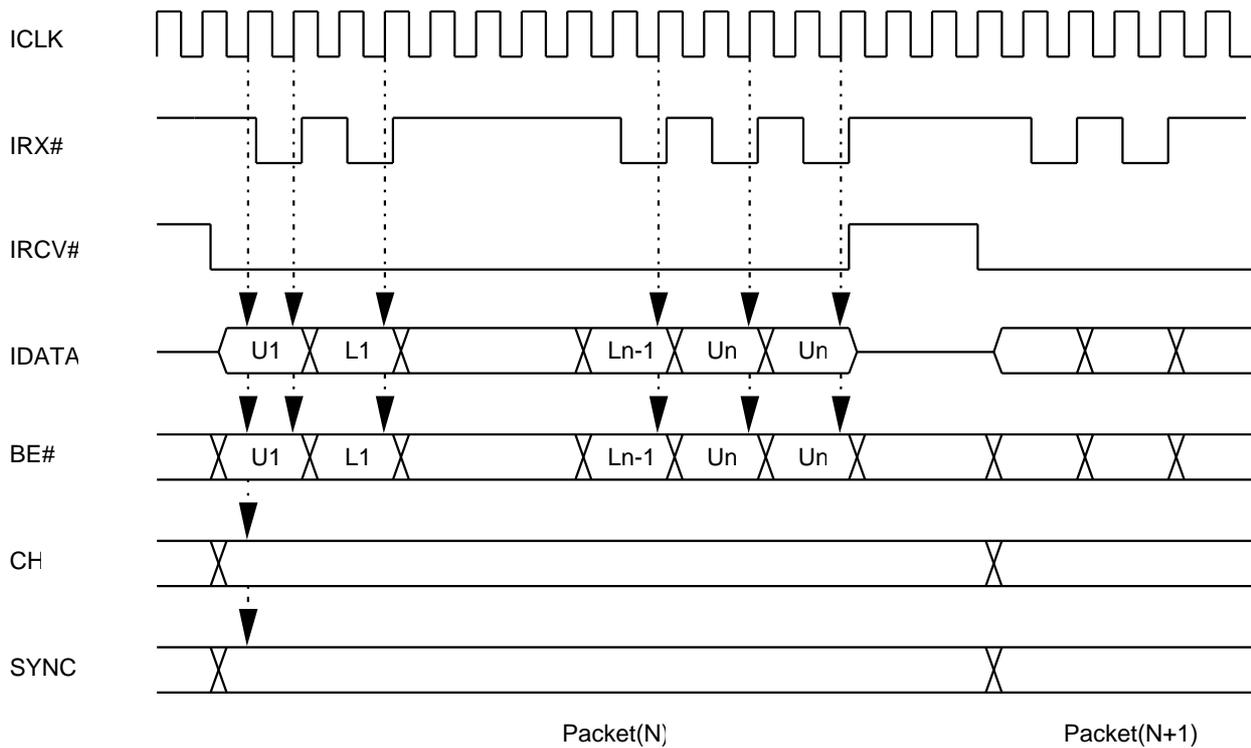


Figure 6.4.1 Isochronous Reception Timing

#### 6.4.1 BE# Signal

It is possible to know the zero-padding byte position with the BE# signal in the pay-load region of the received packet, in the unit of upper 8 bits and lower 8 bits. While CT is received, the BE# signal is not effective. The BE# signal is output in synchronization with the data output on the IDATA bus. BE#[1] shows the data of IDATA[15:8] and BE#[0] shows the data of IDATA[7:0]. BE#=0 indicates the effective data and BE#=1 shows the padding byte. The MD8430 identifies zero padding in accordance with the length value under the conditions of  $(\text{Quadlet}-1) < \text{Length}/4 < \text{Quadlet}$ , based on the length value in the header (Length) and the quadlet value of the packet pay load (Quadlet).

#### 6.4.2 CH Signal

It is possible to know the channel number of the received isochronous packet indirectly, using the CH signal. This is possible only if reception of a maximum of 4 channels has been set up in the IsoMode of the Control Register. (When the lower bits of IsoMode are 0.) In other cases, this feature is unstable. At the time point when IRCV# is asserted, the Isochronous Receive Configuration Register number corresponding to that packet is output. It is held till the assertion of the next IRCV# (next packet reception). CH=00 denotes Isochronous Receive Configuration Register-1, CH=01 is used to denote Isochronous Receive Configuration Register-2, CH=10 is used to denote Isochronous Receive Configuration Register-3, and CH=11 is used to denote Isochronous Receive Configuration Register-4. By these arrangements, it is possible to know the channel indirectly, set by the Isochronous Receive Configuration Register.

#### 6.4.3 SYNC Signal

It is possible to know the status with the Sync signal, where the respective SYNC information set in the sy region in the isochronous header of the received packet and the Isochronous Receive Configuration Register coincides with the following conditions:

##### SYNC values

- 01 : When the StartSync value set in the register coincides with the SYNC value in the packet header.
- 10 : When the StopSync value set in the register coincides with the SYNC value in the packet header.
- 11 : While the StartSync value set in the register coincides with the SYNC value in the packet header and further coincides with the StopSync value thereafter.
- 00 : Under conditions other than the above.

After the time point when IRCV# is asserted, the above conditional values corresponding to that packet are output. These values are maintained till the next IRCV# assertion (next packet reception).

6.5 CycleStart packet reception

When the MD8430 transmits a CycleStart packet in the root mode or receives a CycleStart packet in the non-root mode, it sends out an output to the IDATA bus, which output is only the Cycle\_Time\_Data field in that packet. As shown in Fig. 6.5.1, the external system can identify that there is an output of Cycle\_Time\_Data on the IDATA bus through the assertion of the CT signal.

32 bits of each Cycle\_Time\_Data are output in two groups on the IDATA bus in a bus width of 16 bits. Accuracy of intervals of each Cycle\_Time\_Data in the first output data is the same as the timing accuracy of the CycleTimer in the MD8430 when updating it with Cycle\_Time\_Data. Based on the output timing of the CT signal, the external system can construct a local CycleTimer with the same accuracy of the CycleTimer in the MD8430. (The interval  $\Delta t (=t_2 - t_1)$  from  $t_2$  to  $t_1$  in Fig. 6.5.1 has the same accuracy as that used in the MD8430.)

With these functions, the external system can perform processing like time stamp for example, by utilizing the CycleTimer that is the bus time specified for the IEEE1394 bus.

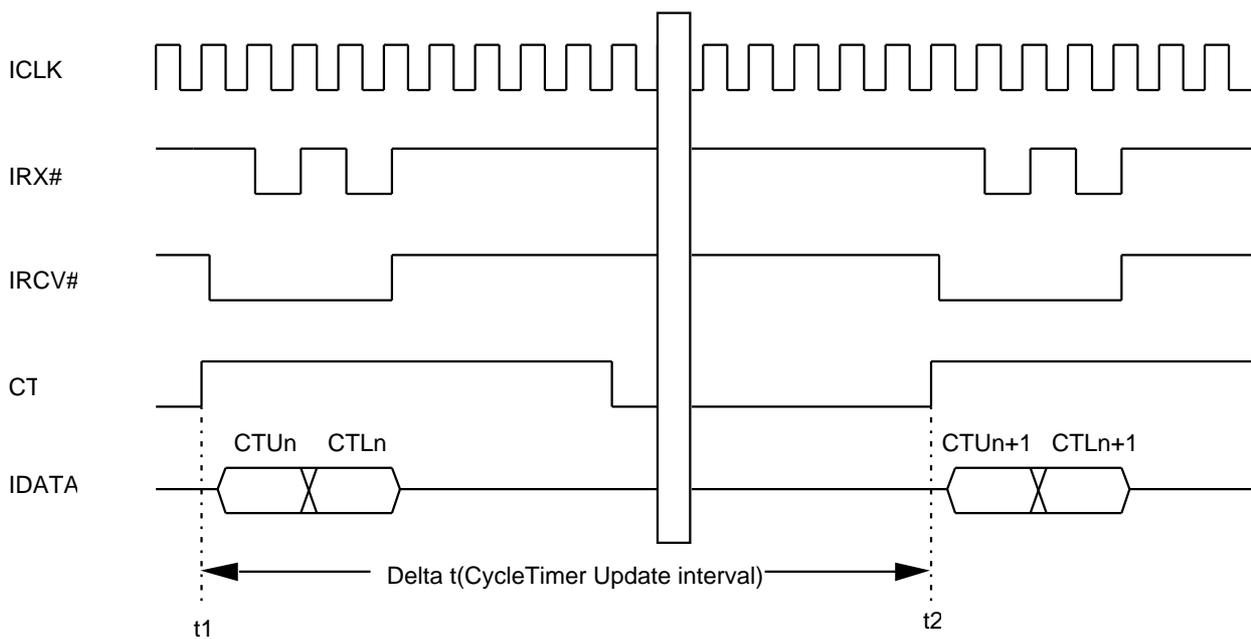


Figure 6.5.1 Cycle\_Time\_Data Output Timing

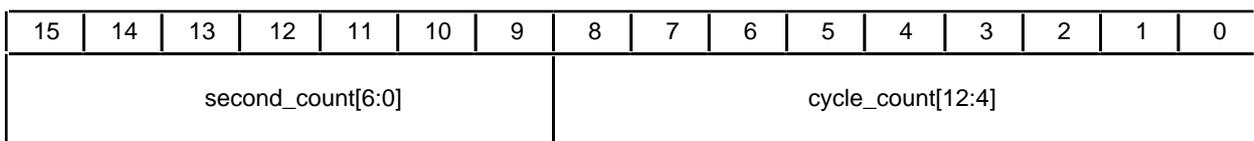


Figure 6.5.2 Contents of CTU

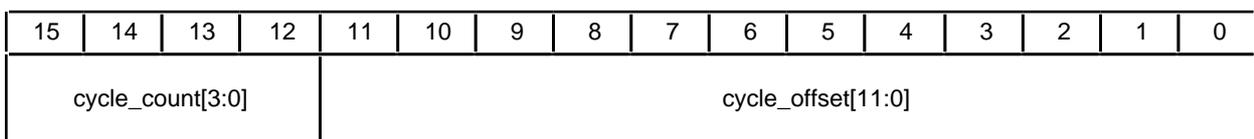


Figure 6.5.3 Contents of CTL

## 6.6 Packet Error Announcement during Reception

When an isochronous packet is received and this packet is not normal due to CRC error, packet defect, or the like, the MD8430 sends out an announcement to the external system about the packet error by asserting the IRERR# signal. Using this IRERR# signal, the external system can abandon the packet that contains an error.

### 6.6.1 Announcement of CycleStart Packet Error

As shown in Fig. 6.6.1.1, announcement of CycleStart packet error is done with the IRERR# signal after the assertion of the CT signal and the lapse of 8 clocks at ICLK, if it is an ordinary CRC error. Even though the CRC error does not occur, the CT signal is asserted till the last timing of the occurrence of an error in the CycleStart packet. (For 9 clocks of ICLK) In the case of an error such as a defect or the like in the CycleStart packet, IRERR# appears before that timing, but this is always an error of the CycleStart packet, where IRERR# occurs in the CT assert period. When the external system intends to update a local CycleTimer counter by the use of this CycleTimer value, this CycleTimer value is loaded to update the CycleTimer counter at the timing after the fall of the CT signal under the condition that IRERR# is not generated in the asserting period of the CT signal. In this manner, updating can be avoided with the CycleTimer value in the CycleStart packet where an error has arisen.

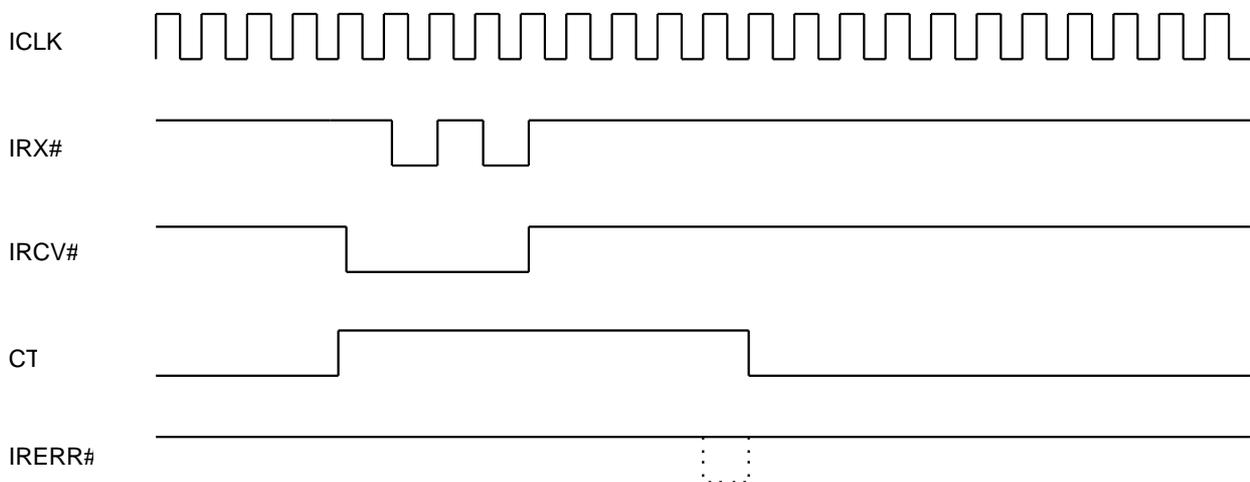


Figure 6.6.1.1 Announcement of CycleStart Packet Error during Reception

6.6.2 Announcement of Isochronous Packet Error

The appearing pattern of IRERR# can differ according to the style of an error, such as CRC error in the header and pay load, failure in coincidence of the length value in the header with the pay-load length in actual packet, a mid-defect in the header, a mid-defect in the pay load, and so on. In any case, such an error appears in the middle of IRCV# assertion, or after IRCV# negation of that packet and before IRCV# assertion for the next packet reception. The relationship between IRX#, IRCV#, and IRERR# comes in a pattern as shown in Fig. 6.6.2.1. In the case of Pattern (1), IRERR# is asserted simultaneously with IRCV# assertion, and packet reception is finished upon the negation of IRCV# while IRX# is not asserted. In this case, completion of reception is shown only with the first quadlet of the packet.

In Cases (2) and (3), a CRC error in the header or a packet defect or the like arises in the middle of reception. In Case (4), IRERR# is asserted with a CRC error in the pay load.

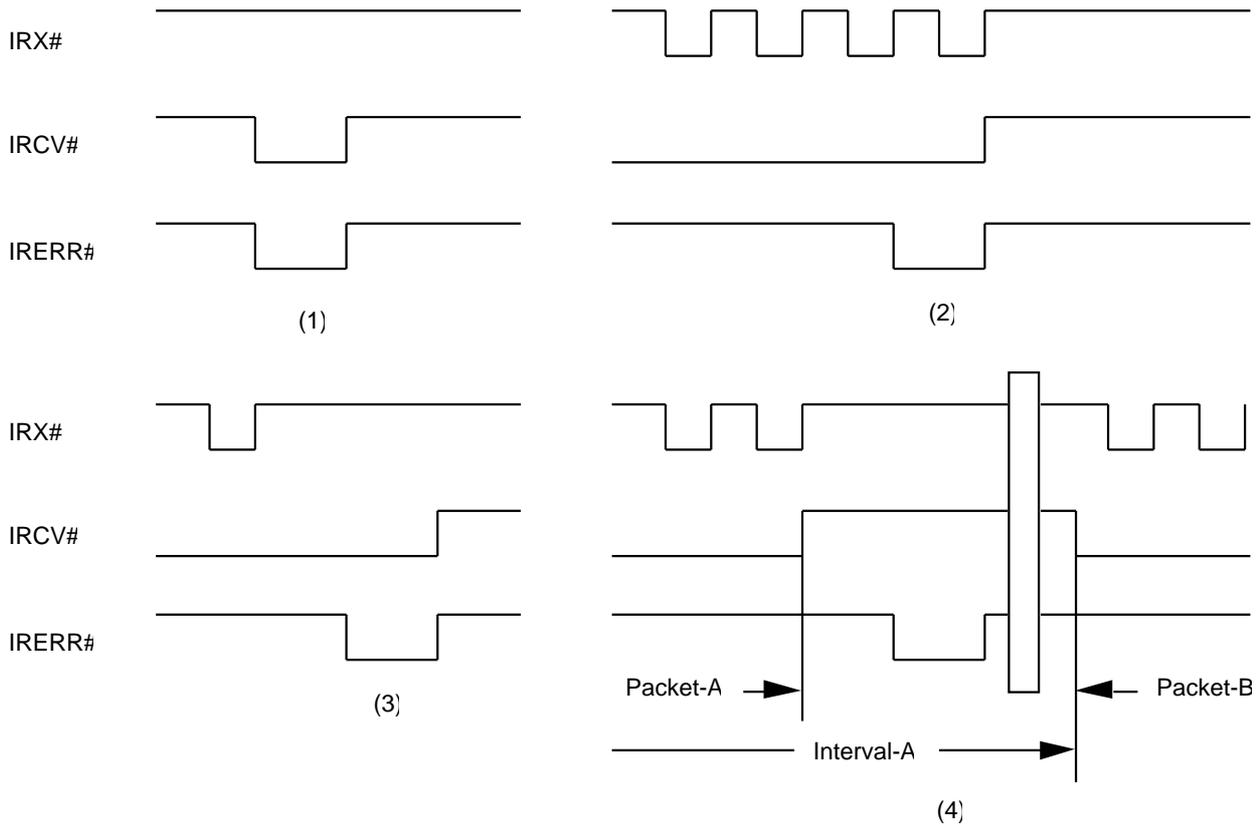


Figure 6.6.2.1 Appearing Pattern of IRERR#

6.7 Difference in Timing of 100MHz, 200MHz, or 400MHz

During packet reception at 100MHz, 200MHz, or 400MHz, timing is different as shown in Fig. 6.7.2. The packet received from the IDATA bus at the rate of 400MHz is generally output at the intervals of 1 clock (25MHz) for ICLK, or every 2 clocks (12.5MHz) at 200Mbps, or every 4 clocks (6.25MHz) at 100Mbps. At 100Mbps, however, two words of a certain quadlet (16 bits) are output every 2 clocks of ICLK as shown in Fig. 6.7.1. In the case of overhead of header's CRC computation, some timing may result in more extended intervals.

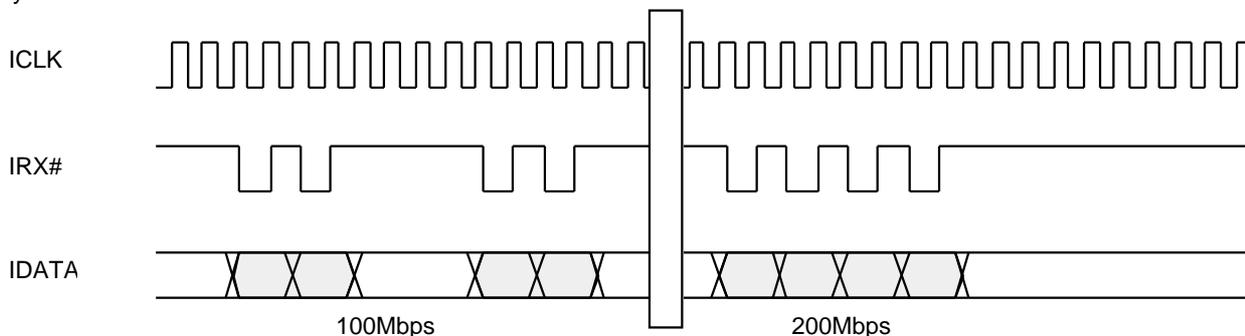


Figure 6.7.1 100, 200Mbps Timing (IBPS=Low: MD8413 compatible mode)

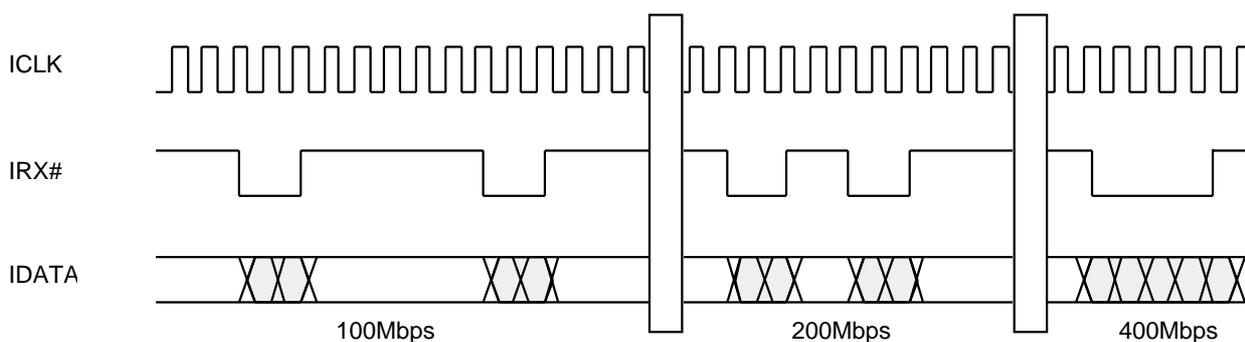


Figure 6.7.2 100, 200 and 400Mbps Timing (IBPS=High: 400Mbps mode)

6.8 Isochronous Bus Timing (Example)

Figures 6.8.1.1 and 6.8.2.1 show examples of Isochronous bus timing. On the both way IDATA bus, Mark □ shows a condition of input into the MD8430, Mark ◻ shows a condition of output from the MD8430, and Mark ■ shows a condition of don't care. Since the descriptions in these figures are arranged for easy understanding, the timing with the signals of ICLK or below is not very accurate in regard to the contents of IEEE1394 BUS Status.

6.8.1 Transmission Timing (Example)

Figures 6.8.1.1/6.8.1.2 show examples of transmission timing. Fig. 6.8.1.1 shows the MD8430-compatible mode. The Iso Bus of the MD8430 can have the same timing of the MD8413 by setting the IBPS pin at Low. In the example of the figure, the ICS for showing the start of the Isochronous Cycle is asserted and the system starts transmission with that cycle. The MD8430 places a request for the 2-Quadlet pre-reading of the Packet-A data. Succeeding the ICS, the CT is used to indicate that only cycle\_time\_data in the CycleStart packet is output to the outside. If any external system uses this value, no generation of IRERR# is confirmed till the negate timing of the CT signal and the CycleTimer counter of the external system is updated. Since then, remaining transmission data are read from the external system upon permission of transmission from the PHY and the resultant data are handed to the PHY. The external system sends out an announcement of the end of packet to the MD8430 by the use of IEOP#, and completes the transmission of Packet-A. If transmission of packets is further attempted in a different channel in the Isochronous Cycle at that time, the ITREQ# signal is kept asserted. This action enables the MD8430 to continue pre-reading of Packet-B that is the next packet. When data transmission of Packet-B is completed and there is no more transmission packet in that cycle, such a condition is told to the MD8430 by negating ITREQ# before the IEOP# timing of Packet-B.

### 6.8.2 Reception Timing (Example)

Fig. 6.8.2.1 shows an example of reception timing. In the example of the figure, the two packets of Channels A and B are continuously received in the Isochronous Cycle. At that time, whether the upper/lower byte of the data is valid or invalid on each IDATA bus is shown by the BE# signal. Information about the channel and SYNC in the header of the received packet data to be output successively in synchronization with the falling of IRCV# is sent to the external system by the use of the CH and SYNC signals. After the reception of Packet-B, the transmission packet of Packet-C having been already requested by the external system (pre-reading of 2 Quadlets of that packet data already finished) is sent to the serial bus. To accomplish the next packet transmission further in that cycle, the external system asserts ITREQ# also on the IEOP# of Packet-C and hence the MD8430 places a request of pre-reading for Packet-D. The MD8430 performs reception processing for Packet-E since it is a receiving packet in higher preference, not Packet-D on the serial bus.

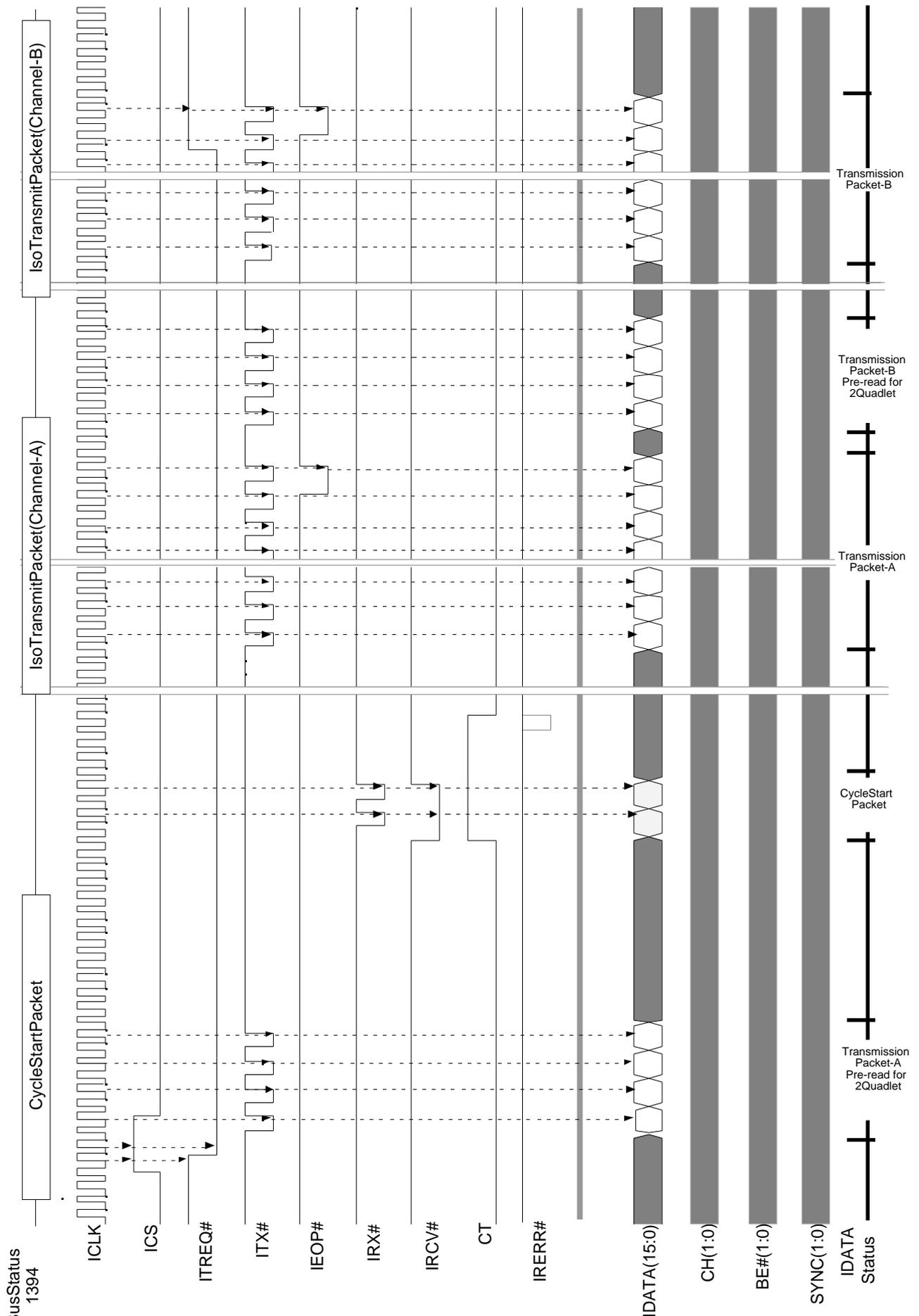
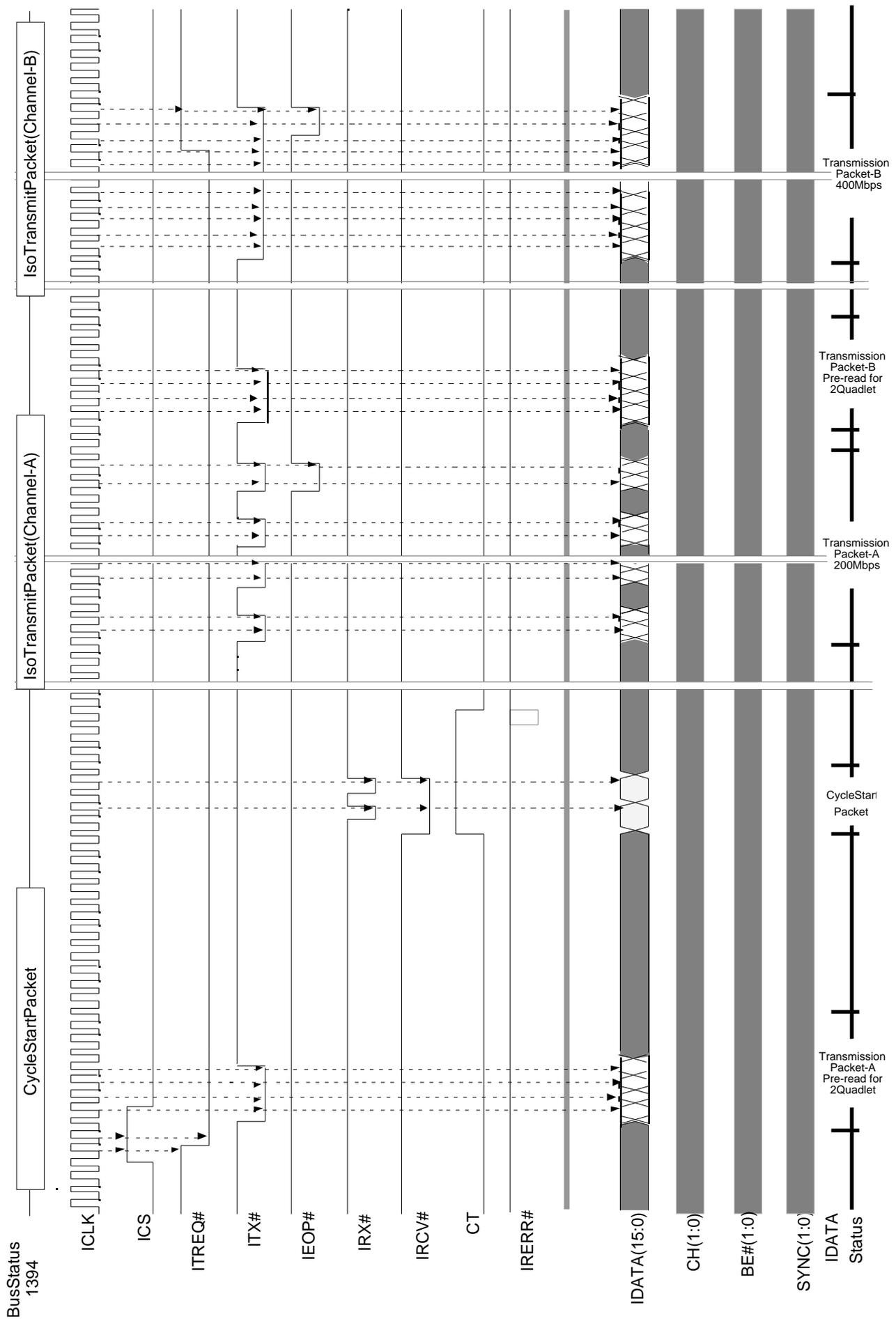


Figure 6.8.1.1 Transmission Timing (MD8413 compatible mode:IBPS=Low)



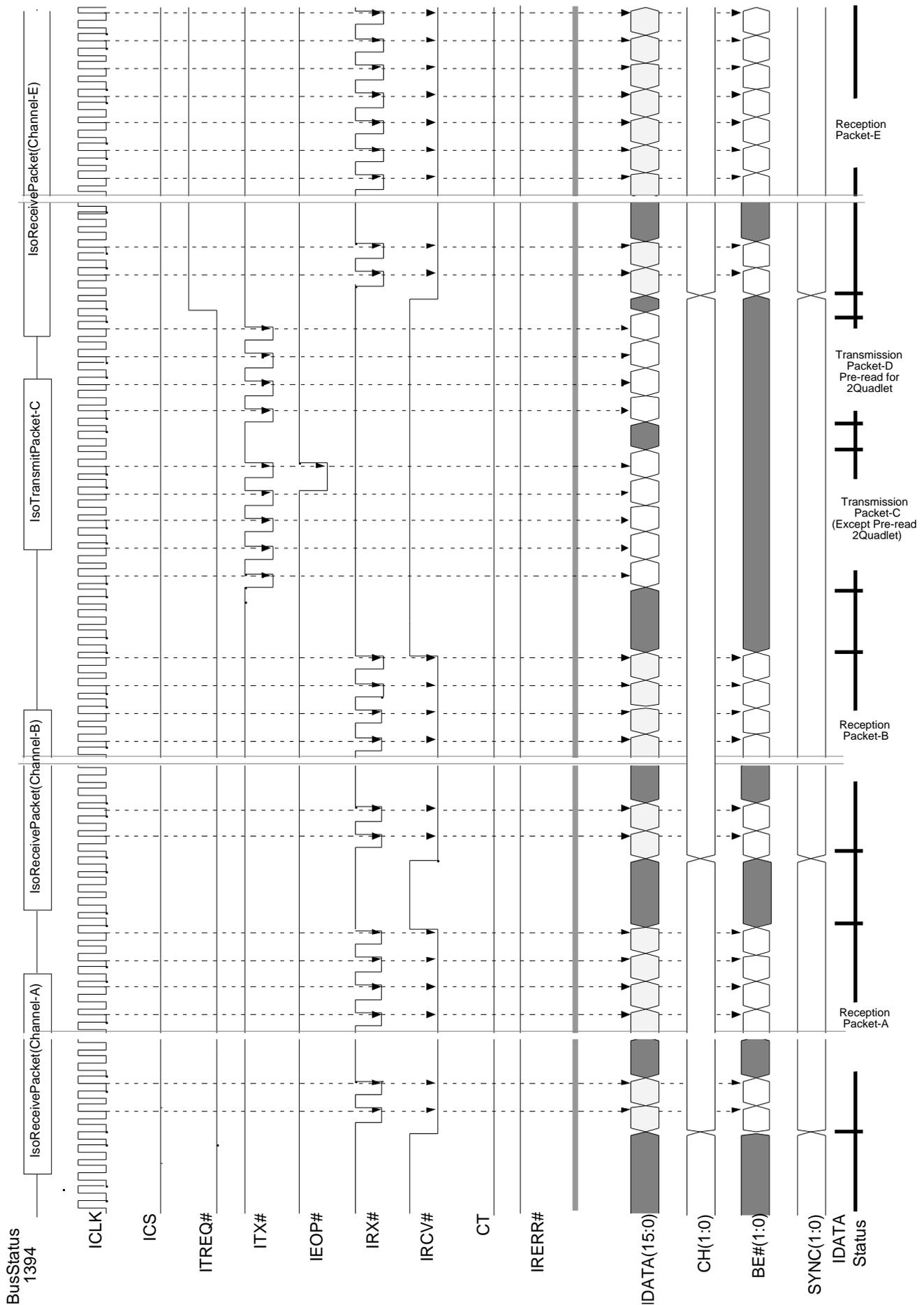


Figure 6.8.2.1 Reception Timing

## 7 Electrical Characteristics

## 7.1 Absolute Rating

Table 7.1.1 Absolute Rating

(VSS = 0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	-0.3 ~ +7.0	V
VIN	Input voltage	-0.3 ~ VDD+0.3	V
IIN	Input current	+ -10	mA
TSTG	Storage temperature	-40 ~ +125	°C

## 7.2 Recommended Operating Condition

Table 7.2.1 Recommended Operating Condition

(VSS = 0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	3.00 ~ 3.60	V
VIN	Input voltage	0 ~ VDD	V
TA	Ambient temperature	0 ~ +70	°C

## 7.3 DC Characteristics

Table 7.3.1 DC Characteristics

(VSS =

Symbol	Item	Terminal	Test condition	MIN	TYP	MAX	Unit
VIH	Input high voltage	SCLK,CTL,		VDD-0.7			V
		Other than above		2.0			
VIL	Input low voltage	SCLK,CTL,				VSS+0.7	V
		Other than above				0.8	
IIH	Input high current		VIN=VDD	-10		10	uA
IIL	Input low current		VIN=VSS	-10		10	uA
VOH	Output high voltage	LPS,LREQ,CTL,D	IOH= -12mA	2.4			V
		Other than above	IOH=-8mA	2.4			
VOL	Output low voltage	LPS,LREQ,CTL,D	IOL= 12mA			0.5	V
		Other than above	IOL= 8mA			0.5	
IOZ	Output disable current		VOUT = VDD or VSS	-10		10	uA
IDD	Dimanic power supply current (3.3V)	VDC	VDD=3.3V				mA

## 7.4 AC Characteristics

Table 7.4.1 Host Interface AC Characteristics (Idle Cycle)

Symbol	Item	MIN	TYP	MAX	Unit
TCSS	CS#, DACK# setup time	0			nS
TCSH	CS#, DACK# holding time	5			nS
TADS	Address setup time	0			nS
TADH	Address holding time	5			nS
TDREQD	DREQ output lagging time	80		130	nS
TRW	Read&write pulse width	60			nS
TRWC	Read&write cycle time	120			nS
TDTD	Read data output lagging time	3		20	nS
TDTH	Read data output holding time	3		15	nS
TWRDS	Write data setup time	10			nS
TWRDH	Write data holding time	5			nS
TRSW	Reset pulse width	160			nS

(Load capacitance: 50pF)

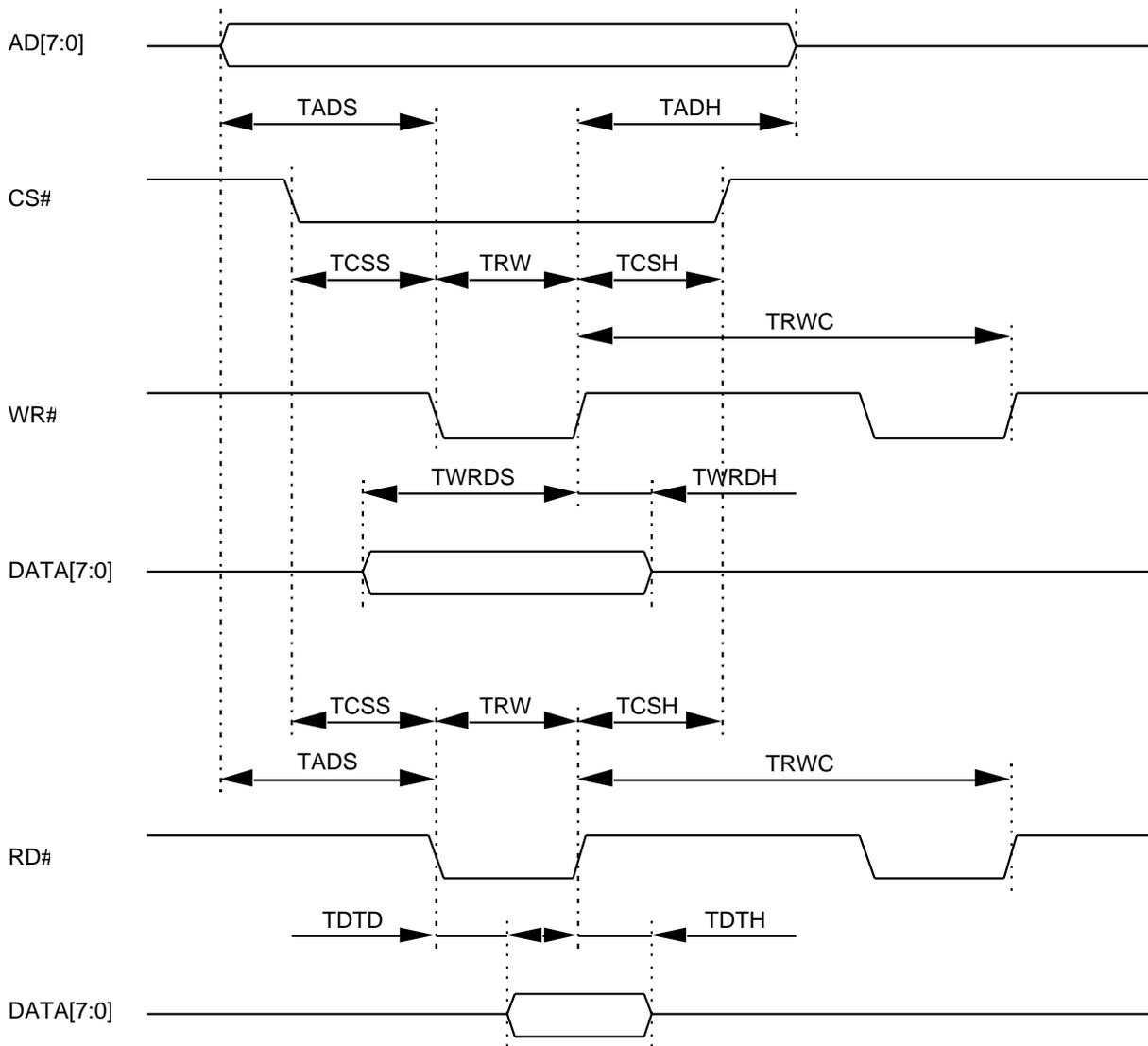


Figure 7.4.1 Host Interface AC Characteristics (Idle Cycle)

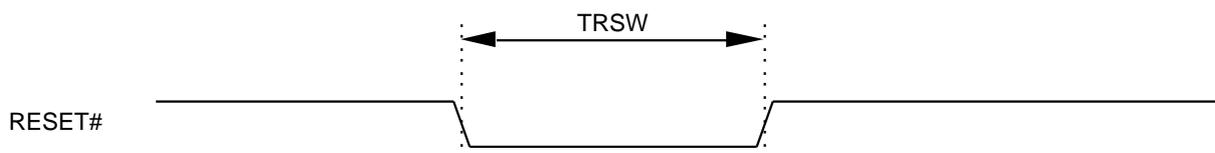


Figure 7.4.2 Host Interface AC characteristics (RESET#)

Table 7.4.2 Host Interface AC Characteristics (DMA Cycle)

Symbol	Item	MIN	TYP	MAX	Unit
THRQD	HREQ output lagging time	1		20	nS
THAKS	HACK setup time	15			nS
THAKH	HACK holding time	0			nS
TADD	Address output lagging time	1		20	nS
TRWD	Read/Write output lagging time	1		20	nS
TDTD	Write data output lagging time	1		20	nS
TRDDTS	Read data setup time	15			nS
TRDDTH	Read data holding time	0			nS
TRDYS	REDY# setup time	15			nS
TRDYH	REDY# holding time	0			nS
TWITS	WAIT# setup time	15			nS
TWITH	WAIT# holding time	0			nS
TCYCD	CYCLEOUT output lagging time	5		15	nS
TCYCH	CYCLEOUT high level time		62.5		uS
TCYCL	CYCLEOUT low level time		62.5		uS

(Load capacitance: 50pF)

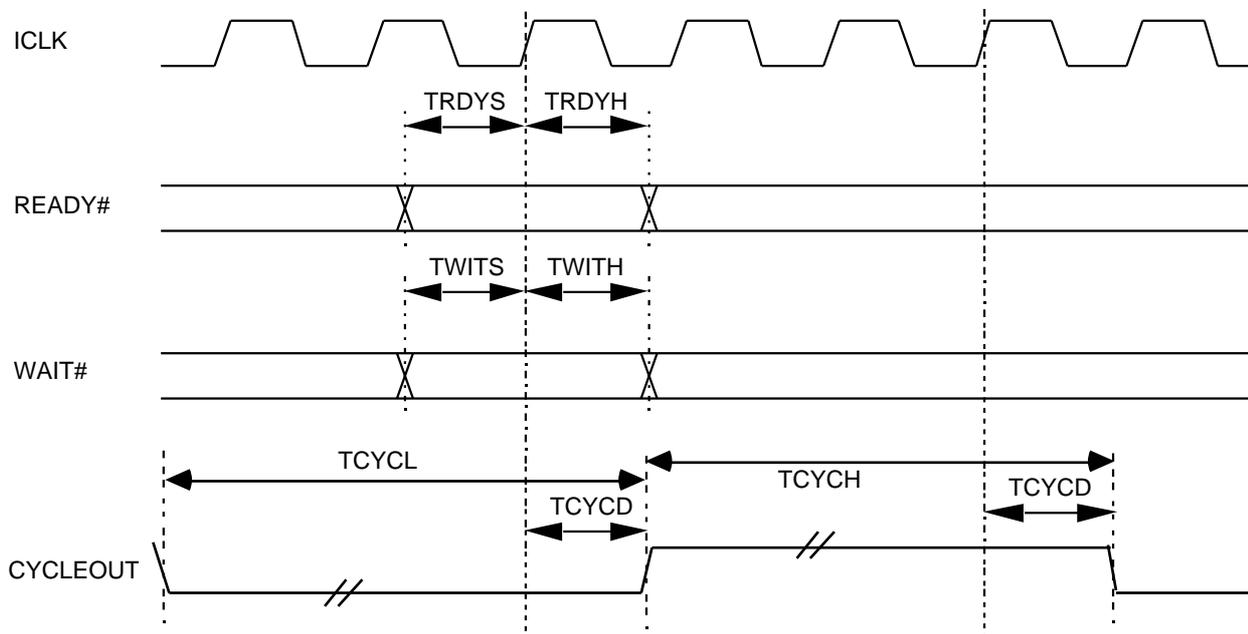


Figure 7.4.3 Host Interface AC Characteristics (DMA Cycle)

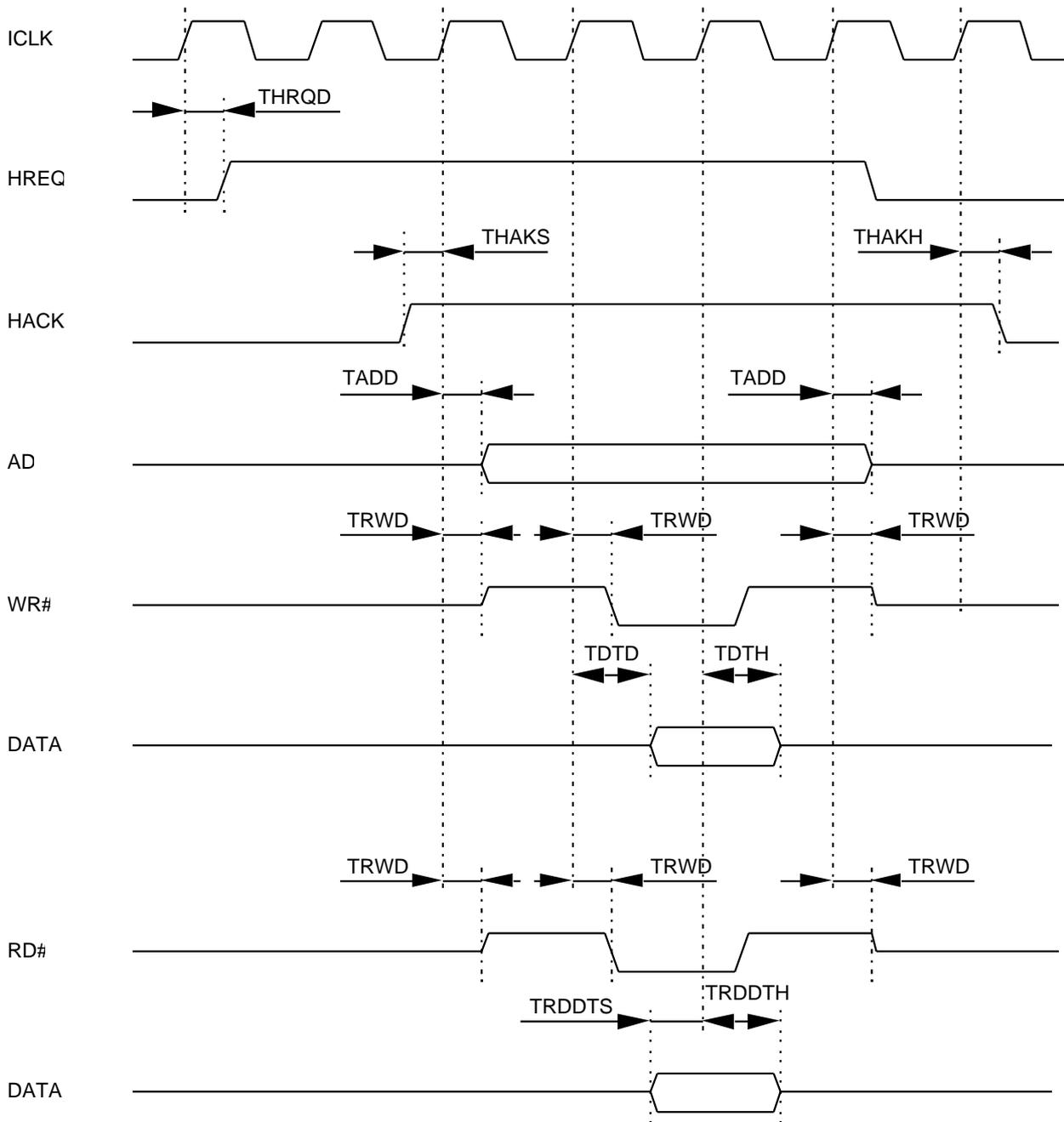


Figure 7.4.4 Host Interface AC Characteristics (DMA Cycle)

Table 7.4.3 PHY Interface AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit
TCTD	Control output lagging time	3		13	nS
TDC	Data output lagging time	3		13	nS
TCTS	Control setup time	6			nS
TCTH	Control holding time	0			nS
TDS	Data setup time	6			nS
TDH	Data holding time	0			nS
TLRD	LREQ data output lagging time	3		13	nS
TSCKC	SCLK cycle time	20			nS
TSCKH	SCLK high level time	8		12	nS
TSCKL	SCLK low level time	8		12	nS
TLPSC	LPS cycle time	360		570	nS
TLPSH	LPS high level time	175		290	nS
TLPSL	LPS low level time	175		290	nS

(Condition: Load capacitance 20pF)

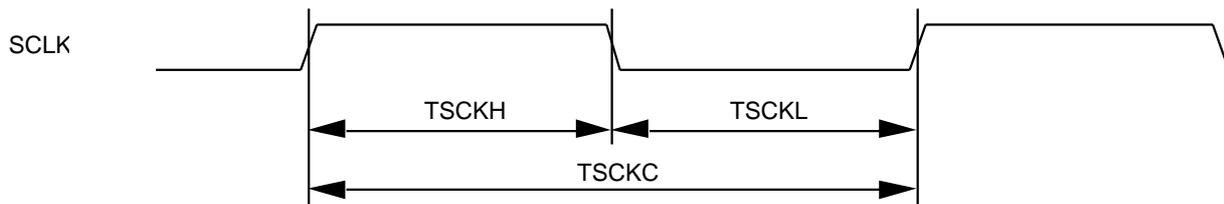


Figure 7.4.5 PHY Interface AC Characteristics (SCLK)

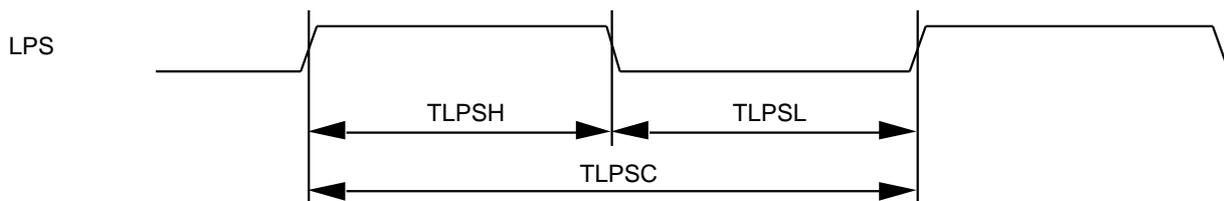


Figure 7.4.6 PHY Interface AC Characteristics (LPS)

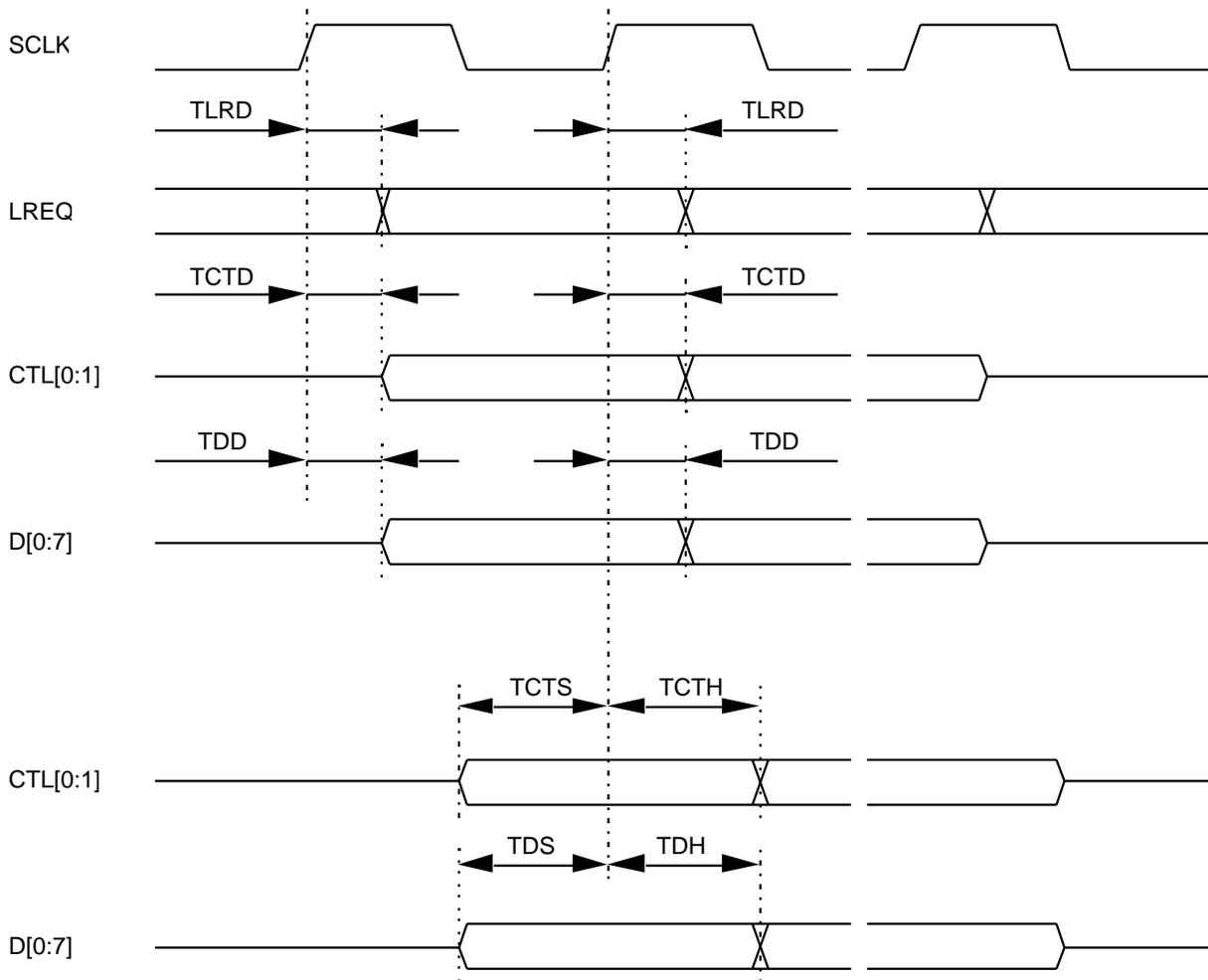


Figure 7.4.7 PHY Interface AC Characteristics (LREQ, CTL, D)

Table 7.4.4 Isochronous Bus AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit
TICKD	ICLK output lagging time	2		12	nS
TICSD	ICS output lagging time	2		14	nS
TITRS	ITREQ# setup time	20			nS
TITRH	ITREQ# holding time	0			nS
TITXD	ITX# output lagging time	2		14	nS
TIEPS	IEOP# setup time	20			nS
TIEPH	IEOP# holding time	0			nS
TIDTS	IDATA[15:0] write setup time	8			nS
TIDTH	IDATA[15:0] write holding time	0			nS
TIRXD	IRX# output lagging time	2		14	nS
TIRVD	IRCV# output lagging time	2		14	nS
TIDFD	IDATA[15:0] output lagging time (IRCV#)	1		5	nS
TIDTD	IDATA[15:0] output lagging time (ICLK#)	2		14	nS
TIDRD	IDATA[15:0] output holding time	0		4	nS
TBCSD	BE#, CH, SYNC output lagging time	2		14	nS
TIERD	IRERR# output lagging time	2		14	nS
TCTD	CT output lagging time	2		14	nS
TBRSTD	BUSRST output lagging time	2		14	nS

(Condition: Load capacitance 50pF)

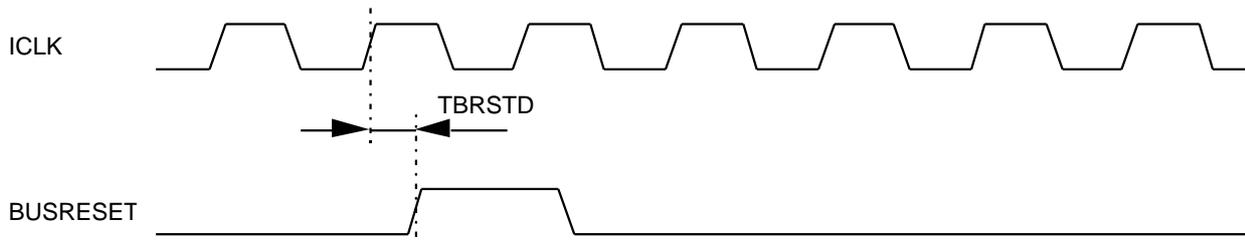


Figure 7.4.8 Isochronous Bus AC Characteristics (BUSRESET)

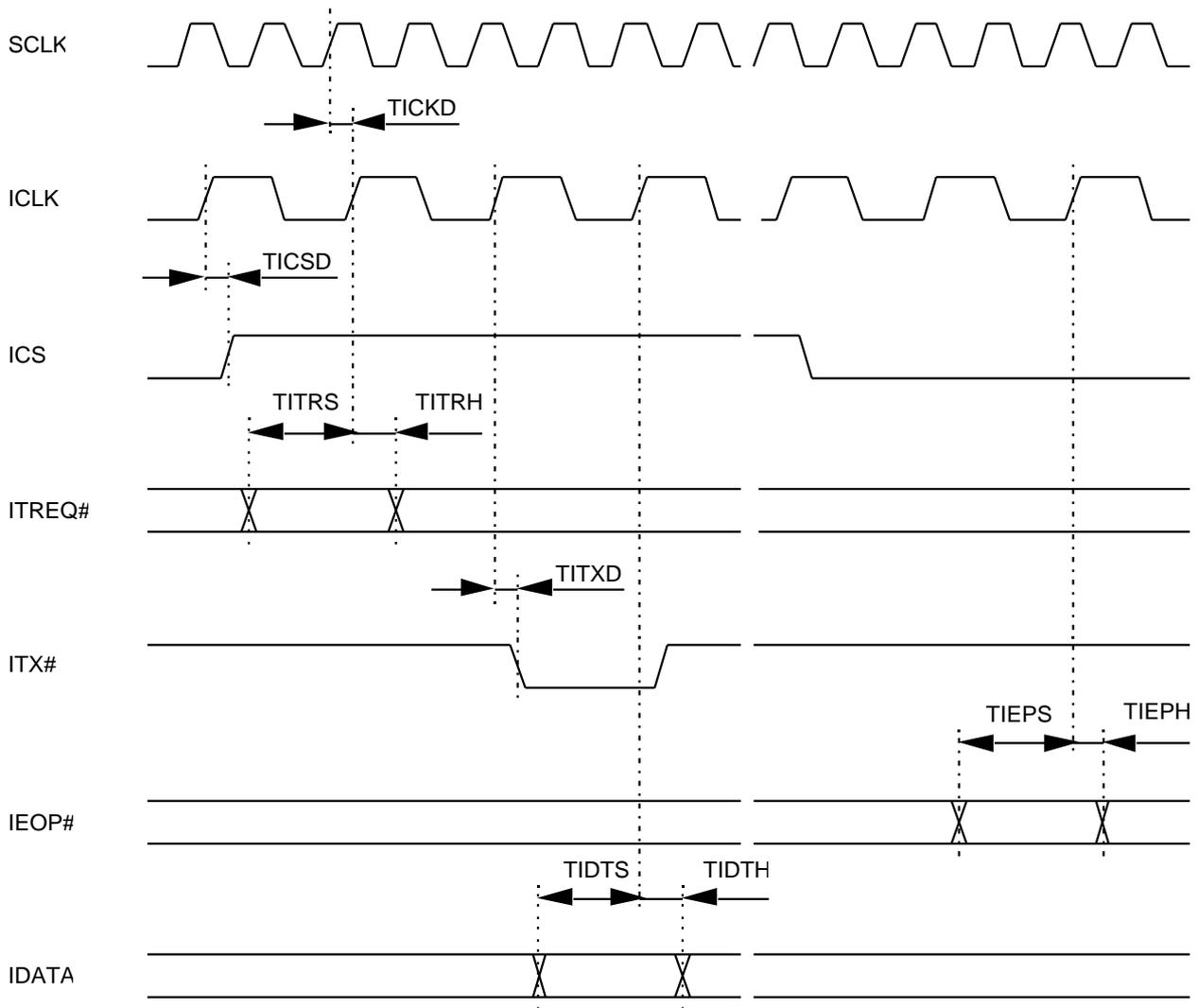


Figure 7.4.9 Isochronous Bus AC Characteristics

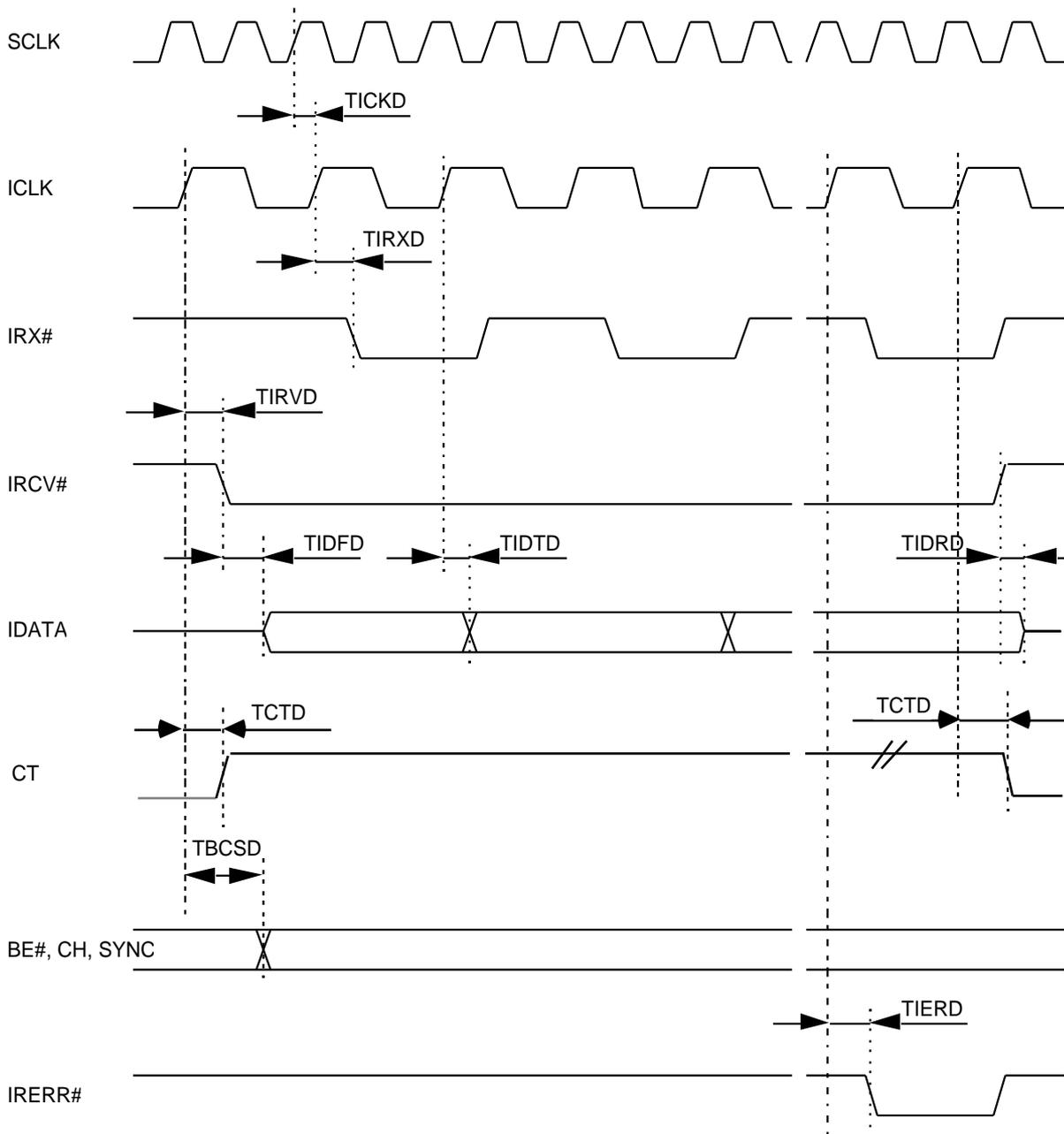


Figure 7.4.10 Isochronous Bus AC Characteristics

8 Terminal Arrays and Outline Drawings

8.1 Terminal Arrays

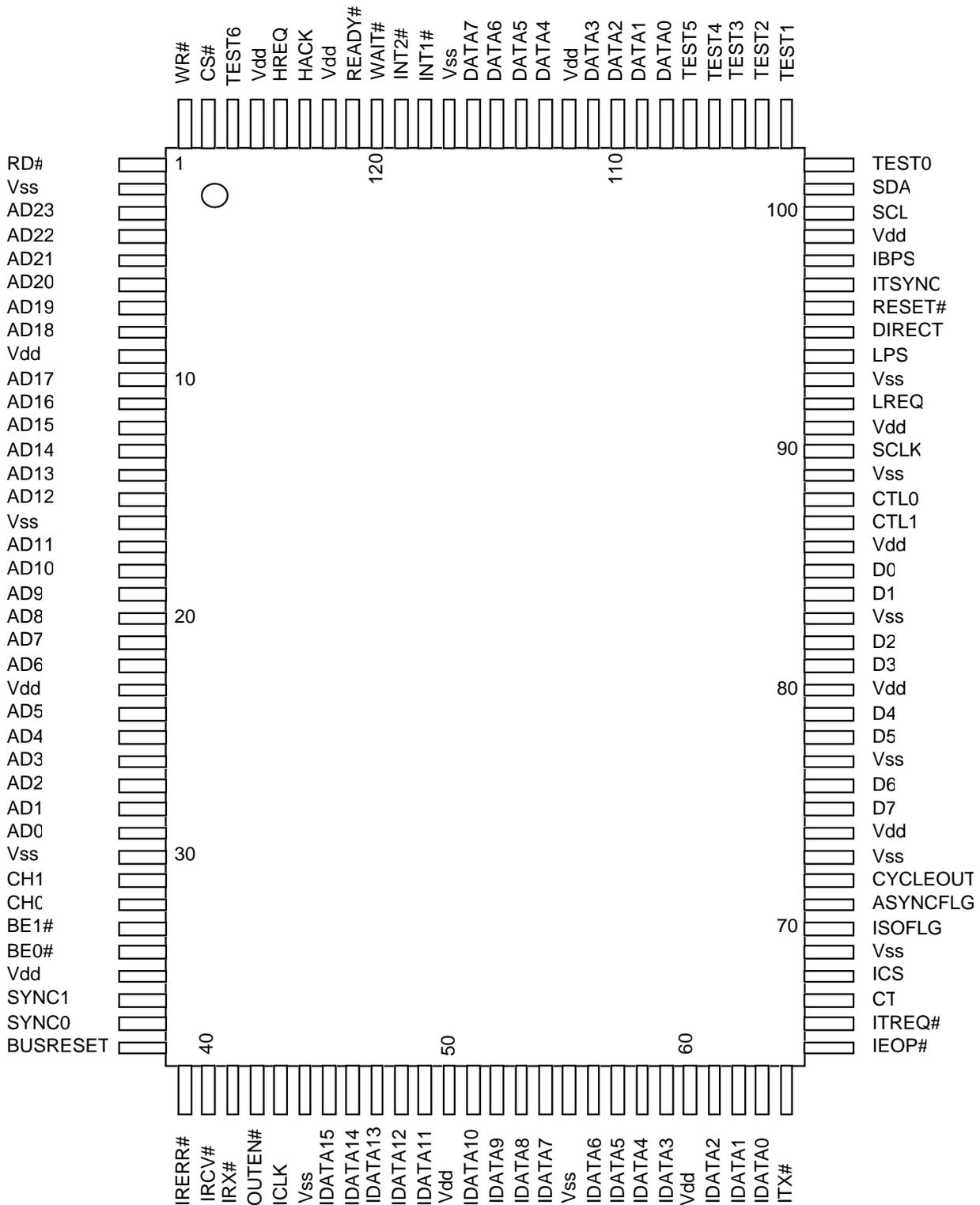
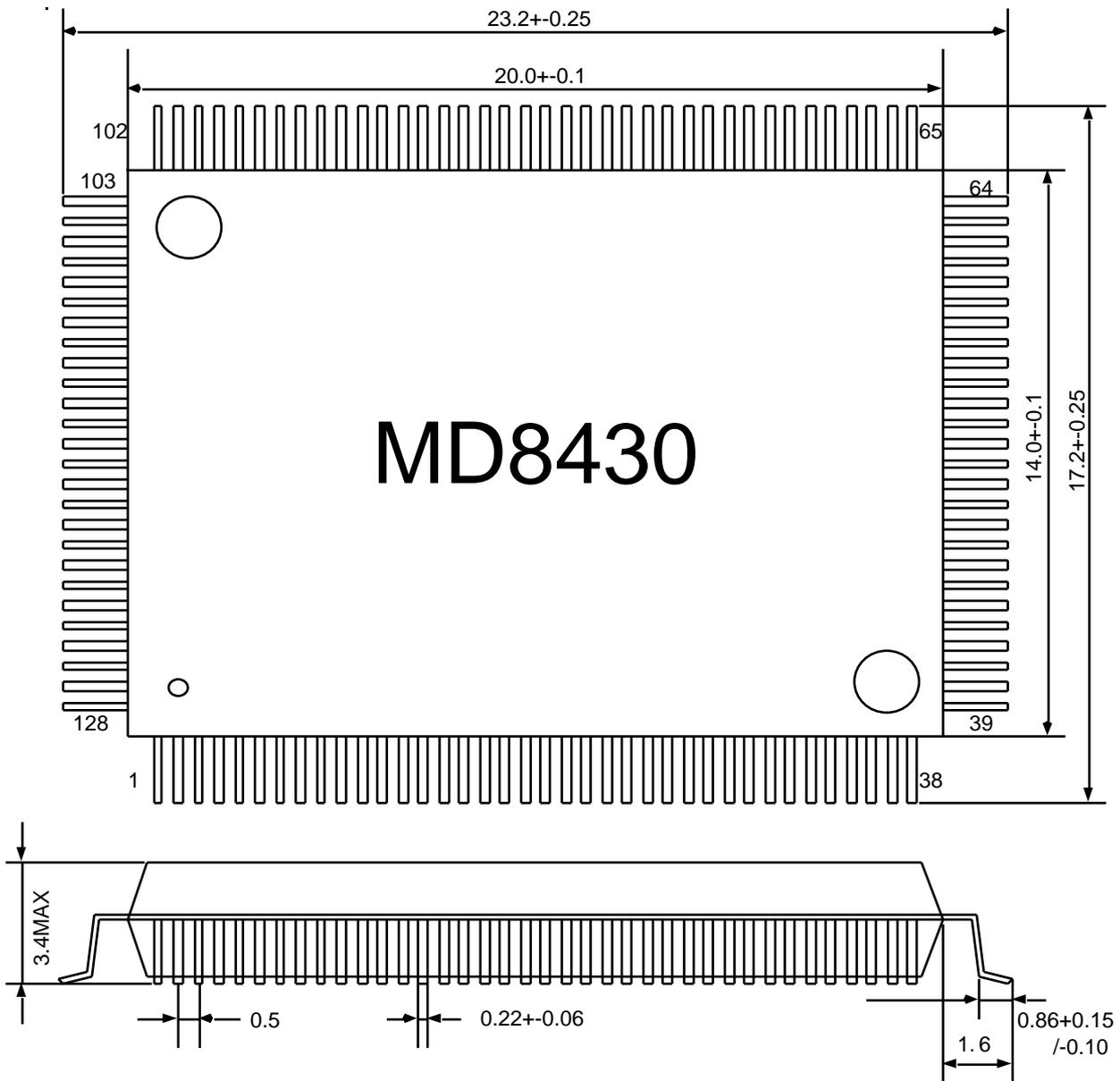


Figure 8.2.1 Terminal Arrays

## 8.2 Outline Drawings



## 9 Errata

### 9.1 LocalSize Register

This register is asked not to write in 0 at unused time. 0 cannot establish size at an unused table. Please establish each bit of Read/Write/Lock of AccessFlag Register in 0 as a countermeasure.

In this case please establish a part of Always1 in 1 by all means in addition to above.

Because size setting is Quadlet unit, please establish it 4byte minute big than it is used. (an example: When there is 16byte access domain, please establish it with 00010100b in LSize[7:0].)

When Destination Address is same, a small thing of table number is effective. Accordingly when it is used an address same as used destination address as an unused table, give a big table of number by all means as an unused table.

### 9.2 Auto Mode

When it is used Auto Mode by Isochronous transmission of a message, please input IEOP at packet end point in time.

Because I have started point reading of the next packet with next IsoCycle when there is not this input, there is the danger that adjustment of data length is not produced.

If point reading share (1Quadlet) is always the System that can be prepared, there is not this need.

### 9.3 Config ROM Access

MD8430 does not consider bootup time of EEPROM. Accordingly reset time of MD8430 needs to be extended till it gets possible to be used after power on of EEPROM of use.

It depends on EEPROM of use, but a WHAT'S COOL does use of PowerOn Reset pulse more than 200msec.

If EEPROM was switched on, reset pulse to need for MD8430 is more than 10 m sec.

## 10 Note

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