

IEEE 1394LINK Layer Controller (MD8413)

General Descriptions

The MD8413 is a controller for high-speed serial-bus link layers, arranged in accordance with IEEE 1394 - 1995. It has all necessary functions for the link layer as a matter of course, and it also offers maximum transfer performance and variable system applications building with an isochronous transfer, by gaining access to the outside through an exclusive bus.

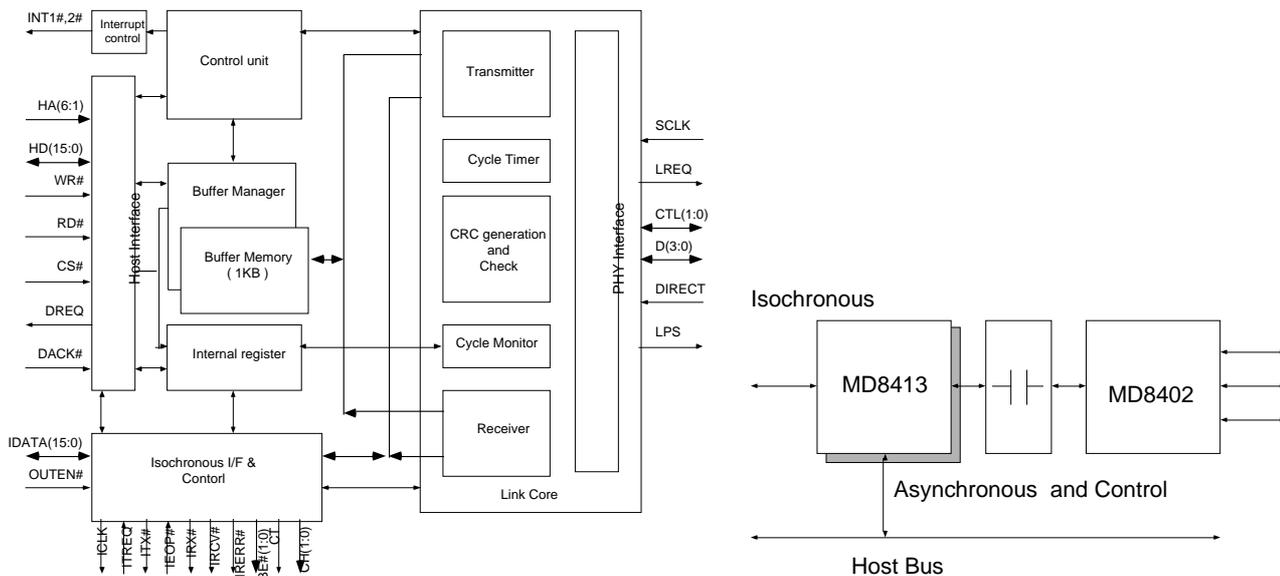
Features

- Packing for transmission and unpacking for reception, according to IEEE 1394 - 1995
- Supporting the CycleMaster
- Parity generation and error detection by 32-bit CRC
- Detection of dropped cycle start messages
- Support of both AC and DC coupling connections with PHY Interface
- Controlling the transfer number for each cycle during isochronous transfer
- Automatic insertion of a header during transmission and automatic separation of the header during reception for the isochronous packet
- Full support of the out-bound retry sequence
- Data bus for exclusive isochronous send/receive
- Support of control signals toward LPS (Link Power Status) of PHY (MD8402)
- Supporting the bus time register

Applications

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|--|---------------|-----------------|------------------------------|
| ■ Digital camera | ■ Digital VTR | ■ Digital audio | |
| ■ Electronic musical instruments(MIDI) | | ■ Scanner | ■ Printer |
| ■ Various storages | ■ DVD | ■ Set-top box | ■ Hardware 1394 Bus Analyzer |

Internal block diagram



Package Outline

100 pin LQFP

Power Voltage

3.3 volts

Functional outlines**Host interface**

The host interface consists of an asynchronous bus with a 16-bit width like the SRAM. Since DMA control support functions are accommodated inside, the DREQ signal can be produced according to the status of buffer, in order to realize high-speed data transfer. Data access to the MD8413 is made in the Big Indian mode.

All registers can be directly accessed from the host. Inner buffer selection is performed by DMA transfer, and it is possible to gain access to the selected buffer.

PHY interface

An interface is available, which enables direct connection with the PHY chip to process a physical layer according to IEEE 1394 - 1995. Either 100Mbps or 200Mbps is acceptable for the PHY chip to be connected.

In the IEEE 1394 - 1995, the connection mode for the PHY and LINK chips is classified to the following two kinds:

- DC connection
- AC connection

This IC supports both kinds of connections.

Transmitter

The transmitter reads out data from the MD8413's internal asynchronous transmission buffer or the isochronous transmission data bus, and performs formatting into each packet format defined in IEEE 1394 - 1995. The resultant packet is sent to the PHY interface. When the CycleMaster bit is "1" and the node employing the MD8413 is a root, a cycle start packet is also sent out to indicate the head of the isochronous cycle.

Receiver

The receiver receives a packet from the PHY interface and identifies if this packet is the one to be accepted by the MD8413 node. If it has been identified as an asynchronous packet, judgment is made with the node address of the MD8413. If it is an isochronous packet, judgment is made with the preset channel number. If it is a packet headed to this node, it is written in the asynchronous reception buffer and data output is transferred to the isochronous data bus. In the case of broadcast packet and snoop mode, no judgment is made and data are written in the respective buffers, transferring output to the data bus.

Built-in buffer

The MD8413 has a built-in buffer with a capacity of 276x32 (bits) configuration for 1K-byte + 20 quadlets in total, to be used for asynchronous transmission and reception. This is a temporary buffer intended for the data-rate absorption between the transmitter and the host bus. The host performs data access to this buffer.

The host splits this buffer in advance for asynchronous transmission and reception. Designation of each buffer size is set at the register. The status information concerned with the grade of vacancy and congestion in the buffer can be picked up by the host in the split unit.

Isochronous transfer functions

The MD8413 has an isochronous function. Since a cycle timer is incorporated, a cycle start packet can be transmitted every 125μsec when the node employing the MD8413 is the CycleMaster. This cycle is produced from the 49.152MHz clock entered from the PHY chip and the trigger is an 8kHz signal entered from the CYCLEIN pin.

If the CycleMaster is not used, synchronism with the CycleMaster is established while making compensation for the cycle timer inside the MD8413 using the value in the packet, each time a cycle start packet is received from another CycleMaster node.

The MD8413 has two types of isochronous modes. HOST is a mode used to gain access to the host in a packet image, and the other is a mode for host access in an image of data stream.

The user determines the mode according to the nature of data source to be handled in isochronous transfer mode. For isochronous packet access with the outside, synchronous transfer is effected using an exclusive isochronous data bus. In this case, data control with the outside is effected by the MD8413 that functions as the master.