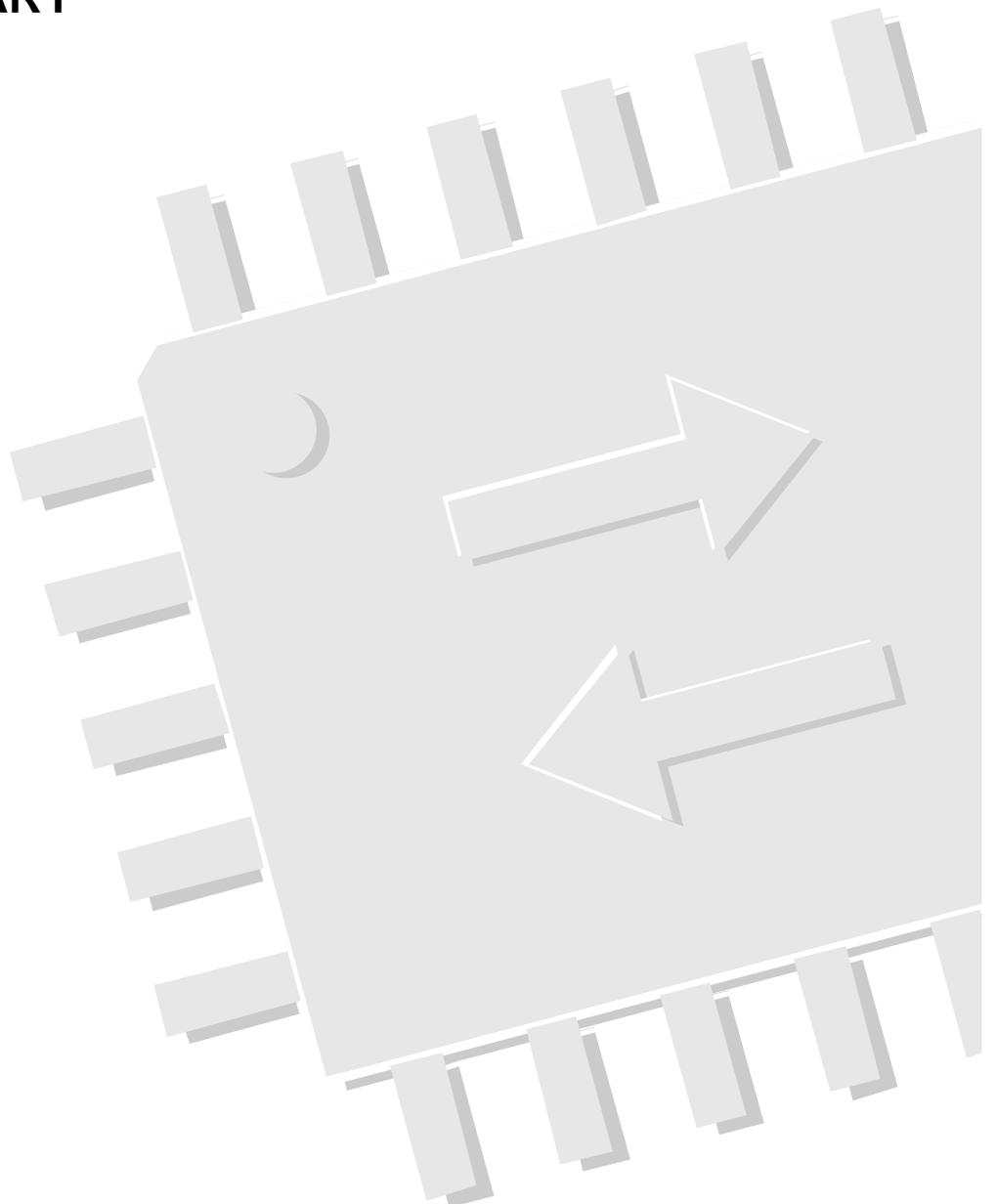


# PHY (IEEE 1394)

# MD8402

Users Manual

**PRELIMINARY**



MEMO

**History**

Rev.	Date	Comments
0.1	11/26/1996	Original
0.2	2/28/1997	3-2-7 Register6,3-2-8 Register7,8
0.3	4/4/1997	Figure1-1 MD8402 Block Diagram Table2-1,Table2-2 MD8402 Terminal Table(1),(2) Table6-3 DC Characteristics Figure7-1 Terminal Arrays Figure8-1 MD8402 Recommended circuit

## Keys

<b>MSB,LSB of Data</b>		:MSB on the left and LSB on the right
<b>Negative logic signal description</b>		:Attached with # at the last end of signal name
<b>Numeral description</b>	:Binary	****b or ****
	Decimal	****
	Hexadecimal	****h
<b>Terminology</b>	:Byte	Data in 8-bit width
	Word	Data in 16-bit width
	Quadlet	Data in 32-bit width
	Octlet	Data in 64-bit width

## Associated Materials

IEEE P1394 Draft 8.0v1 Standard for a High Performance Serial Bus

IEEE Std 1212-1991 Command and Status Register architecture

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## 1 Introduction

The MD8402 is a 200/100Mbit/sec physical channel interface chip for IEEE 1394. It provides a three port twisted pair interface, a interface to a link layer IC, packet data resynchronization and regeneration, and bit level arbitration/initialization logic. The circuitry implements the lower layer of the IEEE 1394 protocol (the electrical parts of the Physical Layer) and interfaces with the 1394 Link Layer.

### 1-1 Features

- Low voltage swing and low current differential transceivers meeting IEEE 1394 requirements.
- Operates at 196.603 and 98.304 Mbit/sec IEEE 1394 data rates.
- Cable Active detects if a port is connected to a active node.
- Automatically shuts down inactive ports to conserve power.
- Speed Signaling to support the multiple data rates.
- Bus initialization and arbitration state machine logic.
- Resynchronizer to synchronize the received data to the local Serial Bus clock.
- Link-On runt packet recognition.
- DS Link encoding decoding.
- Random number generator for resolving initialization contention.
- PLL freq. multiplier to generate the 196.603 MHz clock.
- Supports both direct connect and isolated Phy-Link Interface.
- Cable Power Status detects if the cable power is undervoltage.
- Link Power Status detects if the Link is powered.
- Configuration Management Capable and Power Class description pins.
- Independent TpBias's.

### 1-2 Applications

- |                                  |               |                 |
|----------------------------------|---------------|-----------------|
| ■ Digital camera                 | ■ Digital VCR | ■ Digital audio |
| ■ Electronic musical instruments | ■ Scanner     | ■ Printer       |
| ■ Various storages               |               |                 |

### 1-3 Internal block diagram

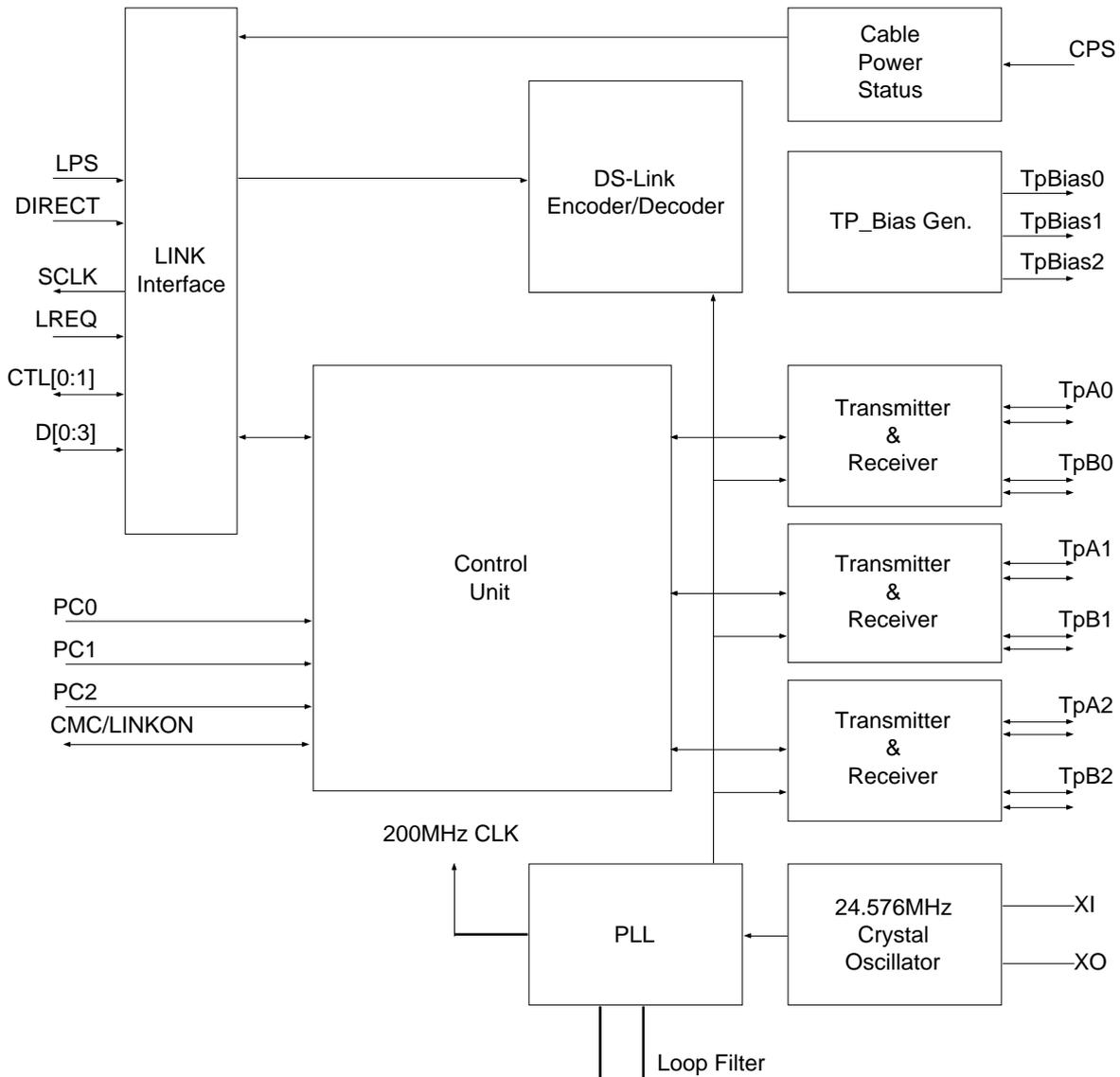


Figure 1-1 MD8402 Block Diagram

### 1-4 Functional outlines

#### 1-4-1 LINK Interface

##### 1-4-1-1 LINK Power Status

The LPS pin is used to detect if the Link is powered up.

If it's low for more than 2.6 $\mu$ s then Link power is considered down and the link interface drivers are tri-stated.

If high for 200ns then the Link is considered powered up and the link interface is re-enabled.

##### 1-4-1-2 LINK On

Link on signal (6.114MHz out) is enable when LinkOn packet is received and LPS is low. When the AC signal is not present the pin's DC level is determined by a external 10k resistor; either pulled high or low depending on the CMC/LINKON pin. Specifically, the pin is an input until the self-id runt packet transmission.

Afterwards, it becomes the LinkOn output. The Link on output is disabled when LPS is becomes high and will not be enabled until reception of a new link command while LPS is low.

### 1-4-1-3 Isolation barrier

The DIRECT input pin is tied low if isolation is present at the Phy Link Interface ie. AC coupled.

The DIRECT is tied high for dc coupled Phy Link interface.

For the solated interface the driver for CTLI[0:1], D[0:3] and LREQ use the digital differentiator circuit. For the dc coupled interface the drivers do not use the digital differentiator and are tri-stated drivers.

## 1-4-2 Twisted Pair Cable Interface

A 4.5 meter cable consists of: a 22 gauge twisted pair for power, two individually shielded 28 gauge 110 $\Omega$  twisted pair for data and clock, and a overall shield. The outer shield is shorted together and connected to chassis ground through a 4700pF cap. in parallel with a 1 megohm resistor.

The cable propagation delay is typically 1.45ns/foot.

The power supply (Vp,Vg) is unregulated 8 to 40 V DC and the maximum current carried by a single cable is 1.5A. A node is not required to be a power source.

Notice that TpA and TpB are connected to TpB and TpA respectively of the adjacent node. This is necessary since the common mode biasing of the transceivers is done at only one end of the cable.

### 1-4-2-1 TpA, TpB Signals

A MD8402 port has two transceivers: TpA and TpB. TpA is used to transmit arbitration bits and packet strobe and to receive packet data and arbitration bits. TpB is used to transmit packet data and arbitration bits and to receive arbitration data and packet strobe. TpA is biased up locally by TpBias and TpB is biased up by the TpBias of the node its connected to.

During packet transmission both TpA and TpB drivers are enabled; TpB transmits the 98.304 or 196.608 Mbit/sec NRZ data while TpA transmits the Strobe. The Strobe signal changes state whenever the data signal does not.

During packet reception both TpA and TpB drivers are disabled and strobe is received on TpB while data is received on TpA.

Just Prior to transmitting a packet outputs a low on TpA and a high on TpB (header) while the MD8402 at the other end of the cable has both the TpA driver and TpB driver disabled. Just after a packet is transmitted the output transitions to the normal termination state of TpA high and TpB low or hold bus state of TpA low and TpB high.

### 1-4-2-2 Drivers and Receivers

The twisted pair signals are balanced differential signals that measure +/-220mV for a high/low and 0V for a Z measured between the conductors. The cables are terminated at each end differentially into 110 $\Omega$ , and are also terminated for AC common mode signals at TpA into 55/2 $\Omega$ .

The twisted pair driver is a high output impedance current switch that outputs +/-4mA differentially for a high/low and 0mA for Z state. The packet receiver is a low offset, high bandwidth receiver. The TpBias pin provides the common mode bias for the local TpA pins and the adjacent nodes TpB pins.

The 0.33uF cap. on TpBias acts as a AC decoupling for the speed signal currents.

The 250pF shunts high freq. common mode noise at the TpB pins.

The 5k resistor is required for cable not active.

### 1-4-2-3 Cable Not Active

The cable not active comparator indicates a No Connect for TpB common mode voltage below the no connect threshold (nominally 0.8V). A external 5k $\Omega$  resistor acts a common mode pull down that drops the common voltage on TpB below the threshold when the cable is not connected to an adjacent node.

### 1-4-2-4 Arbitration - 3 Level Signals

The arbitration comparators are actually sampling comparators that sample on the falling edge of SCLK. The differential thresholds required to detect the 3 level arbitration signals are nominally +110mV and -110mV. A high is detected if the differential signal drops below the negative threshold, and a Z is detected if the differential level is between the two threshold.

A Z state exists only if the drivers at each end are in the Z state.

### 1-4-2-5 Speed Signaling

A 200Mbps speed signal is detected if the TpA common mode voltage drops below the speed signal threshold (nominally TpBias -86mV). The speed signal is transmitted during arbitration.

## 1-4-3 Clock Circuits

### 1-4-3-1 Crystal Oscillator

The oscillator output frequency must be 24.576MHz +/- 100ppm. The crystal is 50ppm and is spec'ed for parallel resonant with a external 10pF loading caps on pins XI and XO to ground respectively.

### 1-4-3-2 PLL

The PLL is used as a frequency multiplier, that provides a 196.608 MHz clock from the 24.576 MHz crystal oscillator output.

## 1-4-4 Miscellaneous Pins

### 1-4-4-1 Cable Power Status

Detects cable power (Vp) undervoltage. Vp is connected to the CPS pin via a series 226k $\Omega$  resistor; the cable voltage drops below a nominal threshold voltage of 7.5V.

### 1-4-4-2 Hardware Reset

Connected to ground via a 0.1  $\mu$  F cap. provides a minimum reset pulse of 15 millisec.

A low on this pin forces all state machines to a known state.

## 2 Terminal Description

### 2-1 Functional description for terminals

pin number	name	I/O	contents
1,24,25,26,27,28,79, 80,81	NC		No Connect.
2,6,10,13,15,19,23,30, 31,32,33,34,37,73,74, 75,76,77,82,83,84,85, 86,87,90,91,100	DVSS		ground.
3	LPS	I	Link Power Status. It's the purpose of detecting in the Link's power status. 0 : Power Down 1 : Power Up
4,8,12,14,17,21,29,35, 36,78,95	DVDD		power.
5	LREQ	I	Link Request. Read/Write of the PHY Register.
7	SCLK	O	49.152MHz the Link system clock.
9,11	CTL[0:1]	I/O	Control signal for the Link interface.
16,18,20,22	D[0:3]	I/O	Data signal for the Link interface.
38	Purb	I	External cap. connected for Power Up Reset. It is connected to DVSS via a 0.1 $\mu$ F cap.
39,41,47,55,58	AVDD1		Analog circuit power 1.
40,44,48,49,50,54, 57,88	AVSS		Analog circuit ground.
42,43	XO,XI	I/O	Crystal oscillator inputs.
45	LF	O	Loop Filter input. Charge pump output.
46	VCOR	I	Loop Filter output. VCO input.
51	Vref	I	1.85V (+/- 4%) external reference voltage input. Should be decoupled via 0.1 $\mu$ F.

Table 2-1 MD8402 Terminal Table (1)

pin number	name	I/O	contents
52	Rext	I	A current source reference register. It's connected to AVSS via external register.
53	CPS	I	This pin is used to detect undervoltage of the cable power (Vp). It's connected to Cable power (Vp) via 226k $\Omega$ .
60,59,56	TpBias[0:2]	O	Common Mode cable bias. Should be decoupled 0.33 $\mu$ F.
69,65,61	TpB[0:2]n	I/O	Arbitration/Speed Signal/Data output, Arbitration/Strobe input. Negative signal.
70,66,62	TpB[0:2]p	I/O	Arbitration/Speed Signal/Data output, Arbitration/Strobe input. Positive signal.
71,67,63	TpA[0:2]n	I/O	Arbitration/Strobe output, Arbitration/Speed Signal/Data input. Negative signal.
72,68,64	TpA[0:2]p	I/O	Arbitration/Strobe output, Arbitration/Speed Signal/Data input. Positive signal.
89	AVDD2		Analog circuit power 2.
93,92	TEST[0:1]	I	TestMode control pin. Connect to DVSS.
94	DIRECT	I	Between the Link and the PHY isolation barrier information. 0:AC connection 1:DC connection
96	CMC/LINKON	I/O	Configuration Management Capable 0 : Uncapable 1 : Capable LINKON
97,98,99	PC[0:2]	I	Power Class[0:2]

Table 2-2 MD8402 Terminal Table (2)

## 3 Control Register

### 3-1 Register Access Method

Every register of the MD8402 usually gains access from the LINK layer IC. Accordingly, a detailed method compare with the Users Manual of the LINK layer IC.

### 3-2 Register Contents

#### 3-2-1 Register0

address 00h

7	6	5	4	3	2	1	0
Physical ID						R	CPS

**Bit 0**      **CPS:** Cable Power Status (R - initial value : the CPS pin)  
Cable Power Status.

**Bit 1**      **R:** root indicator (R - initial value : 0000h)  
Indicates that this node is the root.

**Bit 7~2**    **Physical ID:** physical Node ID (R - initial value : 0000h)  
The address of this node determined during self - identification.

#### 3-2-2 Register1

address 01h

7	6	5	4	3	2	1	0
RHB	IBR	GC					

**Bit 5~0**    **GC:** Gap Count (R/W - initial value : 003Fh)  
Gap count value.

**Bit 6**      **IBR:** Indicates Bus Reset (R/W - initial value : 0000h)  
Instructs the PHY to initiate a bus reset at the next opportunity.

**Bit 7**      **RHB:** Root Hold Bit (R/W - initial value : 0000h)  
Instructs the PHY to attempt to become the root during the next bus reset.

**3-2-3 Register2**

address 02h

7	6	5	4	3	2	1	0
SPD		Reserved		NP			

**Bit 3~0 NP:** Number of port (R- initial value : 0003h)

The number of ports on this PHY. (normally 3, '0011')

**Bit 7~6 SPD:** Speed (R- initial value : 0001h)

Indicates the top speed this PHY can handle. (normally 200Mbps, '01b')

**3-2-4 Register3**

address 03h

7	6	5	4	3	2	1	0
AStat0		BStat0		Ch0	Con0	Reserved	

**Bit 2 Con0:** Connected (R - initial value : 0000h)

If = 1, port0 is connected, else disconnected.

**Bit 3 Ch0:** Child (R - initial value : 0000h)

If = 1, port0 is a child, else parent.

**Bit 5~4 BStat0:** Status of TpB0 (R- initial value : 0000h)

TpB line state on port0.

11b = Z

01b = 1

10b = 0

00b = invalid

**Bit 7~6 AStat0:** Status of TpA0 (R- initial value : 0000h)

TpA line state on port0.

11b = Z

01b = 1

10b = 0

00b = invalid

**3-2-5 Register4**

address 04h

7	6	5	4	3	2	1	0
AStat1		BStat1		Ch1	Con1	Reserved	

**Bit 2** **Con1:** Connected (R - initial value : 0000h)

If = 1, port1 is connected, else disconnected.

**Bit 3** **Ch1:** Child (R - initial value : 0000h)

If = 1, port1 is a child, else parent.

**Bit 5~4** **BStat1:** Status of TpB1 (R- initial value : 0000h)

TpB line state on port1.

11b = Z

01b = 1

10b = 0

00b = invalid

**Bit 7~6** **AStat1** Status of TpA1 (R- initial value : 0000h)

TpA line state on port1.

11b = Z

01b = 1

10b = 0

00b = invalid

**3-2-5 Register5**

address 05h

7	6	5	4	3	2	1	0
AStat2		BStat2		Ch2	Con2	Reserved	

**Bit 2** **Con2:** Connected (R - initial value : 0000h)

If = 1, port2 is connected, else disconnected.

**Bit 3** **Ch2:** Child (R - initial value : 0000h)

If = 1, port2 is a child, else parent.

**Bit 5~4** **BStat2:** Status of TpB2 (R- initial value : 0000h)

TpB line state on port2.

11b = Z

01b = 1

10b = 0

00b = invalid

**Bit 7~6 AStat2:** Status of TpA2 (R- initial value : 0000h)

TpA line state on port2.

11b = Z

01b = 1

10b = 0

00b = invalid

### 3-2-7 Register6

address 06h

7	6	5	4	3	2	1	0
LoopInt	CPStatInt	CPStat	IDidIt	Reserved			

**Bit 7 LoopInt:** Loop Interrupt (R/W - initial value : 0000h)

If = 1, the bus is a Loop.

This bit is set to 0b by a hardware reset or by writing a 0 to this register bit.

**Bit 6 CPStatInt:** Cable Power Status Interrupt (R/W - initial value : 0000h)

If = 1, the cable power voltage has dropped to row.

This bit is set to 0b by a hardware reset or by writing a 0 to this register bit.

**Bit 5 CPStat:** Cable Power Status (R/W - initial value : the CPS pin)

Cable Power Status.

**Bit 4 IDidIt:** Indicates Bus Reset initiated (R/W - initial value : 0000h)

When this node initiate bus reset, this bit is 1.

This bit is the same as i of Self-ID packet.

**Bit 3~0 Reserved:** (R - initial value : 0000h)

### 3-2-8 Register7,8

address 07h~08h

7	6	5	4	3	2	1	0
Reserved							

**Bit 7~0 Reserved:** (R - initial value : 0000h)

## 3-3 List of Registers

Address	7	6	5	4	3	2	1	0
00h	Physical ID						R	CPS
01h	RHB	IBR	GC					
02h	SPD		Reserved		NP			
03h	AStat0		BStat0		Ch0	Con0	Reserved	
04h	AStat1		BStat1		Ch1	Con1	Reserved	
05h	AStat2		BStat2		Ch2	Con2	Reserved	
06h	LoopInt	CPStatInt	CPStat	IDidInt	Reserved			
07h	Reserved							
08h	Reserved							

Table 3-1 List of Registers

## 4 Data format

### 4-1 SelfID Packet

After the identification quadlet data shown in Table 4-1 have been saved, an actual SelfID packet is saved. This operation is completed with the last quadlet ID data as shown in Table 4-4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1110b				0	0	0	0

Table 4-1 SelfID Packet Receive format(first quadlet)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID						0	L	gap_cnt				sp	del	C	pwr	p0	p1	p2	i	m									
logical inverse of first quadlet																															

Table 4-2 SelfID Packet Receive format(SelfID Packet #0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID						1	n	rsv	pa	pb	pc	pd	pe	pf	pg	ph	r	m											
logical inverse of first quadlet																															

Table 4-3 SelfID Packet Receive format(SelfID Packet #1, #2, & #3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ackSent			

Table 4-4 SelfID Packet Receive format(last quadlet)

	n	pa	pb	pc	pd	pe	pf	pg	ph
pkt #1	0	p3	p4	p5	p6	p7	p8	p9	p10
pkt #2	1	p11	p12	p13	p14	p15	p16	p17	p18
pkt #3	2	p19	p20	p21	p22	p23	p24	p25	p26

Table 4-5 SelfID Packet Receive format(pn)

**phy\_ID** : physical\_ID field

A node ID of the PHY chip used to send this packet.

**L** : link\_active field

0 = LINK is not active.

1 = Active link and transaction layer are present in this node.

**gap\_cnt** : gap\_count field

A present value of the PHY\_CONFIGURATION.gap\_count field for this node is saved.

- sp** : PHY\_SPEED field  
 00 = 98.304Mbps  
 01 = 98.304 and 196.608Mbps  
 10 = 98.304 and 196.608 and 393.216Mbps  
 11 = Reserved  
 Available speeds are saved.
- del** : PHY\_DELAY field  
 00 = 144ns or less ( $\sim 14/\text{BASE\_RATE}$ )  
 01~11= Reserved.  
 The delay time of the repeater in the worst case is saved.
- C** : CONTENDER field. CMC/LINKON pin.  
 When this field is set and the link\_active field is also set, this node indicates that it can be a bus or isochronous resource manager.
- pwr** : POWER\_CLASS field. PC[2:0] pin.  
 000= The node does not require power supply.  
 001= The node does has its own power supply that can feed a minimum of 15W.  
 010= The node does has its own power supply that can feed a minimum of 30W.  
 011= The node does has its own power supply that can feed a minimum of 45W.  
 100= The node consumes a maximum of 1W of power from the cable.  
 101= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the LINK and upper layers.  
 110= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 5W to enable the LINK and upper layers.  
 111= The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 9W to enable the LINK and upper layers.
- p0 ... p26** : NORT,child[NPORT],connected[NPORT]field  
 11 = Connected to the child node.  
 10 = Connected to the parent node.  
 01 = Not connected to another PHY.  
 00 = This PHY is not offered.  
 The port status is shown.
- i** : initiated\_reset field  
 If it is set, this node has issued present bus reset.
- m** : more\_packets field  
 If it is set, this node indicates that another SelfID packet of this node is closely following.
- n** : Extended field  
 An extension SelfID packet sequence number (value from 0~2).
- r,rsv** : reserved field  
 Reserved.

## 5 Functional Descriptions

### 5-1 LINK Chip Interface

#### 5-1-1 Connection Method

##### 5-1-1-1 DC connection

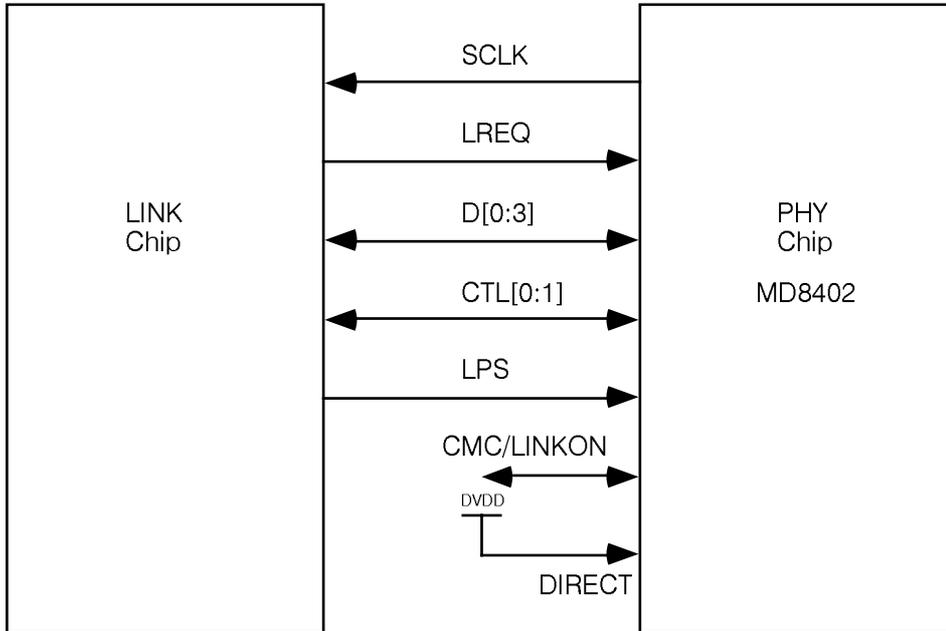


Figure 5-1 MD8402 - LINK Chip Connection Diagram (DC Connection)

##### 5-1-1-2 AC connection

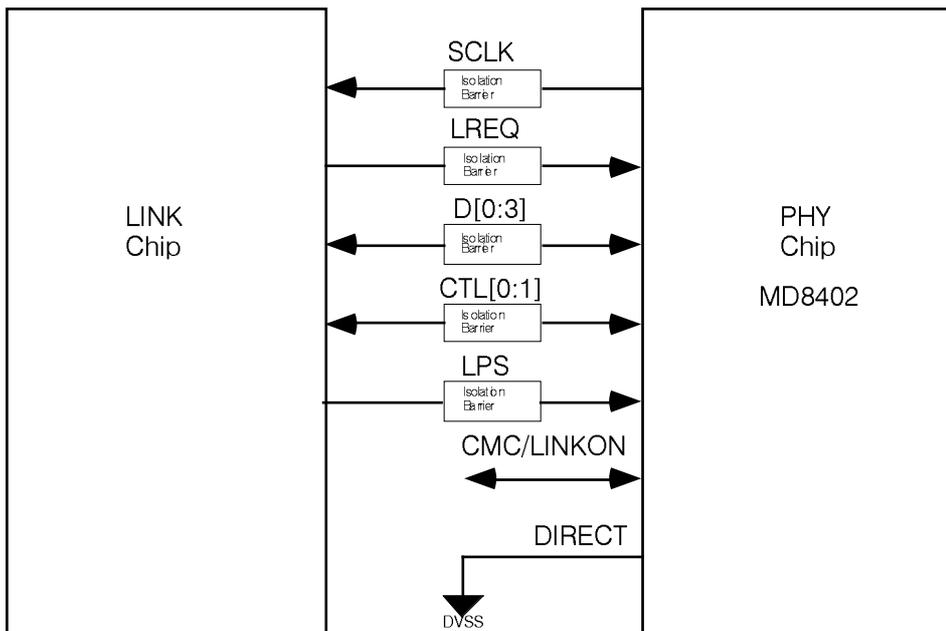


Figure 5-2 MD8402 - LINK Chip Connection Diagram (AC Connection)

5-1-1-3 Isolation Barrier

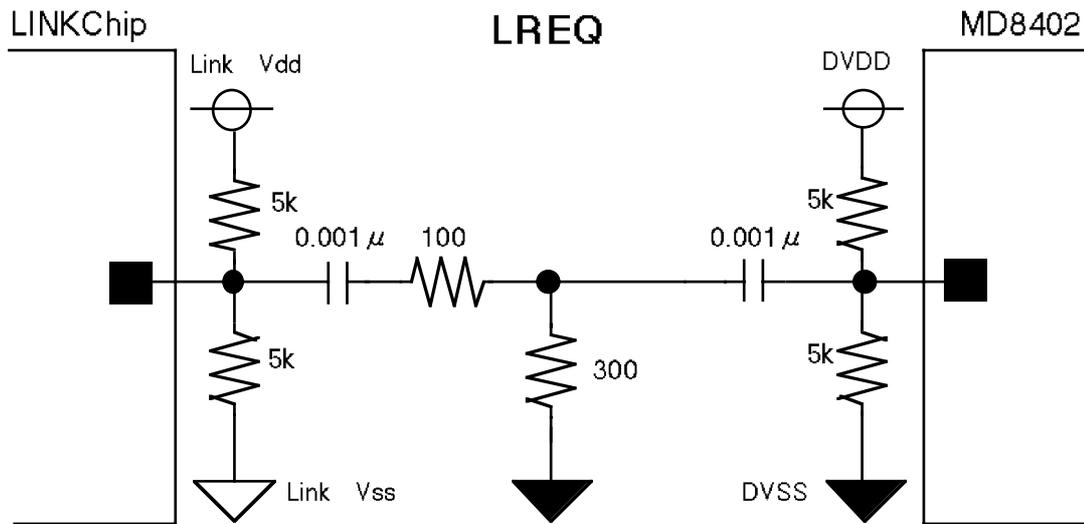


Figure 5-3 the Isolation Barrier circuit for LREQ

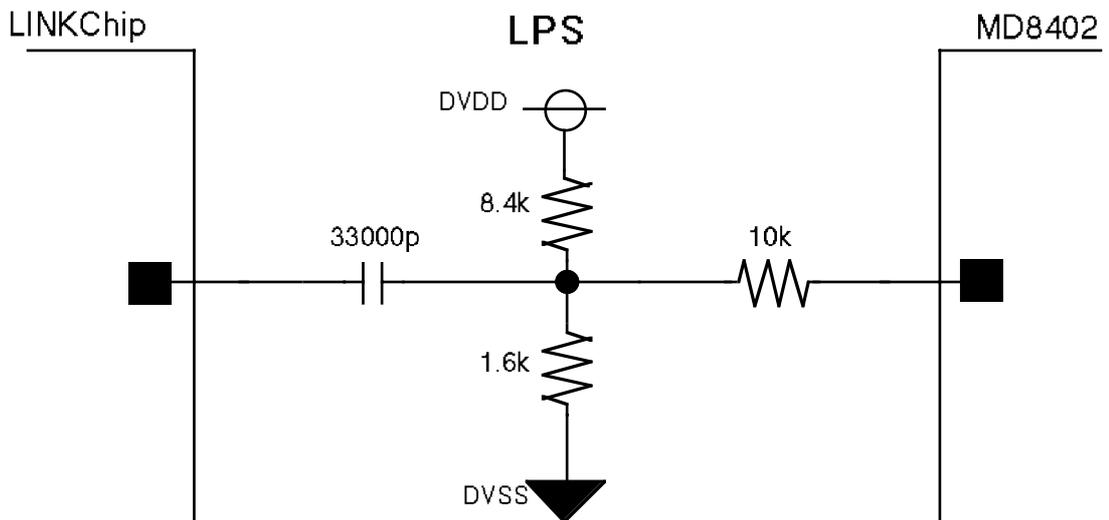


Figure 5-4 the Isolation Barrier circuit for LPS

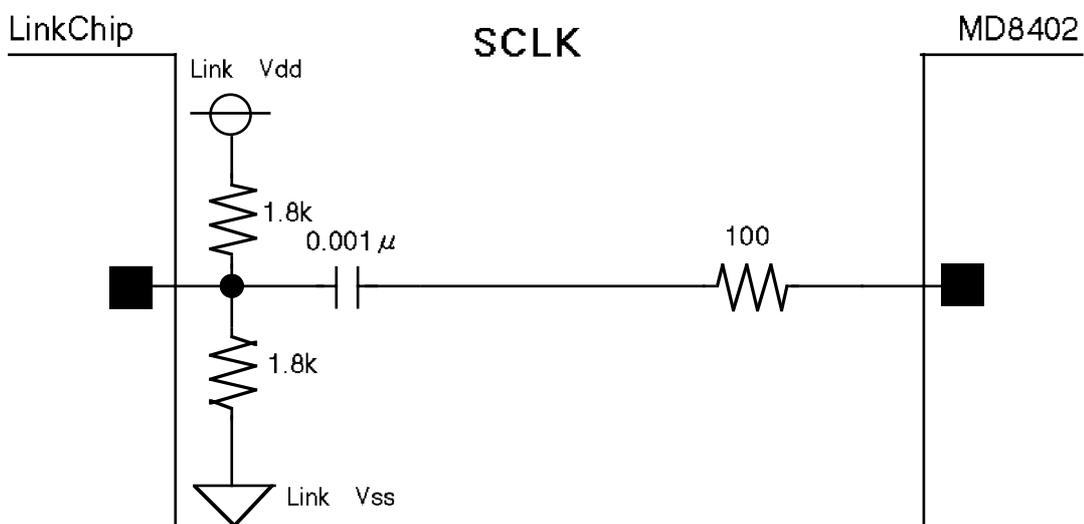


Figure 5-5 the Isolation Barrier circuit for SCLK

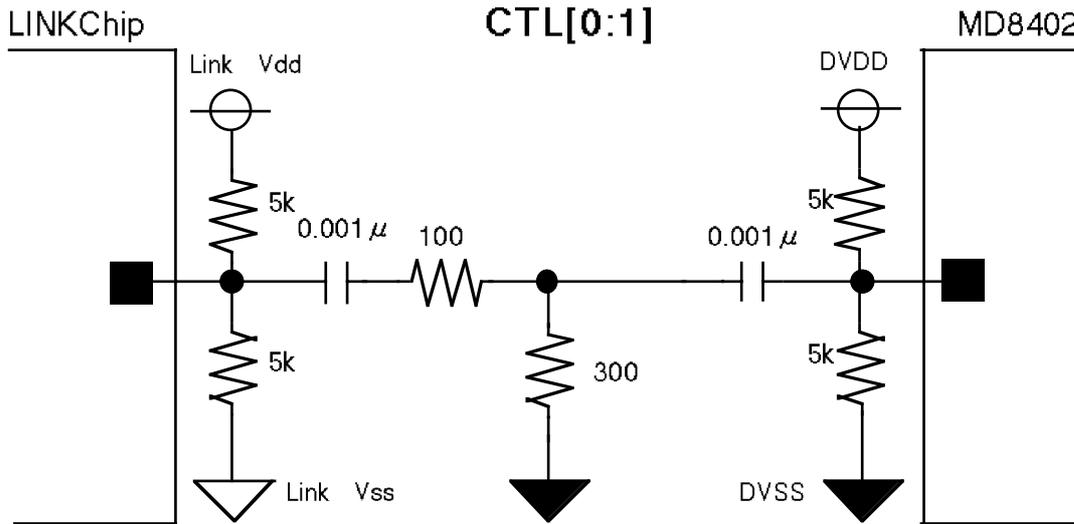


Figure 5-6 the Isolation Barrier circuit for CTL[0:1]

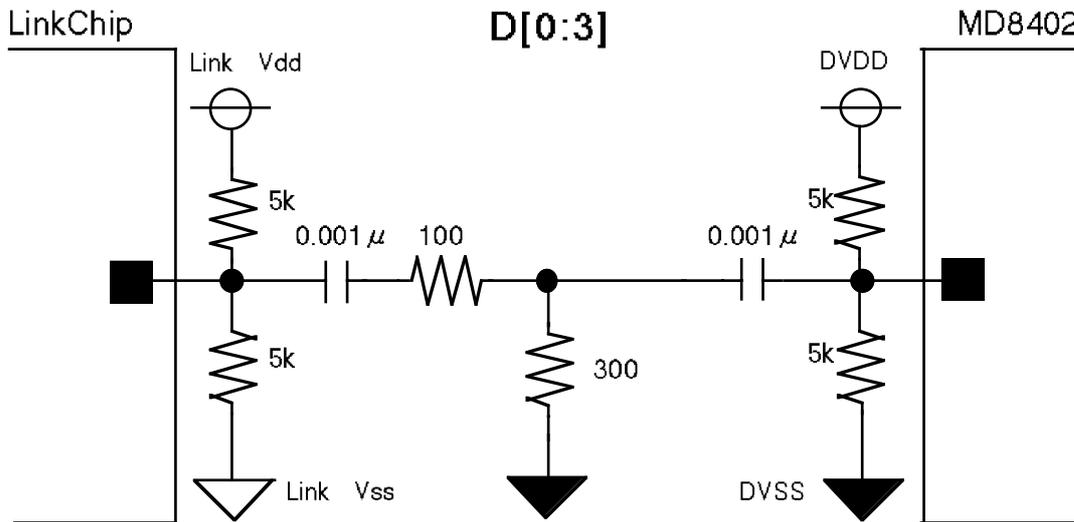


Figure 5-7 the Isolation Barrier circuit for D[0:3]

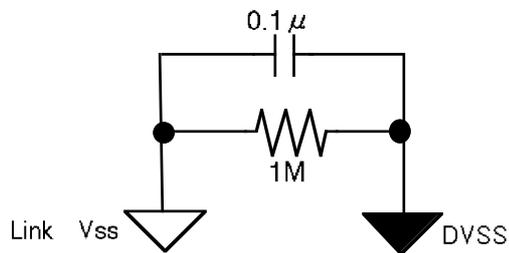


Figure 5-8 the circuit for VSS connection

#### 5-1-1-4 CMC/LINKON pin connection

The circuit for CMC = 1 is shown in Figure 5-9, the circuit for CMC = 0 shown is Figure 5-10.

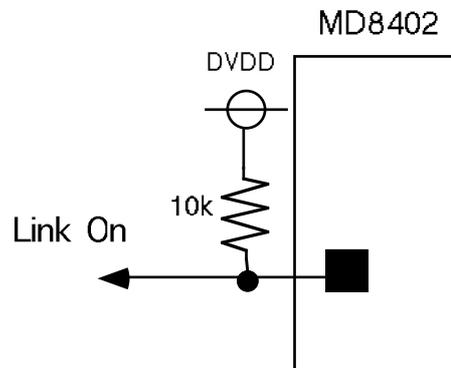


Figure 5-9 the circuit for the CMC/LINKON pin connection (CMC = 1)

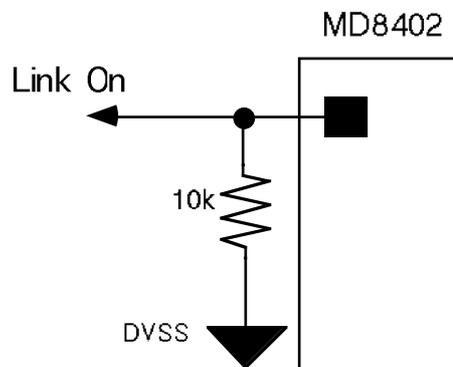


Figure 5-10 the circuit for the CMC/LINKON pin connection (CMC = 0)

### 5-1-2 LINK chip Control

CTL[0:1]	Operation	Contents
00b	Idle	Idle condition, with nothing in operation (default mode)
01b	Status	The PHY chip is sending status information
10b	Receive	An incoming packet is being transferred from the PHY chip to the Link chip
11b	Transmit	The LINK chip is granted the bus to send a packet

Table 5-1 PHY chip control mode1

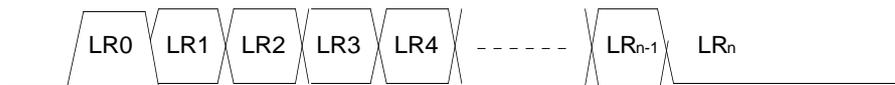
After the PHY-LINK bus control is enabled in the above - mentioned transmit mode, an operation mode is assumed as shown in Table 5-2.

CTL[0:1]	Operation	Contents
00b	Idle	PHY-LINK bus is released since LINK chip has completed data transfer
01b	Hold	<ul style="list-style-type: none"> <li>•The bus is held until data are fixed, since LINK chip is making data transfer</li> <li>•Link chip is calling for another packet transmission, without performing arbitration</li> </ul>
10b	Transmit	The Link chip is sending a packet to PHY chip
11b	Reserved	Reserved

Table 5-2 PHY chip control mode2

### 5-1-3 Request

As a request to gain access to a register of the PHY chip or the PHY-LINK bus, the Link chip sends out a short serial stream to the LREQ terminal. This stream contains the requested type, transferring packet speed, and reading or writing command.



LRn = LREQn

Figure 5-11 LREQ Stream

**5-1-3-1 LREQ**

The request for the PHY-LINK bus is effected with a 7-bit format indicated by LREQ shown in Table 5-3.

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. "1" is always transferred
1~3	Request Type	Indicates the request type shown in Table 5-7
4~5	Request Speed	Indicate the transfer speed of the request PHY chip
6	Stop Bit	Indicate the end of data transfer. "0" is always transferred.

Table 5-3 Request Format

LREQ[4:5]	Data Rate
00	100Mbps
01	200Mbps

Table 5-4 Speed Format

The request of register read-out for the PHY chip is effected with a 9-bit format indicated by LREQ shown in Table 5-5. The request of register write is effected with a 17-bit format indicated by LREQ shown in Table 5-6.

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. "1" is always transferred
1~3	Request Type	Indicates the request type shown in Table 5-7
4~7	Address	Indicates the register address of the reading PHY chip
8	Stop Bit	Indicate the end of data transfer. "0" is always transferred.

Table 5-5 Read Register Format

Bit(s)	Operation	Contents
0	Start Bit	Indicates the start of data transfer. "1" is always transferred
1~3	Request Type	Indicates the request type shown in Table 5-7
4~7	Address	Indicates the register address of the writing PHY chip
8~15	Data	Indicates the register data of the writing PHY chip
8	Stop Bit	Indicate the end of data transfer. "0" is always transferred.

Table 5-6 Write Register Format

LREQ[1:3]	Operation	Contents
000	ImmReq	Immediate request
001	IsoReq	Isochronous request
010	PriReq	Priority request
011	FairReq	Fair request
100	RdReq	Contents of the set register being read out
101	WrReq	Writing in the set register
110,111	Reserved	Reserved

Table 5-7 Request type

## 5-1-4 Transfer

### 5-1-4-1 Status

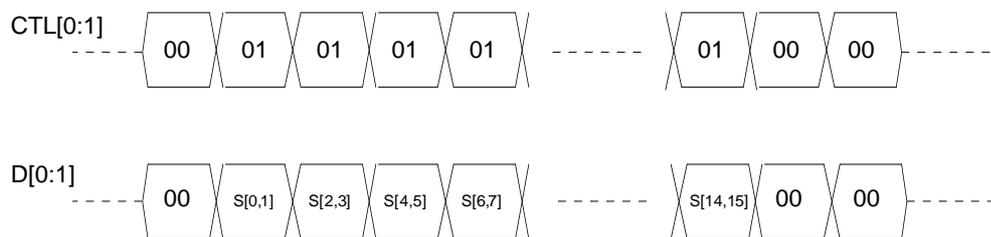


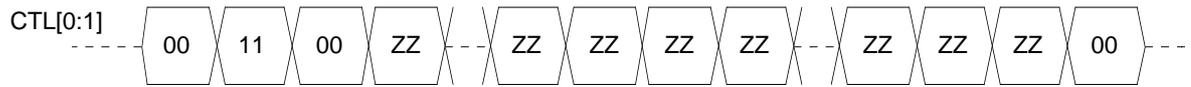
Figure 5-12 Status

Bit (Sn)	Operation	Contents
0	Arbitration Reset Gap	Arbitration Reset Gap is detected
1	Fair Gap	Fair Gap is detected
2	Bus Request	Bus Reset is detected
3	Phy Interrupt	Interrupt to the host is requested
4~7	Address	PHY register address returning the status
8~15	Data	Status data

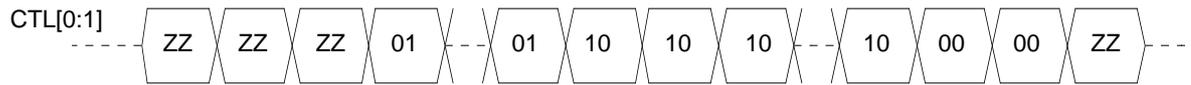
Table 5-8 Status Format

5-1-4-2 Transmit

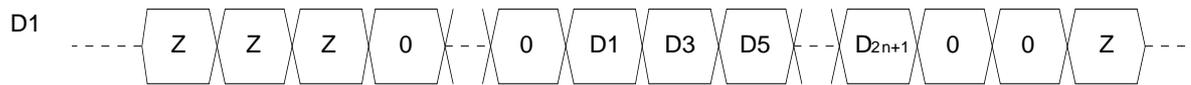
PHY Drive



LINK Drive



100Mbps



200Mbps

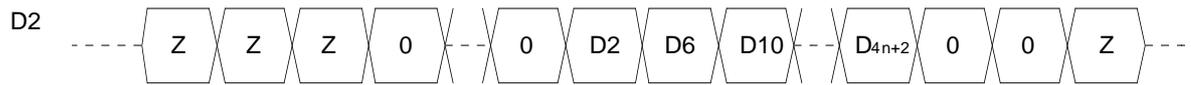
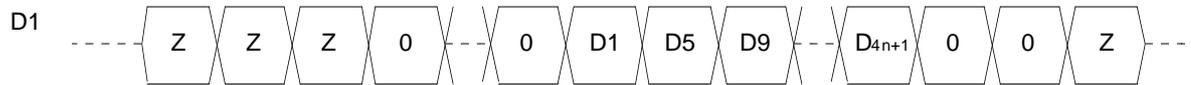
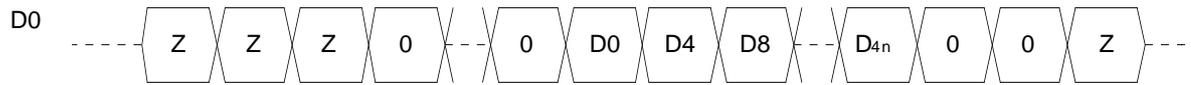
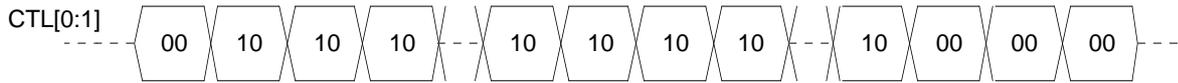


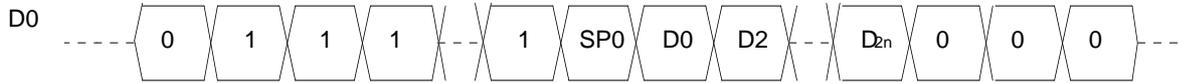
Figure 5-13 Transmit

5-1-4-3 Receive

PHY Drive



100Mbps



200Mbps



Figure 5-14 Receive

SP[0:3]	Data Rate
00XX	100Mbps
0100	200Mbps

Table 5-9 Speed Code (SP[0:3])

## 6 Electric Characteristics

### 6-1 Absolute Maximum Ratings

(VSS = 0V)

Symbol	Item	Rating	Unit
VDD	Supply voltage	-0.5 ~ 5.0	V
VIN	Input voltage	-0.5 ~ VDD+0.5	V
VOUT	Output voltage	-0.5 ~ VDD+0.5	V
TSTG	Storage temp.	-65 ~ 150	°C

Table 6-1 Absolute Maximum Rating

### 6-2 Recommended Operating Conditions

Symbol	Item	Rating	Unit
VDD	Power voltage	3.0 ~ 3.6	V
VIN	Input voltage	0 ~ VDD	V
VOUT	Output voltage	0 ~ VDD	V
TA	Ambient temp.	0 ~ 70	°C

Table 6-2 Recommended Operating Condition

### 6-3 DC Characteristics

DC characteristics under the recommended conditions except special mention.

Link Interface

(VSS = 0V)							
Symbol	Item	Terminal	Test condition	MIN	TYP	MAX	Unit
VIH	Input high voltage	LREQ、CTL[0:1]、 D[0:3]		VDD-0.7			V
		LPS、TEST[0:1]、 DIRECT、PC[0:2]、 CMC/LINKON		VDD-1.0			
VIL	Input low voltage	LREQ、CTL[0:1]、 D[0:3]				0.7	V
		LPS、TEST[0:1]、 DIRECT、PC[0:2]、 CMC/LINKON				1.0	
IIH	Input high current	LREQ、CTL、 D[0:3]	VIH=VDD	-10			$\mu$ A
		LPS、TEST[0:1]、 DIRECT、PC[0:2]、 CMC/LINKON	VIH=VDD	-10			
IIL	Input low current	LREQ、CTL、 D[0:3]	VIL=VSS			10.0	$\mu$ A
		LPS、TEST[0:1]、 DIRECT、PC[0:2]、 CMC/LINKON	VIL=VSS			10.0	
VOH	Output high voltage	SCLK、CTL[0:1]、 D[0:3]	IOH = - 12mA	VDD - 0.5			V
		CMC/LINKON	IOH = - 8mA	VDD - 0.5			
VOL	Output low voltage	SCLK、CTL[0:1]、 D[0:3]	IOL = + 12mA			0.5	V
		CMC/LINKON	IOL = + 8mA			0.5	
IDD	Dynamic power supply current		VDD = 3.3 V		128.0		mA

Table 6-3 DC Characteristics (Link Interface)

## Cable Interface

Symbol	Item	Test condition	MIN	TYP	MAX	Unit
VOD	Differential output amplitude	55Ω differential load	175		265	mV
VTPBIAS	Tpbias output voltage	Source 3[mA] Sink 1.3[mA]	1.89		2.11	V
ICM	Tp Common Mode current	Driver Disabled (Z state)	-25		5	μA
		Driver enabled but no speed signal	-0.18		0.18	mA
ISPD	TPB200Mbit Speed signal		2.76		4.6	mA
ZDIFFZ	Differential input impedance	Driver disabled (Z state)	21.0		7.6	kΩ pF
ZDIFFEN	Differential input impedance	Driver Enabled	3.4		7.6	kΩ pF
CCM	Common mode input Cap.	Measured with Tp pins shorted and driver in the Z state			29	pF
VT NOCONN	Cable Not Active Threshold	Common mode voltage on TpB	0.64		0.96	V
VT CPWD	CPS voltage threshold	Vp pin (R=226kΩ)	6.0		10.0	V

Table 6-4 DC Characteristics (Cable Interface)

## 6-4 AC Characteristics

### Link Interface

Symbol	Item	DC connection			AC connection			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
TSU	D, CTL, LREQ, Setup time	5			1			ns
TH	D, CTL, LREQ, Hold time	1			5			ns
TD	D, CTL, Output Timing time	0		7	0		7	ns
TSCLK	SCLK Cycle time	20			20			ns
TSCLKH	SCLK High Level time	8		12	8		12	ns
TSCLKL	SCLK Low Level time	8		12	8		12	ns

Table 6-5 AC Characteristics (Link Interface)

### Twisted Pair Interface

Symbol	Item	Test condition	MIN	MAX	Unit
TTJITTER	Transmit Jitter on TPA, TPB			+/-0.25	ns
TTSKEW	Misalignment between transmit Strobe on TPA and Data on TPB			+/-0.15	ns
TTRF	Transmit rise and fall times on TPA and TPB	10% to 90% into 55 $\Omega$ , 10pF		2.2	ns

Table 6-6 AC Characteristics (Twisted Pair Interface)

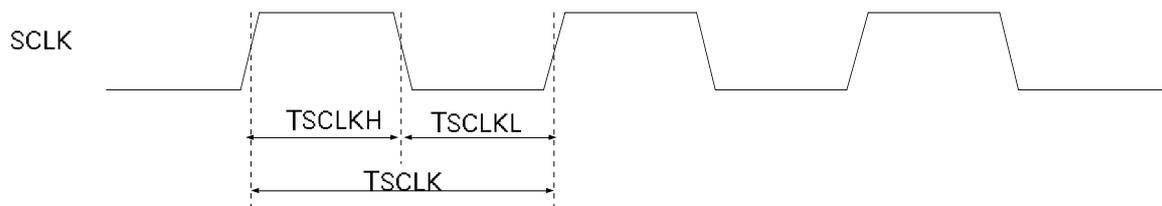


Figure 6-1 Link Interface AC Characteristics (SCLK)

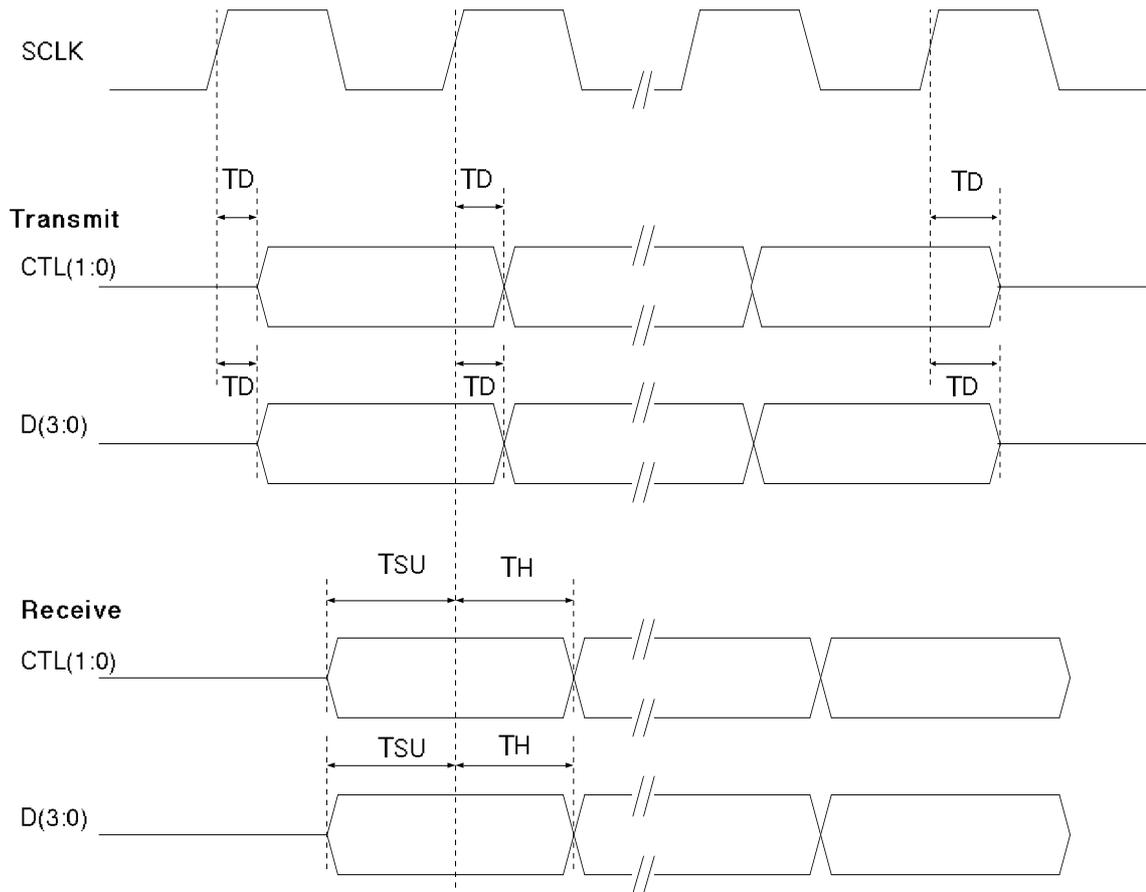


Figure 6-2 Link Interface AC Characteristics (CTL, D)

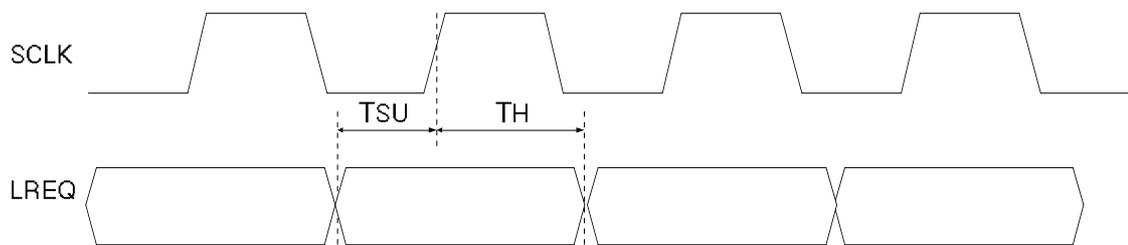


Figure 6-3 Link Interface AC Characteristics (LREQ)



7-2 External Dimensions

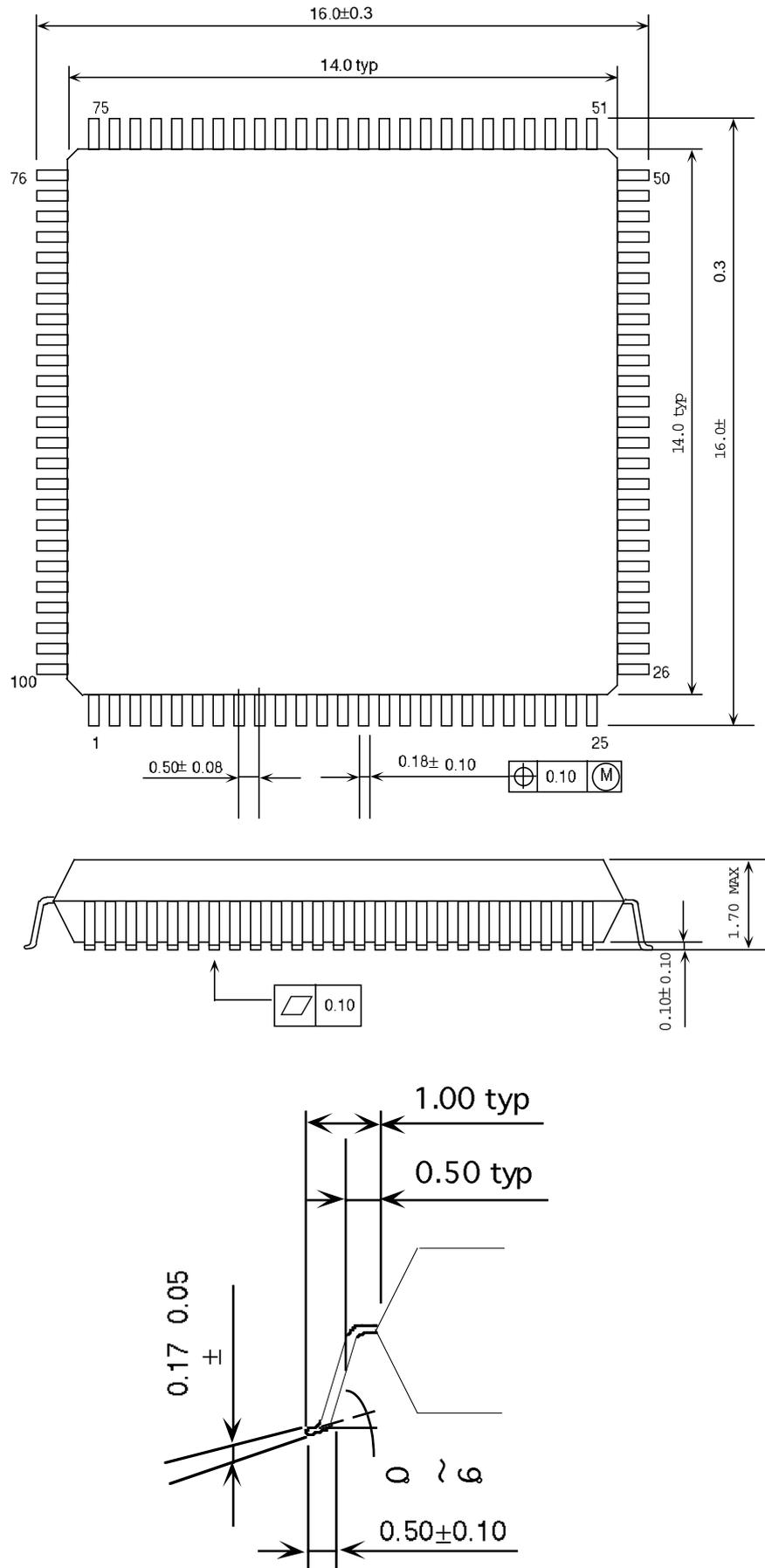


Figure 7-2 External Dimensions



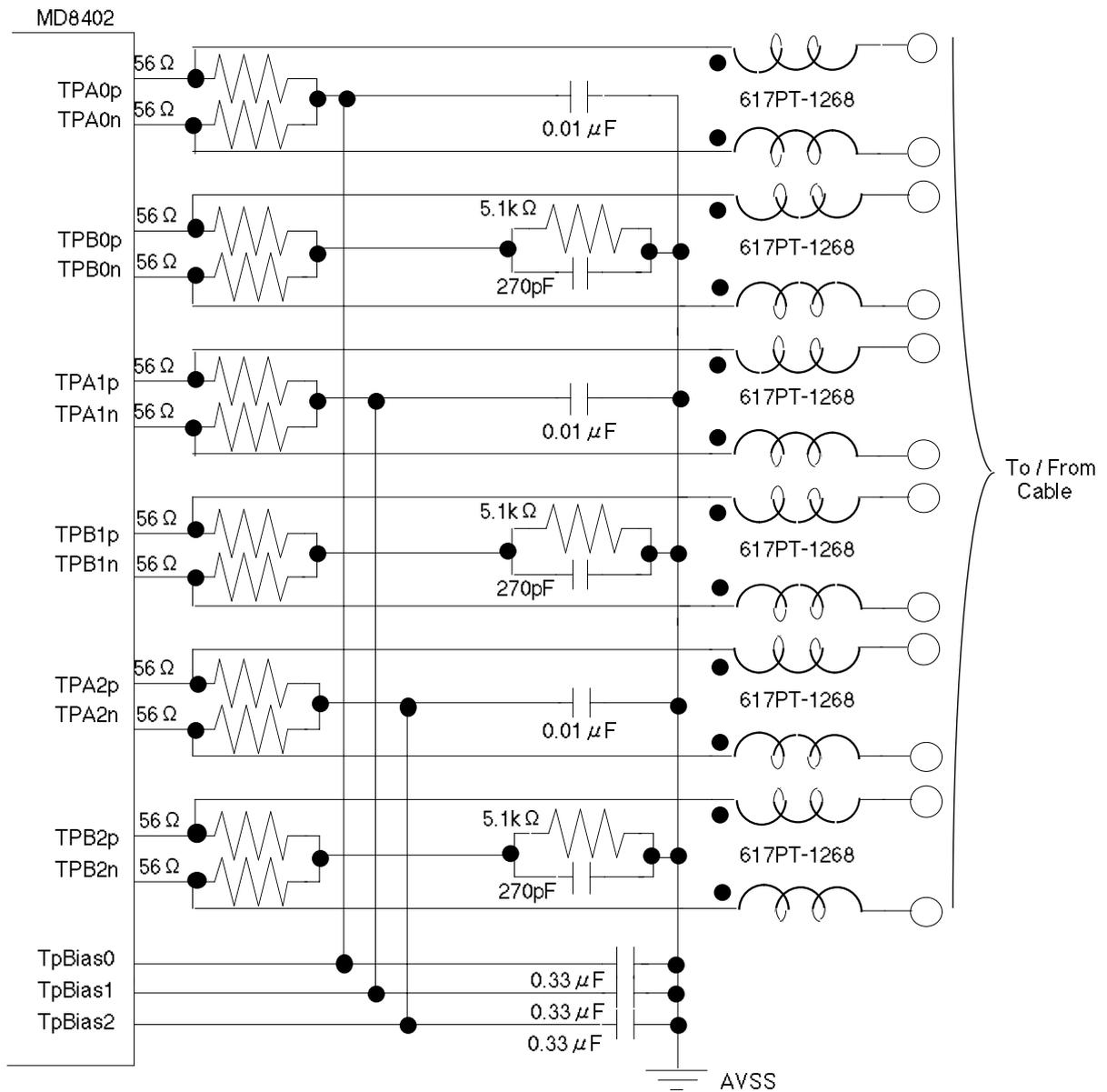


Figure 8-2 Cable Interface connection recommended circuit

- The Cable Interface possibly reduce the existed inductance.

## 9 MD8402 unused ports

### 9-1 management of the unused ports

The MD8402 has three ports, however, in the case of using only two ports or one port, the unused ports should be connected as shown table 9-1.

Terminal of the unused ports	connect
TPAp, TPA <sub>n</sub>	No Connect
TPBp, TPB <sub>n</sub>	AVSS
TpBias	AVSS via 0.33 μF

Table 9-1 management of the unused ports

An as example, shown the circuit in the case of using only one port.

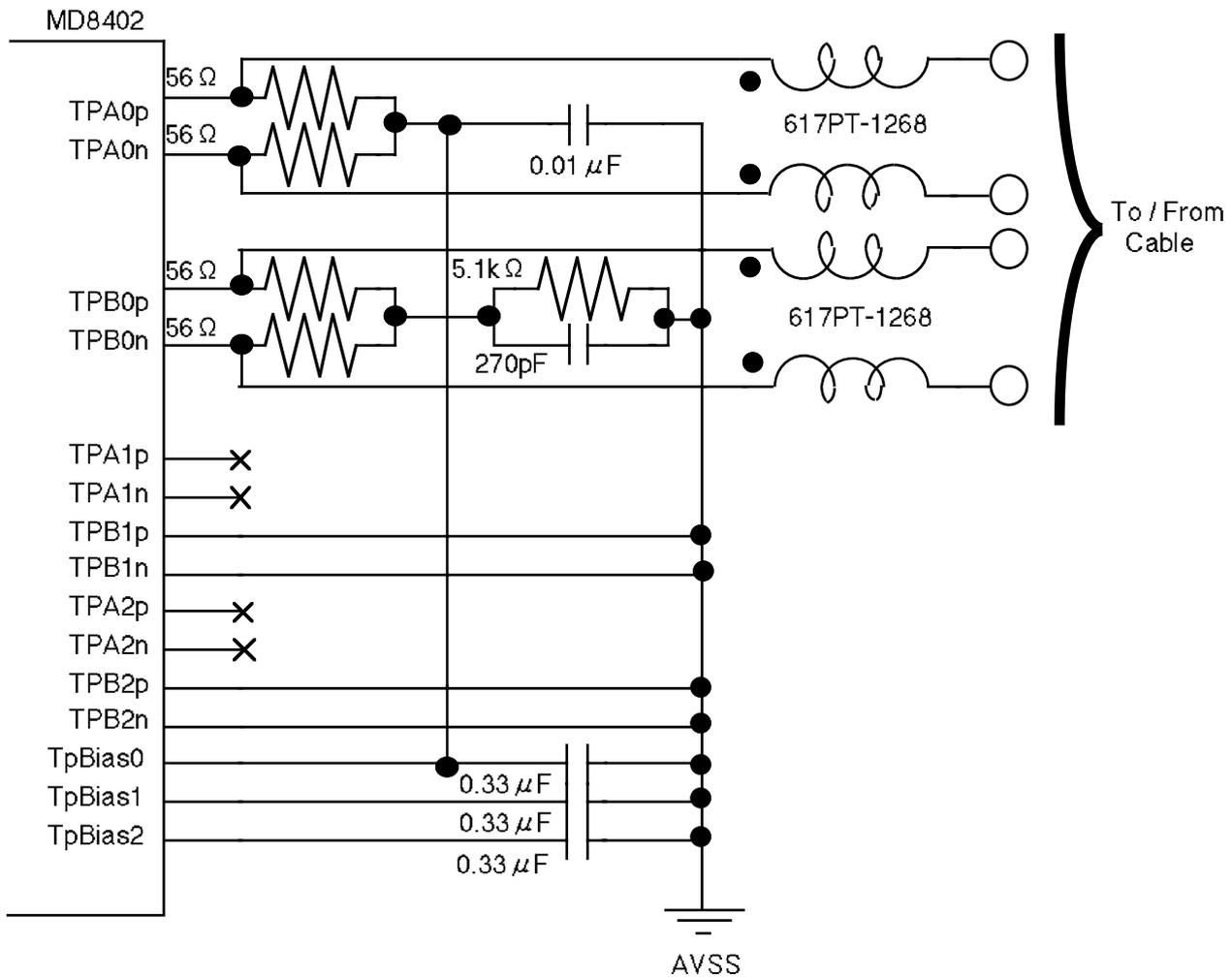


Figure 9-1 the circuit in the case of using only one port

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