DSP Selection Guide
2002 Edition

- Introduction to ADI DSPs
- Processor Selection Guides
- DSP Development Tools
- Support Resources
- Benchmarks
- Training Workshops

www.analog.com/dsp

ANALOG DEVICES

DSP SOLUTIONS THAT MAKE YOUR DESIGN CHALLANGE EASIER

Contents

16-Bit DSP Key Products
Recommended for New Designs

Blackfin™ DSP	Package	Max MMACs	Vcc	Program and Data Memory Words	Status	Price*
ADSP-21535P	B	600	1.5V	154K	Samples Now Release July 2002	$32.00
ADSP-21532S	CA	600	2.25-3.6V**	58K***	Samples Summer 2002 Release 1Q03	$11.50

ADSP-21xx DSP	Package	Max MMACs	Vcc	Program Memory Words	Data Memory Words	Status	Price*
ADSP-2191M	ST,CA	160	2.5V	32K	32K	Released	$16.85
ADSP-2195M	ST,CA	160	2.5V	32K***	16K	Released	$13.90
ADSP-2196M	ST,CA	160	2.5V	24K***	8K	Released	$11.10
ADSP-2188N	ST,CA	80	1.8V	48K	56K	Released	$26.00
ADSP-2189N	ST,CA	80	1.8V	32K	48K	Released	$21.00
ADSP-2187N	ST,CA	80	1.8V	32K	32K	Released	$17.00
ADSP-2185N	ST,CA	80	1.8V	16K	16K	Released	$9.50
ADSP-2186N	ST,CA	80	1.8V	8K	8K	Released	$7.25
ADSP-2184N	ST,CA	80	1.8V	4K	4K	Released	$5.75
ADSP-2188M	ST,CA	75	2.5V	48K	56K	Released	$28.00
ADSP-2189M	ST,CA	75	2.5V	32K	48K	Released	$23.00
ADSP-2185M	ST,CA	75	2.5V	16K	16K	Released	$10.00
ADSP-2186M	ST,CA	75	2.5V	8K	8K	Released	$7.50

Packages: ST = Thin Quad Flat Pack (LQFP) B = Plastic Ball Grid Array
CA = Mini Ball Grid Array

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change

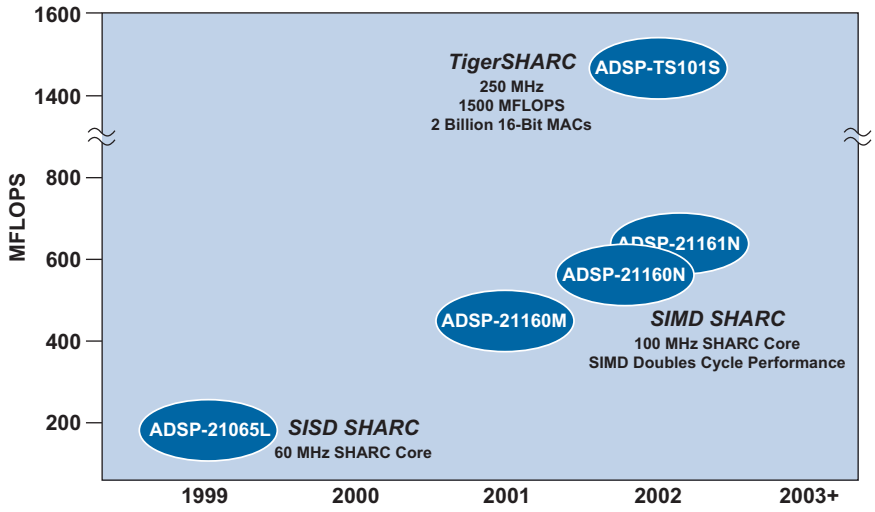
** External voltage range – core voltage regulation on-chip

*** Includes 16K words ROM

Development Tools	ADSP-218x M/N	ADSP-219x	Blackfin DSP
Evaluation Development Platform	ADDS-2189M-EZLITE $295	ADDS-2191-EZLITE $295	ADDS-21535-EZLITE $295
Emulator	ADDS-218X-ICE-2.5V $1995	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	
VisualDSP++ Development Software	VDSP-21XX-PC-FULL $3500 VDSP-21XX-PCFLOAT $4250		VDSP-BLKFN-PC-FULL $3500 VDSP-BLKFN-PCFLOAT $4250

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++. Please contact your local ADI sales representative or distributor for more information.

SHARC® and TigerSHARC® DSP Key Products
Recommended for New Designs



32-Bit Generic	Package	Max MFLOPS	Vcc	On-Chip SRAM	Status	Price*
ADSP-21161N	CA	600	1.8/3.3V	1 Mbits	Samples Now Release 2Q02	$24.63
ADSP-21160M	B	480	2.5/3.3V	4 Mbits	Released	$145.00
ADSP-21160N	B	570	1.9/3.3V	4 Mbits	Samples Now Release 3Q02	$145.00
ADSP-21065L	S, CA	198	3.3V	544 Kbits	Released	$19.50
ADSP-TS101S	B	1500	1.2/3.3V	6 Mbits	Samples Now Release 4Q02	$207.00

Packages: B = Plastic Ball Grid Array (PBGA)
S = Plastic Quad Flat Pack (PQFP)
CA = Mini Ball Grid Array

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change

Processor	Evaluation Development Platform	Emulator	Development Software
ADSP-21161N	ADDS-21161N-EZLITE $495	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	VDSP-SHARC-PC-FULL $3500 VDSP-SHARC-PCFLOAT $4250
ADSP-21160M	ADDS-21160-EZLITE $595 (Available 2Q02)	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	VDSP-SHARC-PC-FULL $3500 VDSP-SHARC-PCFLOAT $4250
ADSP-21160N	ADDS-21160N-EZLITE $650 (Available 3Q02)	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	VDSP-SHARC-PC-FULL $3500 VDSP-SHARC-PCFLOAT $4250
ADSP-21065L	ADDS-21065L-EZLITE $299	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	VDSP-SHARC-PC-FULL $3500 VDSP-SHARC-PCFLOAT $4250
ADSP-TS101S	ADDS-TS101S-EZLITE $995	ADDS-APEX-ICE $4995 ADDS-SUMMIT-ICE $4995	VDSP-TS-PC-FULL $3500 VDSP-TS-PCFLOAT $4250

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++.
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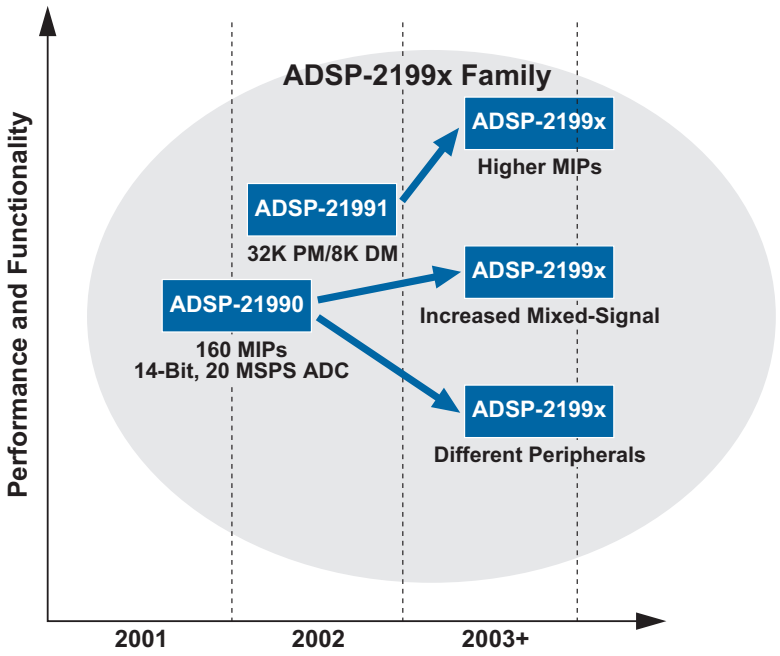
Mixed Signal DSP Key Products
Recommended for New Designs



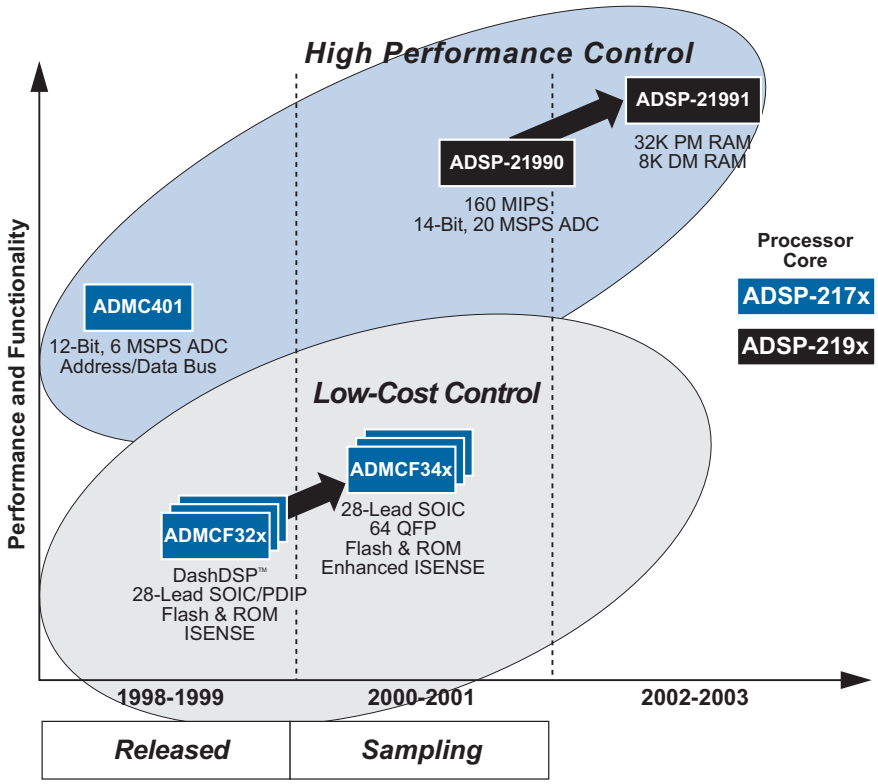
Device	Package	Max MIPS	Program RAM Words	Data RAM Words	ADC	Status
ADSP-21990	ST, BC	160	4K	4K	14-Bit 20 MSPS	Samples Now Release 2Q02
ADSP-21991	ST, BC	160	32K	8K	14-Bit 20 MSPS	Samples 3Q02 Release 4Q02

Packages: ST = Thin Quad Flat Pack (LQFP)
BC = Mini Ball Grid Array (10 x 10 mm)

Processor	Evaluation Development Platform		Emulator		Development Software	
ADSP-2199X	ADDS-21990-EZLITE	$495	ADDS-APEX-ICE	$4995	VDSP-21XX-PC-FULL	$3500
			ADDS-SUMMIT-ICE	$4995	VDSP-21XX-PCFLOAT	$4250

Note: DSP tools pricing is US dollars and subject to change at anytime. Volume discounts are available for VisualDSP++. Please contact your local ADI sales representative or distributor for more information.

Embedded DSP-Based Control Key Products
Recommended for New Designs



Device	Package	Max MIPs	Program RAM	Program FLASH	Program ROM	Data RAM	ADC	Price*
ADMC401	144-LQFP	26	2K		2K	1K	8 Channel, 12-Bit	$19.95
ADMC32x	28-SOIC	20	0.5K		4K	0.5K	Varies	**CF
ADMCF32x	28-SOIC	20	0.5K	4K		0.5K	Varies	$11.65
ADMC341/F341	28-SOIC	20	0.5K	4K (F341)	4K (341)	0.5K	6 Channel, 10-Bit	**CF
ADMC340/F340	64-TQFP	20	0.5K	4K (F340)	4K (340)	0.5K	13 Channel, 10-Bit	**CF

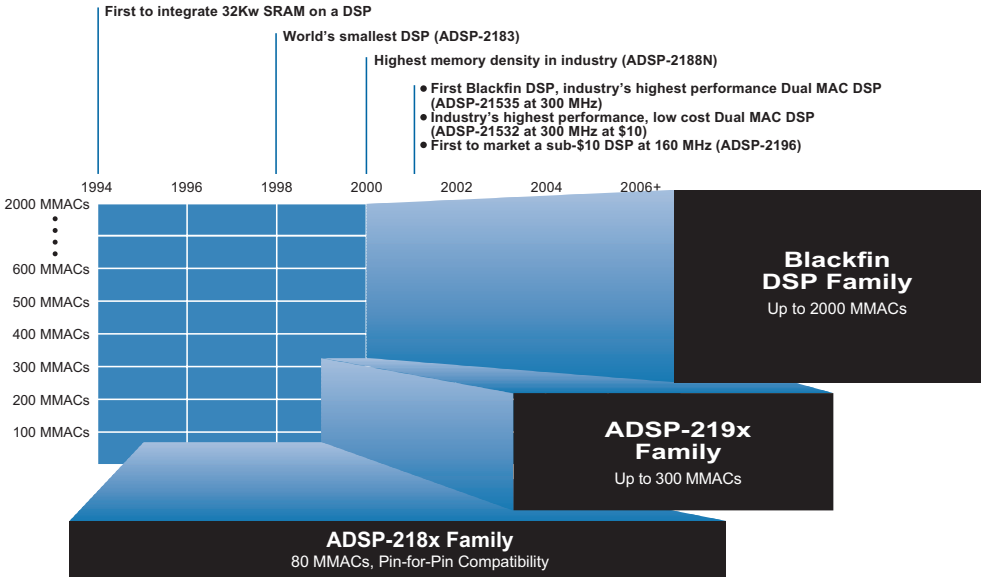
* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary – subject to change
** CF = Contact factory for pricing

Device	Evaluation Development Platform	Price
ADMC401	ADMC401-ADVEVALKIT	$395
ADMC32x/F32x	ADMCF326-EVALKIT ADMCF327-EVALKIT ADMCF328-EVALKIT	$395
ADMC341/F341	ADMCF341-EVALKIT	$395
ADMC340/F340	ADMCF340-EVALKIT	$395

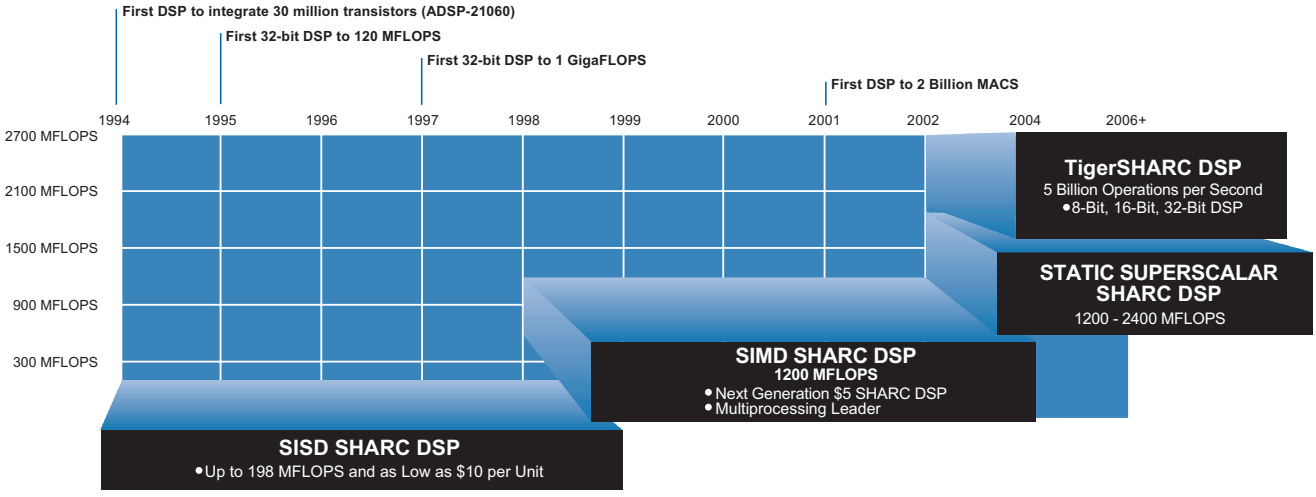
ADI DSP Overview
Architectural Roadmaps

Analog Devices is the world's fastest-growing DSP supplier. Our portfolio includes mixed-signal DSPs, general-purpose DSPs, such as the SHARC®, TigerSHARC®, Blackfin™, and ADSP-21xx DSP families, and embedded DSP solutions that serve secure data, ADSL modems, GSM handsets, internet access, speech processing and motor control applications. ADI leverages 30 years of high performance analog expertise to develop DSPs that make the design challenge easier. ADI's DSP architectures feature simple, yet powerful programming models and are supported by high-quality development tools. More than 30,000 software developers have invested in our 16-bit and 32-bit fixed-point and floating-point DSP architectures.

Analog Devices 16-Bit DSP Roadmap



Analog Devices SHARC DSP Roadmap



DSP Markets and Applications

As the processing capabilities of DSPs increase, they are used in more and more applications.

Audio Signal Processing

DSP Function	Application
• Reverb • Tone Control • Echo • Filtering • Audio Compression • Frequency Equalization • Pitch Shifting • Spatial Effects • Surround Sound	• Musical Instruments & Amplifiers • Audio Mixing Consoles • Recording Equipment • Disc Jockey Mixing Consoles • Broadcast Equipment • Cable TV Equipment • Audio Equipment & Boards for PCs • Toys & Games • Automotive Sound Systems • Digital Audio Tape Players • Compact Disk Players • HDTV Equipment • Digital TV • DVD Players • Home Theater AVR Systems

Recommended DSPs

- ADSP-21065L
- ADSP-2116x
- ADSP-21532
- ADSP-TS101S
- ADSST-MEL-30
- ADSST-AUDIO-7085

Speech Processing

DSP Function	Application
• Speech Synthesis • Speech Recognition • Speech Compression • Text to Speech • Pitch Shifting • Filtering • Speech Record & Playback	• Digital Tapeless Recorders • Voice Store Equipment • Phone Mail • Voice Secure Entry Systems • Intercom Systems • Personal ID Systems • Audio Equipment & Boards for PCs • Toys & Games

Recommended DSPs

- ADSP-218xM/N
- ADSP-21065L
- ADSP-21161N
- ADSP-219x
- ADSP-2153x
- ADSP-TS101S

Communications

DSP Function	Application
• Modulation & Transmission • Demodulation & Reception • Speech Compression • T1 Switching • DTMF • Data Encryption • Signal Recovery • Echo Cancellation • Voice Over Data • Voice Over IP	• Modems • Fax Machines • PBX Systems • Phone Mail Systems • Private Data Communications Systems • Automatic Teller Machines • Broadcast Equipment • Mobile Phones • Digital Pagers • Global Positioning Systems • Secure, Speaker, & Video Telephones • Digital Answering Machines • Satellite Phones • Wireless Local Loop • Telecom Infrastructure

Recommended DSPs

- ADSP-218xM/N
- ADSP-21065L
- ADSP-219x
- ADSP-2153x
- ADSP-TS101S
- ADSST-NAV2400

Multimedia

DSP Function	Application
• Audio Encoding • Audio Compression • Video Encoding • Video Compression • Image Encoding • Image Compression	• Digital Imaging • Digital Printing • Internet Appliance • Broadband • PDA • Video Conferencing

Recommended DSPs

- ADSP-2153x
- ADSP-TS101S

Instrumentation and Measurement

DSP Function	Application
• Fast Fourier Transform (FFT) • Filtering • Waveform Synthesis • Adaptive Filtering • High Speed Numeric Calculations	• Test & Measurement Equipment • Vibration Analysis Equipment • I/O Cards for PCs • Automotive Engine Analyzers • Automotive Wheel Balancers • Industrial Scales & Measurement • Active Mufflers • Oil Drilling Equipment • Seismic Instruments • Power Meters • Exercise Machines • Signal Analyzers • Function/Signal Generators

Recommended DSPs

- ADSP-218xM/N
- ADSP-21065L
- ADSP-21161N
- ADSP-219x
- ADSP-2153x
- ADSP-TS101S
- ADSP-2199x

Medical Electronics

DSP Function	Application
• Filtering • Echo Cancellation • Fast Fourier Transform (FFT) • Beam Forming	• Respiration Monitoring Equipment • Heart Rate/Cardiac Monitoring • Ultra Sound Equipment • Medical Imaging Equipment • Blood Analyzers • Fetal/Infant Monitors • Patient Monitors • Blood Flow Monitors • CAT Scanners • Hearing Aids

Recommended DSPs

- ADSP-218xM/N
- ADSP-2116x
- ADSP-2106x
- ADSP-219x
- ADSP-2153x
- ADSP-TS101S

Optical and Image Processing

DSP Function	Application
• 2-Dimensional Filtering • Fast Fourier Transform (FFT) • Pattern Recognition • Image Smoothing	• Bar Code Scanners • Underwater Object Finders • Automatic Inspection Systems • Fingerprint Recognition • Digital Televisions • Sonar/Radar Systems • Robotic Vision • Vision Systems

Recommended DSPs

- ADSP-2106x
- ADSP-2116x
- ADSP-219x
- ADSP-2199x
- ADSP-2153x
- ADSP-TS101S

Industrial/Motor Control

DSP Function	Application
• Filtering • Fast Fourier Transform (FFT) • Control Loops • Noise Cancellation • Flash Memory	• Motors in Appliances, Robotics or Office Automation • Power Management Equipment • Generators • Elevators • Air Conditioners • Traffic Control Systems • Navigation • Disk Drives • Vibration Analyzers • High Speed Controls • Uninterruptible Power Suppies • Switched Mode Power Supplies

Recommended DSPs

- ADSP-2106x
- ADSP-2116x
- ADMCxxx
- ADSP-2199x
- ADSP-218xM/N
- ADSP-219x
- ADSP-2153x

ADI DSP Key Benefits

Selecting a DSP processor can be a difficult task. Design engineers are concerned with time-to-market, for which ease of use, quality development tools, extensive application engineering support, and the availability of algorithm code are critical. Of course, designers are also concerned with low production cost, low power consumption, system integration, and other criteria such as clock frequency, size of on-chip memory, and high-level language support. To understand the benefits of ADI's families of 16- and 32-bit DSPs and how ADI's architectures are optimized for digital signal processing, keep in mind three basic features of DSP. DSPs must have the ability to:

1) Perform fast arithmetic
2) Fetch data at a fast rate
3) Sequence efficiently through repetitive operations

Key Feature	Benefit
Single Cycle Instruction Execution	• One cycle per instruction execution • ADSP-218x requires no extra latency cycles for decision branches, condition code checking, or subroutine calls • Delayed branches increase efficiency on pipelined architectures such as the SHARC® and ADSP-219x DSP families • Deterministic operations make it easy to develop, profile, and benchmark code • Blackfin™ DSP allows for 1 instruction and 2 data fetches per cycle
Code Compatible Family Members	• All ADSP-21xx Family members share the same base architecture and assembly language • All SHARC DSP Family members share the same base architecture and assembly language • No need to learn or invest in new development tools when moving from one family member to another • Software investment is preserved • Blackfin DSPs utilize an interlocked pipeline so future core versions will protect SW code investment
Simple Programming Language	• Algebraic syntax assembly language makes code easy to use, easy to learn, and easy to read • Unlike competitors who use mnemonics like SPAC and XORX, ADI assembly language syntax makes programming in highly-efficient assembly language easy
Balanced Core, Memory and I/O Integration	• Fast core processing, large on-chip memories, and high bandwidth I/O simplify real-time system development • Up to 14 channels of non-intrusive Direct Memory Access (DMA) allow data movement without interrupting math processing • Blackfin DSPs offer dual-ported L1 memory so the core can be fed while simultaneously loading in new data non-intrusively
Large On-Chip Memory	• Provides ample on-chip storage for most common DSP tasks such as digital filtering and FFTs, eliminating the need for off-chip memory
Efficient Program Sequencing and Zero-Overhead Looping	• Minimizes off-chip memory access wait states • On-chip hardware manages looping and provides the most efficient code execution with no extra programming for repetitive DSP code • No need to control looping with complex software
Pin-for-Pin Compatible Family Members	• Increase speed or memory integration within a common pin-out • Adds flexibility without requiring board redesign

ADI DSP Customer Support

Web

You can visit Analog Devices' **World Wide Web** home page. Browse through a wide assortment of information about the company and products. You can also get detailed technical information as well as cross reference information. A search engine and site map will help you find what you are looking for. You can reach Analog Devices over the internet at **www.analog.com/dsp**. Here you'll find:

- Applications and Solutions
- Development Tools
- Data Sheets & Manuals
- DSP Collaborative
- Technical Support
- University Program
- Training and Education

Faxback System

You can get 24 hour access to data sheets for Analog Devices products by using the Analog Devices FAXback automated literature delivery system. Simply call **1-800-446-6212** and follow the recorded instructions. By providing a FAX code and your FAX number, you can receive a copy of a data sheet in a matter of minutes. An index of products and FAX codes can be faxed to you upon demand. (available for USA and Canada only).

DSP Customer Support

Literature

North America:
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Fax: +852 2506 4755

VisualDSP++™
Integrated Development Environment

Features

Integrated Development and Debugger Environment

- Develop within a single interface (IDE/debugger)
- Profile and trace instruction execution of C/C++ and assembly programs (simulator only)
- Set watchpoints (conditional breakpoints) on processor registers and stacks, as well as program and data memory including:
  - Statistical profiling
  - MP (multiprocessing)
  - Graphical plotting
- Define all project and tool configurations through property page dialog boxes
- Set project-wide or individual file settings for debug or release mode project builds
- Create source files using an integrated, full-featured editor with syntax highlighting, OLE drag and drop, and bookmarks

VisualDSP++ Kernel (VDK)

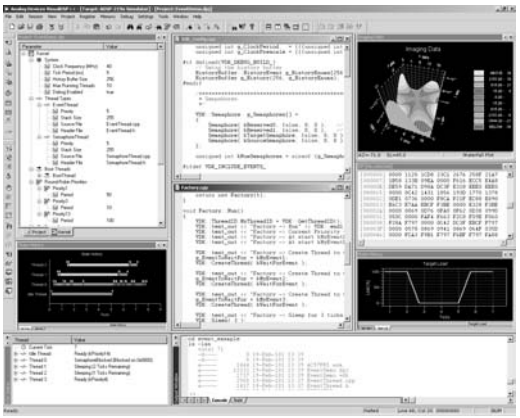
- Scheduling and resource management
- Supports threads, events, semaphores, critical and unscheduled regions

Code Generation Key Features

- Develop applications using an optimizing C/C++ compiler
- Intersperse inline assembly statements within C/C++ source code
- Create executables using a linker that supports multiprocessing, shared memory, and code overlays
- Access numerous math, DSP, and C/C++ runtime library routines
- Create host, link port, and PROM boot images
- Initialize all data and code memory locations using modifiable loader
- Concatenate multiple executables within single PROM image

Overview

VisualDSP++™ is an easy-to-use project management environment, comprised of an integrated development environment (IDE) and debugger. VisualDSP++ enables management of projects from start to finish from within a single interface. The project development and debug environments are integrated, allowing movement easily between editing, building, and debugging activities.



VisualDSP++ interface

Platform and Processor Support

VisualDSP++ supports the SHARC® DSP, TigerSHARC® DSP , Blackfin™ DSP, and the ADSP-218x and ADSP-219x DSP families on Windows® 98, Windows NT, Windows 2000, and Windows XP. Refer to ADI's web site for specifications and availability.

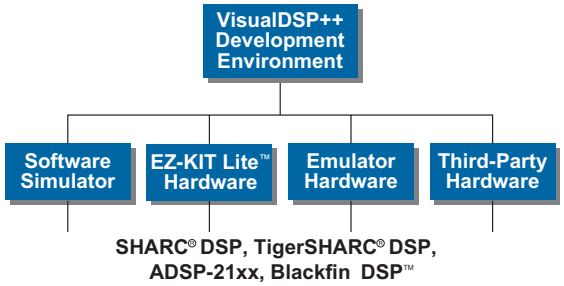
Flexible Project Management

The IDE provides flexible project management for the development of DSP applications. The IDE includes access to all the activities necessary to create and debug DSP projects. The IDE editor allows the creation or modification of source files or viewing of listing or map files. This powerful editor is part of the IDE and includes multiple language syntax highlighting, OLE drag and drop, bookmarks, and standard editing operations such as undo/redo, find/replace, copy/paste/cut, and go to.

The IDE allows access to the DSP C/C++ compiler, C/C++ runtime library, assembler, linker, loader, and splitter. Specification of options for these tools is made possible through the property page dialogs. Property page dialogs are easy to use and simplify configuring, changing, and managing projects. These options may be defined once and then modified to meet changing development needs. The DSP code generation tools can be accessed from the operating system command line.

Greatly Reduced Debugging Time

The VisualDSP++ debugger has an easy-to-use, common interface to all DSP simulators and emulators available through Analog Devices, Inc. (ADI) and from many third party partners. The debugger has many features that greatly reduce debugging time. C/C++ source can be viewed interspersed with the resulting assembly



VisualDSP++ simplifies DSP development via common development environment across all ADI hardware and DSPs

code. Users can profile execution of a range of instructions in a program; set watch points on hardware and software registers, program and data memory; and trace instruction execution and memory accesses. These features enable users to correct coding errors, identify bottlenecks, and examine DSP performance. The custom register option allows developers to select any combination of registers to view in a single window. The debugger, when used with the simulator, can also generate inputs, outputs, and interrupts to simulate real world application conditions. With C++, developers can realize a significant increase in time to market with the ability to efficiently work with complex signal processing data types and take advantage of specialized DSP operations without having to understand the underlying DSP architecture.

VisualDSP++ simplifies DSP development via common development environment across all Analog Devices hardware and DSPs.

VisualDSP++ Kernel

The VisualDSP++ Kernel (VDK) provides state-of-the-art scheduling and resource allocation techniques tailored specifically to address the memory and timing constraints of DSP programming. These techniques enable engineers to use example code more efficiently, eliminating the need to start from the very beginning. The VDK has standard libraries and frameworks with defined APIs that allow easy inclusion of boilerplate, class libraries and value-added IP code.

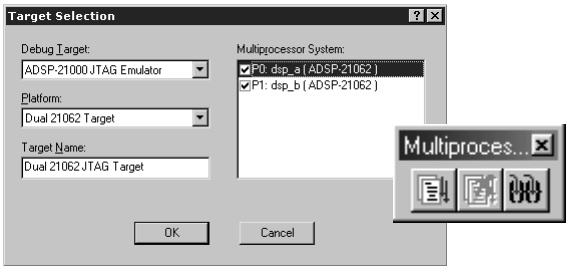
ActiveX

ActiveX allows new functionality to be added by developers and third parties to VisualDSP++ in the form of “plug-ins” that integrate into the VisualDSP++ environment. Third parties will be able to seamlessly port their software to VisualDSP++’s front-end. Developers will be able to merge tool suites together to improve design, analysis and verification thus they will only need to learn one interface to use ADI third party tools.

Multiprocessing Support

VisualDSP++’s smart multiprocessor (MP) debug support provides a seamless interface to multiple DSPs on the same physical hardware. Users are able to issue parallel step, run, and halt commands to all of the applicable DSPs. The developer can pick and choose individual DSP register or memory sets of interest by pinning those that should be updated between runs, halts and steps. This feature also eliminates screen clutter in multiprocessor debugging.

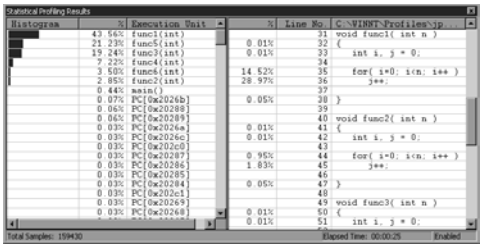
VisualDSP++



VisualDSP++'s multiprocessor dialog box and toolbar

Statistical Profiling

Statistical profiling allows for a more generalized form of profiling that JTAG emulator debug targets can take advantage of. The debugger has the ability to unintrusively random sample the target processors PC and then present the user with a graphical display of the resultant samples. This allows the user to easily see where their application is spending most of its time.



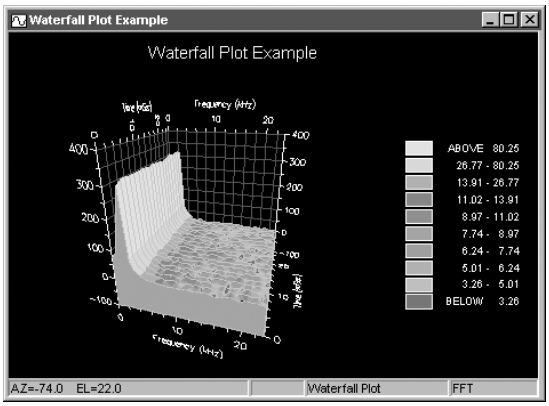
VisualDSP++'s statistical profiling window

Graphical Profiling

The plot window supports exporting images to both bitmap and JPEG format files and has highly configurable formatting options such as title, subtitle, font size, font face, font color and element colors.

Code Generation Tools

DSP code generation tools allow development of applications that take full advantage of the DSPs architecture, including multiprocessing, shared memory, and memory overlays. Code generation tools include the C/C++ compiler, C/C++ runtime library, DSP and math libraries, assembler, linker, loader and splitter. Code generation tools work seamlessly within the VisualDSP++ environment.



VisualDSP++'s plot window

VisualDSP++ Component Software Engineering (VCSE)

VCSE supports an Interface Definition Language (IDL) and compiler that allows developers to create and use components without having to become familiar with the detail of the model and the mechanisms it involves, allowing them to concentrate on the application itself. Component Software is designed to function as a re-usable part of a larger program. Components can easily be integrated into an application and capable of reusability. Integration with VisualDSP++ simplifies the process of incorporating and utilizing components from a variety of developers.

C/C++ Compiler and Assembler

The C/C++ compiler generates efficient code that is optimized for both code density and execution time. The C/C++ compiler can be easily interfaced with assembly code modules. Thus, users can program in C/C++ and still use assembly for time-critical loops. The math, DSP, and C/C++ runtime library routines help shorten time to market. The SHARC DSP, TigerSHARC DSP, Blackfin DSP, ADSP-218x (ADSP-218x does not have C++) and ADSP-219x DSP family assembly language is based on an algebraic syntax that is easy to learn, program, and debug. The enhanced assembler helps the programmer write optimal assembly code by analyzing code sequences and

providing feedback to the user on latencies and stalls. Feedback is given as warnings and informational messages out of the assembler and in the assembler listing.

Linker & Loader

The linker provides flexible system definition through linker description files (.ldf). In a single .ldf file, users are able to define different types of executables for a single or multiprocessor system. The linker resolves symbols over multiple executables, maximizes memory use, and allows common code to be shared among multiple processors. The loader supports creation of host, link port, and PROM boot images. Along with the linker, the loader allows multiprocessor system configuration with smaller code and faster boot time.

Expert Linker

The “Expert” Linker creates a graphical utility that makes it easier for users to produce Linker Definition File (LDF) without having to learn the LDF syntax. The graphical representation of the commands in an LDF file also allows the engineer to manipulate the graphical representation for changes to the LDF or generation of an LDF file. The Expert Linker also allows users to optimize their placement of code.

Cache

The Blackfin DSP simulator collects cache statistics that are associated with both the PC/Source Line and the Cache Line/Set. Collectable statistics are; Total Cache Accesses, Cache Hits, and Cache Misses. There will be three types of displays: Histogram by PC/Source Line, Cache Line Display where hit/miss data is associated by Cache Line/Set(way), Summary Display of totals for hits/misses by cache.

Pipeline Viewer

The Pipeline Viewer is an ActiveX plug-in that allows a user to visually display the instruction flow through the sequencer's pipeline. Stalls, aborts and other pipeline events are graphically displayed. Visualization of the pipeline and of the pipeline events allows a user to better understand where and why latencies and stalls are being introduced into an executable. Armed with this knowledge the user can optimize an executable's instruction sequence to minimize the number of pipeline events.

The DSP Collaborative™

The VisualDSP++ environment enables independent third party companies to add value using ADI’s published set of application programming interfaces (API’s). The DSP Collaborative is a comprehensive collection of DSP development support companies. The DSP Collaborative product offerings – real-time operating systems, emulators, high-level language compilers, and multiprocessor hardware – can interface seamlessly with VisualDSP++ thereby simplifying development across all platforms and targets.

Ordering Information

Please call your local Analog Devices sales representative or distributor for pricing and ordering information. You may also visit the ADI web site and buy online at www.analog.com.

http://www.analog.com/dsp/tools

Development Tools
16-Bit DSP Family and Blackfin™ DSP Family

Development tools from Analog Devices are one of the industry's most complete lines, from the economical EZ-KIT Lite™ evaluation kits to an integrated development environment. These tools are easy to learn and easy to use, and allow designers to bring DSP-based products to market quickly and efficiently.

VisualDSP++ Integrated Development Environment

VisualDSP++™ is a comprehensive toolset for Blackfin DSP, ADSP-218x and ADSP-219x DSPs. VisualDSP++ enables design engineers to easily develop, debug, and deploy code throughout the research, design, development, and test stages of any project. VisualDSP++ integrates all of the code generation tools below:

- Assembler
- Linker
- Simulator
- C/C++ compiler
- Debugger
- PROM splitter
- Graphical plotting
- Expert Linker
- Math, DSP and C/C++ runtime library
- Integrated develoment environment
- VisualDSP++ Kernel
- Statistical profiling
- VisualDSP++ Component Software Engineering

(ADSP-218x does not have C++ support)

EZ-KIT Lite™ Evaluation Kit: The EZ-KIT Lite provides an easy way to evaluate the power of ADI's DSPs and begin to develop applications. These systems consist of a stand-alone evaluation board and an evaluation suite of VisualDSP++ to facilitate architecture evaluations via a PC-hosted tool set. Restrictions: Software is limited for use with the EZ-KIT Lite and program memory is limited in size. With the EZ-KIT Lite users can:

- Evaluate ADI's DSPs
- Learn about DSP applications
- Simulate & debug applications
- Prototype applications

Emulators: Emulators provide non-intrusive target-based debugging of DSP systems. Compact and easy to use, these in-circuit emulators perform a wide range of emulation functions including single-step and full-speed execution with pre-defined breakpoints, viewing and/or altering of register and memory contents. A serial port emulator is available for the ADSP-218x DSP family and JTAG emulators are available for ADSP-219x DSPs and the Blackfin™ DSP family.

Model	Supported DSP
Evaluation Kits	
ADDS-2181-EZLITE	ADSP-2100 Family ADSP-2181
ADDS-2189M-EZLITE	ADSP-218x Family
ADDS-2191-EZLITE	ADSP-219x
ADDS-21535-EZLITE	Blackfin DSP
Development Software	
VDSP-21XX-PC-FULL	ADSP-21xx Family VisualDSP++ IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-21XX-PCFLOAT	ADSP-21xx Family VisualDSP++ Floating License
VDSP-21XX-PC-TEST	ADSP-21xx Family VisualDSP++ Test Drive 30-Day Free Trial
VDSP-BLKFN-PC-FULL	Blackfin DSP Family VisualDSP++ IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-BLKFN-PCFLOAT	Blackfin DSP Family VisualDSP++ Floating License
VDSP-BLKFN-PC-TEST	Blackfin DSP Family VisualDSP++ Test Drive 30-Day Free Trial
Emulators	
ADDS-218X-ICE-2.5V	ADSP-218xM/N Family
ADDS-APEX-ICE	ADSP-219x and Blackfin DSP USB-Based
ADDS-SUMMIT-ICE	ADSP-219x and Blackfin DSP PCI-Based

Development Tools
SHARC® and TigerSHARC® DSP Family

The 32-bit floating-point SHARC® DSP family of products offer the simplicity of floating-point mathematics coupled with high memory integration. With the highest level of floating-point performance, the TigerSHARC® DSP products offer the flexibility of 1, 8, 16 and 32-bit fixed-point math in addition to floating-point arithmetic.

VisualDSP++ Integrated Development Environment

VisualDSP++ is a comprehensive toolset for SHARC and TigerSHARC DSPs. VisualDSP++ enables design engineers to easily develop, debug, and deploy code throughout the research, design, development, and test stages of any project. VisualDSP++ integrates all of the code generation tools below:

- Assembler
- Linker
- Simulator
- C/C++ compiler
- Debugger
- PROM splitter
- Graphical plotting
- Expert Linker
- Math, DSP and C/C++ runtime library
- Integrated develoment environment
- VisualDSP++ Kernel
- Statistical profiling
- VisualDSP++ Component Software Engineering

EZ-KIT Lite™ Evaluation Kit: The EZ-KIT Lite provides an easy way to evaluate the power of ADI's DSPs and begin to develop applications. These systems consist of a stand-alone evaluation board and fundamental debugging software to facilitate architecture evaluations via a PC-hosted tool set. Restrictions: Software is limited for use with the EZ-KIT Lite and program memory is limited in size. With the EZ-KIT Lite users can:

- Evaluate ADI's DSPs
- Learn about DSP applications
- Simulate & debug applications
- Prototype applications

Emulators: Emulators provide non-intrusive target-based debugging of DSP systems. Compact and easy to use, these JTAG emulators perform a wide range of emulation functions including single-step and full-speed execution with pre-defined breakpoints, viewing and/or altering of register and memory contents. DSP emulators are available for PCI and USB host platforms.

Model	Supported DSP
Evaluation Kits	
ADDS-21061-EZLITE	ADSP-2106x Family
ADDS-21160-EZLITE	ADSP-21160M
ADDS-21160N-EZLITE	ADSP-21160N
ADDS-21161N-EZLITE	ADSP-21161N
ADDS-21065L-EZLITE	ADSP-21065L
ADDS-TS101S-EZLITE	ADSP-TS101S
Development Software	
VDSP-SHARC-PC-FULL	SHARC DSP Family VisualDSP++ IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-SHARC-PCFLOAT	SHARC DSP Family VisualDSP++ Floating License
VDSP-SHARC-PC-TEST	SHARC DSP Family VisualDSP++ Test Drive 30-Day Free Trial
VDSP-TS-PC-FULL	TigerSHARC DSP Family VisualDSP++ IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-TS-PCFLOAT	TigerSHARC DSP Family VisualDSP++ Floating License
VDSP-TS-PC-TEST	TigerSHARC DSP Family VisualDSP++ Test Drive 30-Day Free Trial
Emulators	
ADDS-APEX-ICE	USB-Based
ADDS-SUMMIT-ICE	PCI-Based

http://www.analog.com/dsp/tools

The DSP Collaborative™
ADI's Third Party Partner Network

Tap Into the Experience and Global Reach of the DSP Collaborative

Working together to extend your design team

The DSP Collaborative partners (Analog Devices' Third Party Network) offer tools, services and solutions for a wide range of applications/markets:

- Communications
- Audio
- Medical imaging
- Speech processing
- Motor control
- Industrial automation
- Optical networking
- Voice over IP

When you select Analog Devices as your DSP vendor, you're broadening your design team to include the industry-leading resources of the DSP Collaborative. The DSP Collaborative is comprised of over 180 partners who offer more than 700 commercial products, in addition to hundreds of custom solutions that build on more than 35 years of signal processing experience found in every one of our DSPs. These partners offer consulting services as well as a wide range of commercial off-the-shelf (COTS) products. Their development tools are specifically designed to work with Analog Devices' DSP-based systems.

With the DSP Collaborative, you are supported by highly-reputable brands, patented technologies, and the pioneers in real-time system design and debug. The DSP Collaborative partners offer products and services that provide both system and application-level expertise.

Speed up your design process by leveraging the solutions our partners have to offer:

- Algorithms and libraries
- MATLAB® DSP support
- Real-Time Operating Systems
- Development and evaluation boards
- COTS hardware boards
- DSP systems
- Emulators
- Debuggers

Design with Analog Devices' DSP Collaborative team approach with a proven strategy for maximizing your resources!

http://www.analog.com/dsp/3rdparty

The DSP Collaborative™
Key Partners

BittWare, Inc.

BittWare, Inc. is a leading supplier of SHARC-based hardware and software solutions, providing our clients with innovative off-the-shelf and application-specific solutions for their high-performance, real-time signal processing and I/O requirements. Based exclusively on Analog Devices' SHARC technology, BittWare's product family includes innovative standard DSP boards and I/O peripherals on a variety of embedded platforms including PCI bus, CompactPCI, PC/104, PC/104-Plus, PMC, PMC+, and ISA bus. From prototype to high-volume production, off-the-shelf products to application-specific solutions, BittWare is the embedded SHARC DSP solutions provider.

http://www.bittware.com

Transtech DSP

Transtech DSP is a total solutions provider of high performance DSP equipment. Pioneers of multi-processing DSP systems for more than fourteen years, Transtech systems use a number of processors families, including the SHARC and TigerSHARC DSPs, and a choice of industry standard formats such as VME, PCI, PMC and CompactPCI. The company's extensive product line also includes I/O boards, software tools, libraries, drivers, and enclosures, to provide our customers with complete systems or custom designs. Transtech products are used to solve the most computer intensive of signal processing problems, which include radar, sonar, software radio, surveillance and medical imaging.

http://www.transtech-dsp.com

LYRtech Signal Processing (LSP)

LYRtech Signal Processing (LSP) provides engineers with complete, board-level solutions to their signal processing needs. It offers a comprehensive line of mixed DSP/FPGA boards that result in increased performance, cost effectiveness and overall efficiency of developed systems. Simplifying the design task, LSP provides its users with a high-level integration with The MathWorks' MATLAB/SIMULINK tools, as well as Xilinx's System Generator. The integration makes it possible to rapidly implement designs, but later also perform software optimization through low-level schemes (embedded JTAG, optimized libraries, profilers, etc.). Completing the line, LSP provides customers with comprehensive consulting and support packages in the fields of telecommunications and multimedia.

http://www.signal-lsp.com

SPA DSP Software Algorithms

Analog Devices SPA Technology Centre (formerly Signal Processing Associates) is recognized worldwide for providing expertise in DSP solutions for the telecommunications and multimedia industry since 1987. The SPA product range consists of a broad portfolio of DSP software algorithms including speech compression, echo cancellation, fax and data modem-pumps, error correction and numerous other telephony code modules. Typical product application areas are listed below. The SPA Technology Centre is renowned for excellent customer support, product documentation and APIs that allow rapid integration of the code into customer's new product designs.

Audio/Speech Software Algorithms
G.723.1 (5.3/6.3 kbit/s)
G.723.1A (5.3/6.3 kbit/s)
G.729 (8 kbit/s)
G.729A (8 kbit/s)
G.729B (8 kbit/s)
G.729AB (8 kbit/s)
G.728 (16 kbit/s)
G.726 (40/32/24/16 kbit/s)
G.727 (40/32/24/16 kbit/s)
G.722 (64/56/48 kbit/s)
G.711 (64 kbit/s)
Variable Rate Coders
H.32x Audio Modules
Voice Activity Detectors (VAD)
Voice AGC (Variable response time)
Comfort Noise Generator (CNG)
End to End Synchronization

Echo Cancellation Software Algorithms
G.168 Line Echo Canceller (LEC)
G.165 Line Echo Cancellation (LEC)
Acoustic Echo Cancellation (AEC – variable span)
Acoustic Echo Suppression (AES)

Data Modem Software Algorithms	
V.33 (14,400 bps 4-wire)	V.22 (1,200 bps)
V.32bis (14,400 bps)	V.23 (1,200/75 bps)
V.32 (9,600 bps)	Bell 212A (1,200 bps)
V.29 (9,600 bps 4-wire)	Bell 103 (300 bps)
V.22bis (2,400 bps)	V.21 (300 bps)
V.27ter (4,800 bps 4-wire)	

Facsimile Modem Software Algorithms	
V.17 (14,400 bps)	V.27ter (4,800 bps)
V.33 (14,400 bps)	V.21 (300 bps)
V.29 (9,600 bps)	

Forward Error Correction (FEC) Software Algorithms	
Viterbi / Trellis	Interleavers
Reed Solomon	

Telephony Software Algorithms
Relay (4-64 kbit/s transmission of voice/fax/data over internet, satellite, radio, microwave, ISDN, LAN, ATM & other packet networks)
Internet Audio
Speakerphone
DTMF Detector (high performance & Bellcore, EIA, ETSI, Telstra compliant)
DTMF Encoder (high performance & ITU, Bellcore, EIA, ETSI, Telstra compliant)
Call Progress
Caller ID
RTP/JIB (Jitter Buffer)
Ring Detector
E & M Signalling
Tone Detection System (TDS)
Gaussian Noise Source (GNS) Ultra-high quality wideband gaussian noise generator

Product Application Areas	
Internet Telephony	H.324
VoN	H.323
VoIP	H.320
VoDSL	Audioconferencing
VoATM	Videophones/Feature-phones
VoCable	Digital Voice Storage
FoN	Frame Relay
FoIP	PBX Equipment
TRAU/Transcoders	RAS
Basestations	DSVD
Wireless/Mobile	DCME
Gateways	ISDN
CPE/IADs/SOHO/CO	Rural Radio Networks
IP Phones	Satellite/Microwave Systems

SPA DSP Software Algorithms

	Description	Peak MIPS	Average MIPS	PM (Words)	DM (Words)	PM+ (Words)	DM+ (Words)
Vocoders							
G.723.1	5.3 kbit/s	18.4	16.9	9558	11679	0	951
G.723.1	6.3 kbit/s	18.9	17.6	9558	11679	0	951
G.723.1A	5.3 kbit/s + VAD/CNG	18.6	17	9558	11679	0	951
G.723.1A	6.3 kbit/s + VAD/CNG	19.1	17.6	9558	11679	0	951
G.729	8 kbit/s	19.9	18.9	8844	4634	0	1432
G.729A	8 kbit/s (low MIPS)	10.8	10.4	7932	4677	0	1532
G.729B	8 kbit/s + VAD/CNG	20.1	19.3	12064	5405	0	1603
G.729AB	8 kbit/s (low MIPS + VAD/CNG)	12.7	10.8	11900	7700	0	1821
G.728	16 kbit/s	29	27	7947	2272	930	1743
G.726	40/32/24/16 kbit/s	8.5	8	1466	240	47	100
G.727	40/32/24/16 kbit/s	9.9	N/A	1262	252	♦	♦
G.722	64/56/48 kbit/s	12.9	N/A	1458	217	♦	♦
G.711	64 kbit/s	0.4	0.4	111	6	0	0
G.711 (II)	64 kbit/s + adaptive CNG	1	N/A	2011	1700	0	50
Echo Cancellation							
G.165/G.168	16 msec, ECD On	6.6/7.03	N/A	1100/1211	354/412	276	340
G.165/G.168	16 msec, ECD Off	4.5/4.97	N/A	1100/1211	354/412	276	340
G.165/G.168	32 msec, ECD On	9.2/10.6	N/A	1100/1211	354/412	276	340
G.165/G.168	32 msec, ECD Off	7.1/8.57	N/A	1100/1211	354/412	276	340
G.168	64 msec	15	N/A	1000	124	0	1700
G.168	128 msec (sparse)	●	N/A	●	●	●	●
AEC 64 msec span	Acoustic Echo Canceller	5.2	N/A	3153	3059	♦	♦
AEC 128 msec span	Acoustic Echo Canceller	7.2	N/A	3153	3059	♦	♦
AEC 256 msec span	Acoustic Echo Canceller	11.2	N/A	3153	3059	♦	♦
AEC 384 msec span	Acoustic Echo Canceller	15.2	N/A	3153	3059	♦	♦
Telephony							
DTMF	Encoder	0.5	N/A	68	78	2	0
DTMF	Decoder	1	N/A	1300	320	0	256
Caller ID	*Bellcore (I & II)	1.8	N/A	939	53	0	180
Call Progress	*Tone Generation	0.5	N/A	70	80	4	2
TDS	*Tone Detection System	2.5	N/A	1207	641	●	●
VAD	Voice Activity Detection	0.2-2.0	N/A	515	166	0	123
CNG	Comfort Noise Generation	1	N/A	2011	1700	0	50

This table presents only a selection of SPA's most popular ADSP-218x and ADSP-219x based code modules.
Please contact SPA or refer to the SPA web site (www.analog.com/spa) for a full list of available algorithms.

♦ Not currently multiple instance ● Contact SPA for figures * Other Standards on request

SPA DSP Software Algorithms

SPA Code Modules

The table on the previous pages summarize the key resources used by SPA's most commonly used DSP software code modules. Please contact SPA or refer to the SPA web site (www.analog.com/spa) for a full set of available algorithms. Apart from the addition of new modules, SPA also continuously revises existing implementations in order to further reduce MIPS and memory figures.

Optimized Assembler Code

The algorithms presented have been implemented for execution on the Analog Devices ADSP-218x series of fixed-point DSPs and are currently being ported to the new ADSP-219x series of fixed-point DSPs. The code has been written in highly optimized assembler code and is hand-crafted by experienced DSP engineers in order to provide the lowest possible use of DSP resources (MIPS, Program Memory and Data Memory).

MIPS & Multiple Channels

It should be noted that SPA provides both peak and average MIPS figures, as any MIPS budget should use peak figures in order to choose a DSP of sufficient resources. Most of SPA's code modules have been written to be multiple-instance capable. This means multiple channels of the same function can be run on one DSP. For example, six channels of G.729A can be executed concurrently on an 80 MIPS ADSP-218xN DSP.

Program & Data Memory

Running multiple channels of the same algorithm on the same DSP requires only one copy of the program, thus keeping Program Memory (PM) usage low. Each additional instance of the same algorithm also requires less Data Memory (DM), due to re-use of common tables and variables. This is referred to as DM+ in the table overleaf. A similar concept applies to storage of data in Program Memory for additional instances, and is referred to as PM+ in the table.

Multiple Functions

Low MIPS and memory not only allows multiple channels of the same module to be run on one DSP, it also allows many different functions/modules to be run on one DSP. For example, you could run G.723.1, G.729A, G.726, G.168 and DTMF detection simultaneously on one 52 MIPS DSP.

Choice of DSPs

The table on the previous pages allows you to calculate how many MIPS and how much memory will be required by a given set of functions. Knowing these figures, and allowing for any user specific shell or functions, will enable you to select the most appropriate DSP (of sufficient resources) from the ADSP-218x product range. With the release of the new 160 MIPS based ADSP-219x core comes an even higher channel density capability per DSP. Added benefits of the higher MIPS DSPs include lower power consumption per channel and lower board space per channel.

Standards Compliance & Code Quality

SPA code modules are compliant with international standards such as the International Telecommunications Union (ITU) and the voice coders are 100% bit compliant with the ITU test vectors. SPA's algorithms have been extensively tested, are used by numerous companies world-wide and have proven interoperability. SPA code modules have a common Application Programming Interface (API) based on a memory mapped interface scheme. Detailed specification sheets are available for download from the SPA web site (www.analog.com/spa). Other support documentation includes developer's guides and test reports.

Commercial Aspects

SPA can provide demonstration code for evaluation purposes and has excellent customer support to assist with selection and integration issues. Specialized customization and consulting services are also available. SPA provides flexible pricing and licensing arrangements. The benefits of licensing SPA's code, compared to in-house development, include improved time-to-market, experienced support, reduced risk, controlled cost and the ability to allocate resources to other projects.

To Order - Contact SPA

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info@spa.com.au www.analog.com/spa

To truly assess a processor's performance, you have to look beyond MHz, MIPS, or MFLOPS. There are many attributes which may be more accurate predictors of a DSP's real-time embedded processing performance.

Circular Buffers

Circular buffers allow a region of memory to be continually accessed without explicit program interaction. The buffer uses a pointer that automatically resets to the beginning of the buffer (wrap around) if the pointer is advanced beyond the last location in the buffer. Circular buffers are a key feature of DSP routines. Multiple buffers are used in the same routine to store filter coefficients and implement a delay line of input samples. Performance suffers if the DSP core has to perform pointer calculations along with the calculations for the routine. Performance also suffers if the DSP core only supports one circular buffer and must save and restore address registers to implement multiple buffers.

ADI's DSPs have hardware support for multiple circular buffers, eliminating processor overhead for address calculations.

Data Registers

The number of general-purpose data registers available can impact the code performance. Fewer registers require intermediate results to be stored in memory decreasing performance and increasing the load on the memory bus.

ADI DSPs feature a secondary register set which allows for quick context saves when interrupts occur, rather than delaying responses to the interrupt while all register values are saved to memory.

DMA Channels/Non-Intrusive DMA

The DMA (Direct Memory Access) channels transfer data between an external source and the DSP's on-chip memory. With DMA channels, data transfers occur without the core processor having to execute data movement instructions. For example, the overhead clock cycles used to move data for an FFT can add a significant amount of time to overall algorithm execution. With multiple DMA channels available, all data transfers happen without core involvement, eliminating any overhead clock cycles.

One of the strengths of Analog Devices' DSP architecture is that these DMAs do not interfere with the core operation. This capability is referred to as non-intrusive or zero-overhead DMA.

Interrupt Latency

Interrupt latency is a measure of how quickly a DSP responds to an interrupt. Quick response is important especially in real-time processing. For example, an interrupt might indicate the availability of data which is only available for a finite amount of time. Therefore, fast response is critical or the data will be lost.

ADI DSPs feature fast interrupt response time for quick execution of interrupt service routines.

Benchmarks
Comparing DSPs

Multiprocessing Support

Even with the powerful DSPs available today, there are times when the DSP task for a given system does not fit into a single DSP. Examples of such applications include sonar, radar, medical imaging, audio mixers, etc. In these cases, the ability to connect multiple DSPs in a system without any glue logic greatly simplifies the implementation.

ADI offers SHARC DSPs with specialized hardware for glueless multiprocessing.

On-Chip Memory/On-Chip SRAM Size

The amount of on-chip memory available can greatly impact system performance, cost, size, power consumption and complexity. Any time the DSP core accesses external memory, the performance can suffer. Off-chip memory often requires the core to wait additional cycles. In contrast, the DSP core can access on-chip memory at the same rate as its instruction rate. The addition of external memory adds extra components to the system which increases cost, power consumption, and complexity.

ADI leads the industry in DSP SRAM integration. ADI processors have on-chip memories which often eliminate the need for external memory in a system. Furthermore, the memory is configurable for data word size, code word size and storage size. This allows designers to tailor the memory to meet the algorithm requirements.

TDM Mode

TDM (Time Division Multiplexed) mode refers to time division multiplexing which is a common mode for transferring serial data. In telecommunications applications, T1 and E1 lines use TDM. TDM allows multiple serial devices to send and receive information using the same physical connection. TDM also allows communication between multiple DSPs.

All ADI DSPs support TDM mode in the serial ports.

Zero-Overhead Looping

The code for most DSP routines falls naturally into a set of nested loops. Without the support for zero-overhead looping, the DSP core must spend cycles calculating the loop termination values, in addition to the cycles used to process the algorithm's computations. Without zero-overhead looping, performance degrades.

ADI offers 16-bit fixed-point and 32-bit fixed/floating-point DSPs with zero overhead, nestable looping to save instruction cycles.

16-Bit DSP Family Benchmarks

ADSP-21535 Benchmarks	Cycle Count	Execution Time @ 300 MHz
Block FIR Filter	h/2	
Biquad IIR Filter (4 coeff)	2.5*bq	
Complex FIR Filter	2*h	
1024-Point Complex FFT (prescaled)	13938	47 us
256-Point Complex FFT (out-of-place)	3610	12 us
ADSP-219x Benchmarks	**Cycle Count**	**Execution Time @ 160 MHz**
FIR Filter Tap	h	
Biquad IIR Filter (4 coeff)	5*bq	
Complex FIR Filter	4*h	
1024-Point Complex FFT Radix 2	48320	302 us
Division	19	119 ns
Sin/Cos	11	69 ns
Arc Tangent	13	81 ns
In/log10	11	69 ns
ADSP-218x Benchmarks	**Cycle Count**	**Execution Time @ 80 MHz**
FIR Filter Tap	h	
Biquad IIR Filter (4 coeff)	5*bq	
Complex FIR Filter	4*h	
1024-Point Complex FFT Radix 4	37203	465 us
256-Point Complex FFT Radix 4	7423	93 us
Division	19	238 ns
Sin/Cos	25	313 ns
Arc Tangent	13	163 ns
In/log10	11	138 ns
Square Root	23	288 ns

h = # of taps
bq = # of biquads
x = # of samples

BDTImark2000™ Scores

ADSP-21535	(300 MHz)	1690
ADSP-219x	(160 MHz)	420
ADSP-218x	(80 MHz)	240

The BDTImark2000™ is a summary measure of DSP speed, distilled from a suite of DSP benchmarks (not shown) developed and independently verified by Berkeley Design Technology, Inc. A higher BDTImark2000™ score indicates a faster processor. For a complete description of the BDTImark2000™ and underlying benchmarking methodology, as well as additional scores, please visit http://www.bdti.com. BDTImark2000™ (c) 2002 BDTI.

SHARC® DSP Family Benchmarks

Just looking at the cycle time, clock speed, MIPS or MFLOPS of a DSP cannot give an accurate indication of the true performance of the processor. Benchmarks are important in that they show how a particular DSP performs in the context of an application. The smaller the benchmark number, the quicker the algorithm execution. If a DSP can perform the task quicker, the processor can perform more tasks in a given amount of time.

SHARC DSPs are the highest performance 32-bit DSPs available. These processors excel at IEEE floating-point math, 32-bit fixed-point math, and extended precision 40-bit floating-point math.

The ADI 32-bit DSP family offers a maximum performance for minimum system cost, while dramatically shortening product development time and critical time-to-market.

Benchmarks	ADSP-21065L	ADSP-21161N
Clock Speed	66 MHz	100 MHz
Instruction Cycle Time	15 ns	10 ns
MFLOPS Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
MOPS (32-bit Fixed-Point) Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	0.27 ms (SISD)	0.09 ms*
FIR Filter (per Tap)	15 ns	5 ns*
IIR Filter (per Biquad)	60 ns	20 ns*
Matrix Multiply		
(3x3) x (3x1)	135 ns	45 ns*
(4x4) x (4x1)	240 ns	80 ns*
Divide (y/x)	90 ns	60 ns*
Inverse Square Root	135 ns	90 ns*

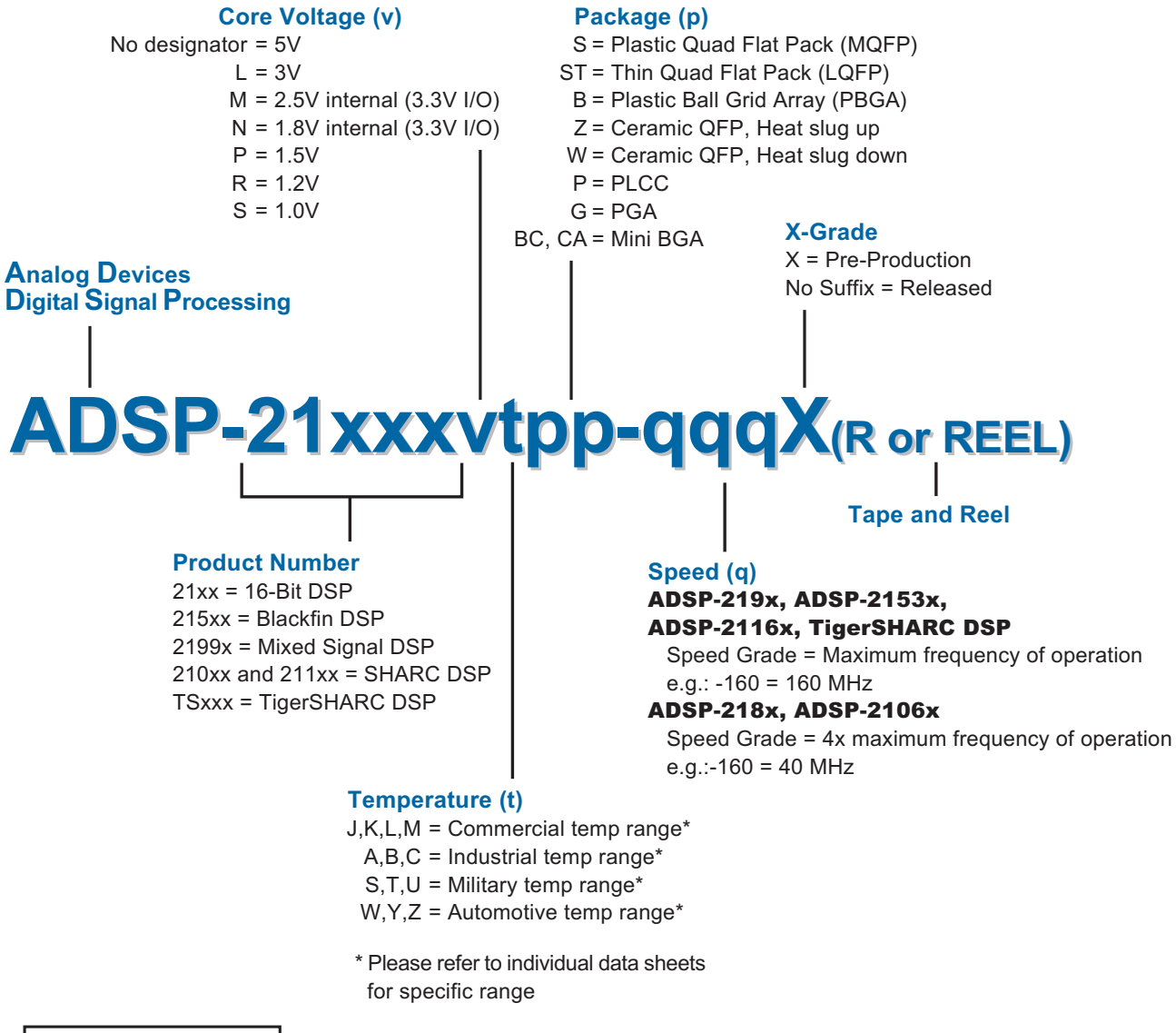
1024-Point Complex FFT (in place)
32-BIT Floating-Point DSPs

DSP Processor	Instruction Rate	Instruction Cycle Time	Number of Cycles	Total FFT Time
TMS320C6701	167 MHz	6 ns	19, 875	0.12 ms
TMS320C6711	150 MHz	6.7 ns	19, 875	0.13 ms
TMS320C6712	100 MHz	10 ns	19, 875	0.19 ms
ADSP-21065L	66 MHz	15 ns	18, 221	0.27 ms
ADSP-21160N	95 MHz	11 ns	10,778*	0.10 ms
ADSP-21161N	100 MHz	10 ns	10,778*	0.09 ms

* These benchmarks provide single channel extrapolation of measured dual channel processing performance.

Specification Source: TI, website www.ti.com

DSP Part Numbering System



Examples:
ADSP-21535PKB-300
ADSP-2191MKST-160X
ADSP-2189NKCA-320
ADSP-21161NKCA100X

Blackfin™ DSP Family

High Performance, Low Power Dual-MAC, 16-Bit Fixed-Point DSP

ADI's new Blackfin DSP family is based on the Micro Signal Architecture (MSA) jointly developed by ADI and the Intel Corporation. Blackfin DSPs enable efficient processing of video, image, and voice data by combining high-performance signal processing functionality with the advantages of a RISC microcontroller instruction set. This unified programming model eliminates the complexities traditionally associated with multiprocessor systems consisting of individual signal and control processing elements.

Highly Parallel Computational Blocks

Computational blocks within the architecture are designed to maximize the number of math operations that can execute within the same cycle. The heart of the Blackfin DSP architecture is the Data Arithmetic Unit that includes two 16-bit Multiplier Accumulators (MACs), two 40-bit Arithmetic Logic Units (ALUs), four 8-bit video ALUs, and a single 40-bit barrel shifter. Each MAC can perform a 16-bit by 16-bit multiply on four independent data operands every cycle. The 40-bit ALUs can accumulate either two 40-bit results or four 16-bit results. With this architecture, 8-, 16- and 32-bit data word sizes can be processed natively for maximum efficiency.

Flexible Addressing Capabilities

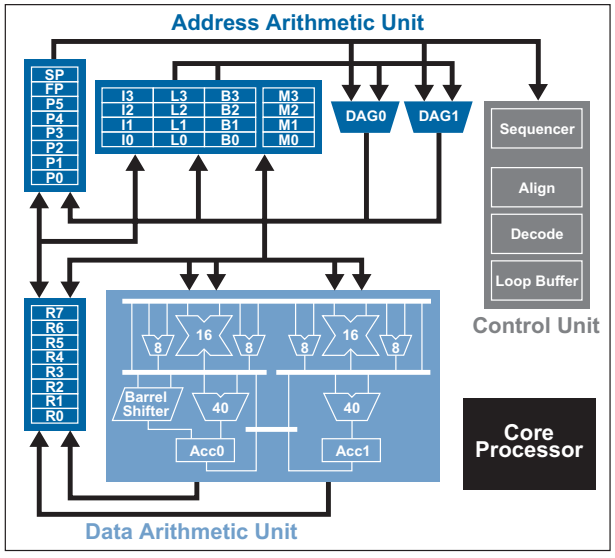
Blackfin DSPs provide efficient addressing of data variables by supporting multiple addressing modes including indirect, auto-increment and decrement, indexed, and bit reversed. Two data address generators (DAG) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file that contains four sets of 32-bit index, modify, length, and base registers useful for implementing multiple circular buffers in internal or external memory. There are also eight additional 32-bit registers – P0 through P5, frame pointer, and stack pointer-- that can be used as pointers for general indexing of variables and stack locations.

Hierarchical Memory

Blackfin DSPs support a hierarchical memory model that expedites memory access to the core for maximized throughput. The L1 memory is connected directly to the core and operates at full system clock speed. L2 memory, also operating at full system clock speed, is utilized for accessing larger, bulk arrays of program and data memory.

To provide for the performance needs of a DSP and the programming ease of a RISC MCU, L1 memory can be configured as SRAM, cache, or a combination of both. System designers can map critical DSP data sets that require high bandwidth and low latency into SRAM, while maintaining the simple cache programming model for microcontroller code.

The Memory Management Unit provides a memory protection mechanism that, when coupled with the core's User and Supervisor modes, can support a full OS Kernel, a feature not typically found on general-purpose DSPs.



Dynamic Power Management

Blackfin DSP Dynamic Power Management permits system designers to dynamically vary both the operating frequency and voltage of the DSP. This capability enables the DSP power consumption characteristics to be optimized to the individual algorithm being executed. Transitions between various performance levels can be implemented under user control resulting in significantly lower system power consumption and longer battery life for handheld devices.

Superior Code Density

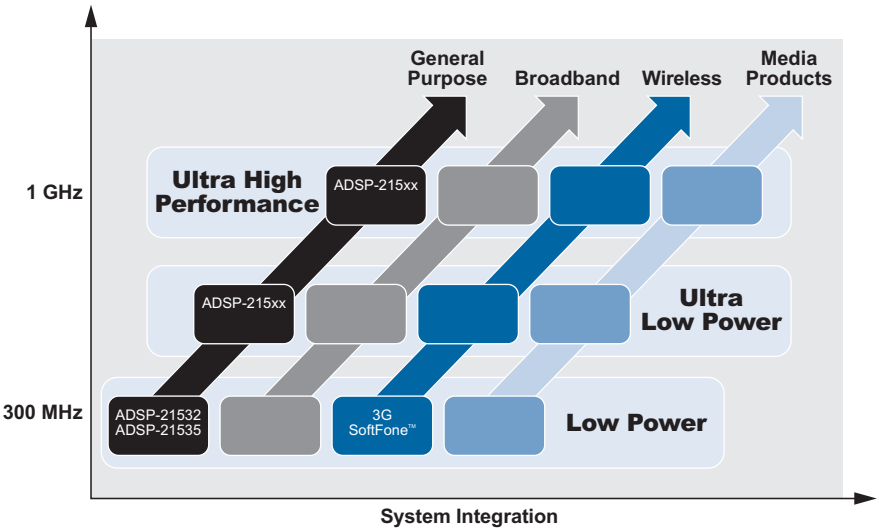
Blackfin DSPs provide excellent code density by employing a variable length instruction encoding scheme. The more frequently used instructions such as data moves are encoded as compact 16-bit words. The more challenging DSP and math operations are encoded as 32-bit double words. Additionally, a 64-bit multi-operation packet consisting of one 32-bit and two 16-bit words can be constructed for a variety of instruction combinations. This merging of CISC and RISC instruction encoding formats enables excellent code density while retaining high system performance. Blackfin DSPs also support both 16-bit and 32-bit external memory arrays with no memory alignment restrictions.

Video Instructions

Blackfin DSPs integrate quad 8-bit video ALUs that facilitate the processing of arrays of 8-bit data – the common word size of red-green-blue pixel processing algorithms. The Blackfin DSP instruction set architecture also includes specific pixel manipulation instructions. These instructions enable the optimized execution of algorithms such as MPEG-2, MPEG-4, and JPEG compression and decompression. Implementing video algorithms in software allows OEMs to adapt to evolving standards and new functional requirements without hardware changes.

Roadmap to Maximum Performance

The current Blackfin DSP family combines performance of 300 MHz/600 MMACs with a robust and complete set of peripherals. Future product offerings will extend this performance base to 1 GHz/2 GMACs with expanded peripheral functionality. Blackfin DSP technology will also be leveraged to provide application specific solutions for a variety of rapidly growing vertical market segments including wired/wireless communications and digital imaging. These complete solutions combine optimized hardware components with validated software components.



ADSP-21535 Blackfin™ DSP

High Performance 16-Bit DSP for Networking & Digital Imaging

The new ADSP-21535 combines a high performance DSP, Dynamic Power Management, programming ease of use with a rich, powerful peripheral set in order to be the central element for a variety of application solutions with a minimum of external components and cost.

Features

- High-performance 300 MHz/600 MMAC dual-MAC DSP core
- 308 KBytes of On-Chip Memory
  - 16 KBytes of L1 Program Memory
  - 36 KBytes of L1 Data Memory
  - 256 KBytes of Unified L2 Memory
- External Memory Controller with glueless support for synchronous and asynchronous memories
- Memory Management Unit providing memory protection
- 32-bit 33 MHz PCI V2.2 interface with both master and slave functionality
- USB Device V1.1 controller supporting up to 8 endpoints
- Two full-duplex Synchronous Serial ports (SPORTs)
- Three 32-bit timer/counters supporting PWM output and pulse width/event count input modes
- 12 channel peripheral and memory DMA controller capable of internal, external and PCI transfers
- Two UARTs with auto-baud capability (one supports IrDA® functionality)
- Two SPI-compatible ports
- 16 General Purpose I/O
- PLL capable of 1x to 31x frequency multiplication
- Event controller
- Real-time clock
- Watchdog timer
- Debug/JTAG interface
- Commercial and industrial temperature range
- 260-Lead (19 mm x 19 mm) PBGA package

Benefits

- World's first truly high-performance DSP processor with integrated RISC MCU functionality and multimedia processing capabilities in a single instruction set
- Flexible Software Controlled Dynamic Power Management
- Optimized compiler and architecture that supports development in High Level Languages like C/C++ while also delivering comparable code densities of traditional microcontrollers.
- Variety of architectural features that support efficient use of a full RTOS to manage application tasks

Applications

- Automotive applications
- Broadband home gateways
- Central office/network switch
- Digital imaging and printing
- Global positioning systems
- Home networking/wireless LAN
- Industrial signal processing
- Internet appliances
- Internet audio
- Modem solutions
- Private Branch Exchanges (PBX)
- Telecommunications
- Video conferencing
- VoIP phone solutions

Model	L1/L2 Memory	MHz	Pin/Pkg	Price* (1000)
ADSP-21535PKB-300	52KB/256KB	300	260-PBGA	$32.00
ADSP-21535PKB-200	52KB/256KB	200	260-PBGA	$30.00
ADSP-21535PBB-200	52KB/256KB	200	260-PBGA	$31.00

K = Commercial Temp (0ºC to +85ºC Case)
B = Industrial Temp (-40ºC to +105ºC Case)
* All pricing is budgetary – subject to change

ADSP-21532 Blackfin™ DSP

Low Cost, 16-Bit DSP for Consumer Multimedia

The ADSP-21532 is a low cost member of the Blackfin DSP family. The ADSP-21532 integrates a variety of general purpose and application-tuned peripherals that minimize the overall system IC count and bill of materials costs. This system integration and enhanced peripheral set make the ADSP-21532 particularly well suited for consumer multimedia and other cost sensitive applications including video security systems, video-enabled information appliances, Internet audio and video, and home and car entertainment.

Features

- High-performance 300 MHz/600 MMAC dual-MAC DSP core
- 116 KBytes of on-chip L1 memory
  - 48 KBytes Program RAM
  - 32 KBytes Program ROM
  - 36 KBytes Data RAM
- External Memory Controller with glueless support for synchronous and asynchronous memories
- Memory Management Unit providing memory protection
- Parallel Peripheral Interface supporting ITU-R 656 video data formats
- Two dual-channel, full-duplex Synchronous Serial Ports (SPORTs) supporting eight stereo I²S channels
- Three 32-bit timer/counters supporting PWM output and pulse width/event count input modes
- 12 channel peripheral and memory DMA controller supporting one and two-dimensional data transfers
- Three timer/counters supporting PWM and pulse width/event count modes
- UART with support for IrDA®
- SPI-compatible port
- PLL capable of 1x to 31x frequency multiplication
- Event handler
- Real-time clock
- Watchdog timer
- Debug/JTAG interface
- 160-lead (12 mm x 12 mm) Mini-BGA package
- Industrial temperature range

Benefits

- Flexible, software-controlled Dynamic Power Management with on-chip voltage regulation from 2.25V to 3.6V input supply
- Enhanced instructions to process audio, image, and video data in multimedia applications
- Enhanced interfaces enabling glueless connection to a variety of audio, video, and multimedia data converters
- User definable ROM option reduces the requirement for external components and minimizes system bill of materials costs

Applications

- Automotive telematics
- Biometrics
- Games and learning aids
- Home theatre
- Information appliances
- Internet audio
- Set top boxes
- Video conferencing
- Video security and surveillance

Model	L1 Memory	MHz	Pin/Pkg	Price* (1000)
ADSP-21532SBCA-300	116KB	300	160-MiniBGA	$11.50

B = Industrial Temp (-40ºC to +105ºC Case)
* All pricing is budgetary – subject to change

ADSP-2100 Architecture
Providing over 15 Years of Code-Compatible DSP Excellence

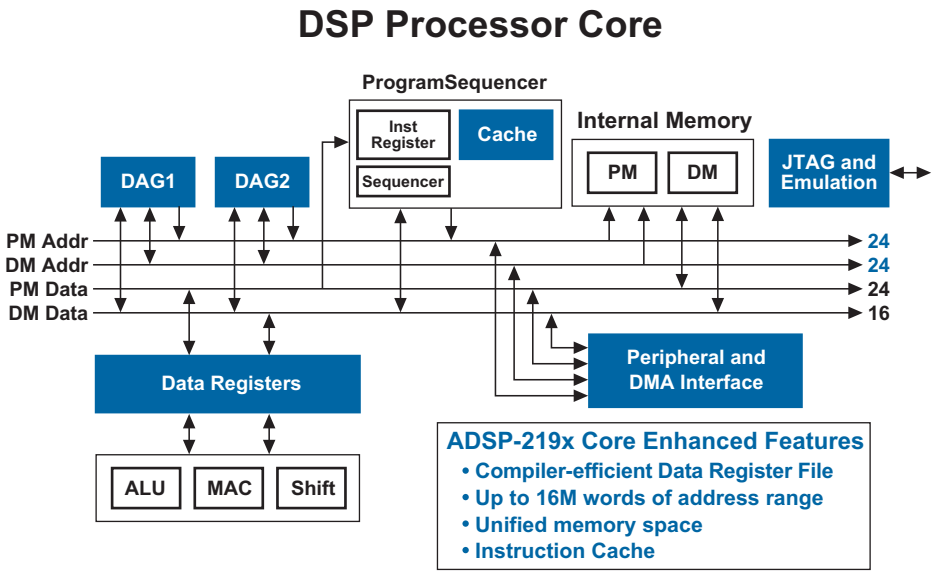
The ADSP-2100 family architecture is built around a common instruction set architecture (ISA) which is optimized for signal processing. All instructions are executed in a single clock cycle, including multi-function instructions. The architecture also features a high level algebraic programming syntax.

In addition, ADSP-21xx processors operate on 24-bit instructions and 16-bit data. The wider instruction word allows the device to use a more complex and robust instruction set than a 16-bit opcode. The 16-bit data word provides wide dynamic range, while the narrower bus width (16-bit as opposed to 32- or 64-bit wide) reduces power consumption.

Processors are available with up to 2.4 Mbits of SRAM around the DSP core to increase code execution and overall system performance. All ADSP-21xx processors integrate a programmable DMA controller to support maximum I/O throughput and processor efficiency. The ADSP-218x supports up to 4 Mbytes of external memory while the ADSP-219x architecture increases its address bus to 24-bits to support a total of 16M words of external memory. The ADSP-219x also balances a high performance processor core with high performance buses (PM, DM, DMA). It also provides two 40-bit accumulators and a 40-bit shifter, which help minimize data overflow during complex operations.

Addressing modes

ADSP-21xx processors also support immediate, register-direct, memory-direct, and register-indirect addressing modes. The ADSP-219x adds register, indirect-post-modify, immediate-modify, and direct- and indirect-offset addressing modes. Each address generator supports as many as four circular buffers, each with three registers. The ADSP-219x supports as many as 16 circular buffers using a DAG shadow register set and a set of base registers for additional circular-buffering flexibility.



ADSP-2100 Architecture

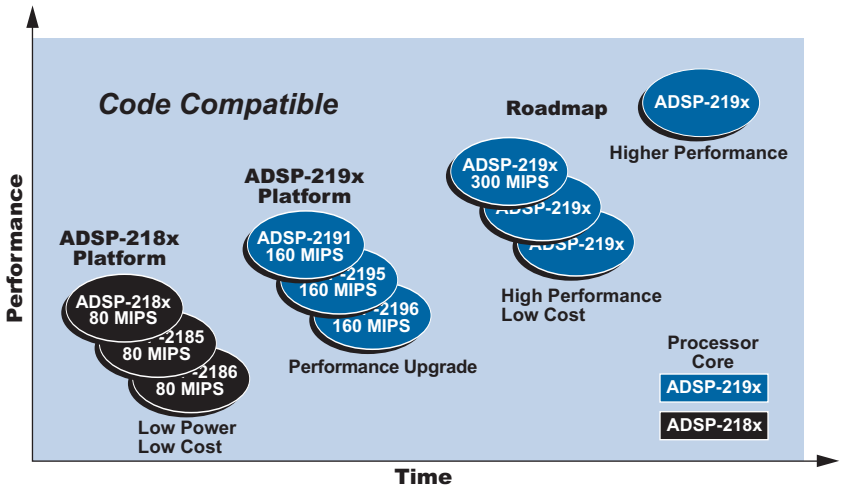
Providing over 15 Years of Code-Compatible DSP Excellence

Special Instructions

The ADSP-2100 architecture contains dedicated loop hardware and a "DO UNTIL" loop instruction that supports loops ranging from zero to 16K iterations, or loops with infinite iterations. The ADSP-218x supports up to four-deep nesting via its loop hardware and the ADSP-219x supports as many as eight. In addition to the standard arithmetic and logic instructions, the ALU (arithmetic-logic unit) supports division primitives. The ADSP-219x program sequencer features a 6-deep pipeline, and supports delayed branching. The ADSP-219x buses and instruction cache also provide rapid, unimpeded data flow to the core to maintain the high execution rate.

Compiler Friendly

Many of the enhancements to the ADSP-219x architecture were made to improve compiler efficiency. More flexible DAG addressing modes, added secondary DAG register, increased depth to stacks, and extended address reach to 16M words drastically improves compiler code efficiency.



ADSP-219x Family
160 MHz DSPs for Telephony and Signal Processing

The ADSP-219x series represent ADIs newest generation of ADSP-2100 code-compatible, fixed-point DSPs operating at 160 MHz. DSPs in this series integrate a high level of system interfaces to provide DSP developers with a rapid upgrade path to higher performance and lower system cost. The ADSP-219x DSP peripheral set has been optimized for Telephony applications by integrating three multi-channel serial ports that support up to 128 TDM channels, a 16-bit parallel and 16-bit host interface – this enables rapid deployment of cost effective voice platforms. The DSPs integrate up to 32K words of 24-bit program memory RAM, 32K words of 16-bit data memory RAM, and 16K words of 24-bit ROM. The ADSP-2191, ADSP-2195, and ADSP-2196 are all pin-compatible allowing many possibilities for system upgrades. Pin-to-pin compatibility allows programmers to migrate to larger memory models to increase end-product functionality without hardware redesign.

Features

- 160 MHz / MIPs 16-bit performance
- Up to 64K words on-chip SRAM
- 16K words on-chip ROM
- Boot ROM
- 16-bit external memory interface
- Host port interface (8- or 16-bit)
- Three full duplex multi channel TDM serial ports
- Two SPI interfaces
- One UART
- Three general purpose timers with PWM and input capture modes
- 16 general purpose I/O pins
- 11 DMA channels
- On-chip PLL with 1x to 32x input frequency multiplication
- IEEE JTAG 1149.1 test access port
- 2.5 volt supply with 3.3 volt I/O
- 144-Lead LQFP, 144-Lead mini-BGA

Benefits

- Programmable PLL with oscillator enables full speed operation from low-speed input clocks or crystals
- User selectable power-down modes reduces system power consumption
- On-chip ROM with application specific user code lowers cost in high volume systems
- Up to 11 DMA channels operate in parallel maximizes I/O throughput
- Efficient C/C++ compiler simplifies software programming task

Applications

- Telephony
- Modems
- Private Branch Exchange (PBX)
- Voice over network
- Home gateways
- Integrated access devices
- Optical networking
- Data acquisition
- Industrial automation

Model	DM RAM	PM RAM	PM ROM	MHz	Pin/Pkg	Price* (1000)
ADSP-2191MKST-160	32K	32K	–	160	144-LQFP	$16.85
ADSP-2191MBST-140	32K	32K	–	140	144-LQFP	$16.85
ADSP-2191MKCA-160	32K	32K	–	160	144-MBGA	$16.85
ADSP-2191MBCA-140	32K	32K	–	140	144-MBGA	$16.85
ADSP-2195MKST-160	16K	16K	16K	160	144-LQFP	$13.90
ADSP-2195MBST-140	16K	16K	16K	140	144-LQFP	$13.90
ADSP-2195MKCA-160	16K	16K	16K	160	144-MBGA	$13.90
ADSP-2195MBCA-140	16K	16K	16K	140	144-MBGA	$13.90
ADSP-2196MKST-160	8K	8K	16K	160	144-LQFP	$11.10
ADSP-2196MBST-140	8K	8K	16K	140	144-LQFP	$11.10
ADSP-2196MKCA-160	8K	8K	16K	160	144-MBGA	$11.10
ADSP-2196MBCA-140	8K	8K	16K	140	144-MBGA	$11.10

M indicates 2.5 volt operation
K = Commercial Temp (0ºC to +70ºC ambient)
B = Industrial Temp (-40ºC to +85ºC ambient)
* All pricing is budgetary – subject to change

ADSP-218x M and N Series
16-Bit Fixed-Point Digital Signal Processors

The ADSP-218x M and N series members offer low power (1.8V), low cost, and high performance 16-bit DSPs. All series members are pin and code compatible and are differentiated solely by the amount of on-chip SRAM. These feature combined with ADSP-21xx code compatibility provide a great deal of flexibility in the design decision.

Features

- .3mA/MIP@ 1.8V core supply[1]
- 12.5 ns instruction cycle time (80 MIPS)[2]
- Up to 48K words program RAM and 56K words data words on chip
- I/O voltage support to 3.3V
- 16-bit bit internal DMA port
- 8 bit memory DMA
- Two double buffered serial ports (1 with TDM mode)
- I/O memory interface with 2048 locations
- 100-lead LQFP, 144-lead mini-BGA

Benefits

- Simple algebraic assembly language reduces development time and time to market
- Pin compatible packages mitigates product developments risks
- 16-bit bit DMA port makes bus interfacing easier
- Code compatible with all 21xx derivatives ensures reuse of legacy code
- Large on chip memory eliminates the need for expensive SRAM
- 144-ball mini-BGA package provides for maximum space savings (10 mm x 10 mm)

Applications

- Consumer telephony
- Embedded speech processing
- POS terminals
- PBX
- Smart card readers
- Multi channel voice processing
- Industrial measurement control

[1] .5mA/Mip, 75 MIPS on 'M' series
[2] 13 ns on 'M' series

Model	PM/DM	MHz	Pin/Pkg	Price* (1000)
ADSP-2188NBST-320	48K/56K	80	128-LQFP	$26.00
ADSP-2188NBCA-320	48K/56K	80	144-MBGA	$28.00
ADSP-2189NBST-320	32K/48K	80	128-LQFP	$21.00
ADSP-2189NBCA-320	32K/48K	80	144-MBGA	$23.00
ADSP-2187NBST-320	32K/32K	80	128-LQFP	$17.00
ADSP-2187NBCA-320	32K/32K	80	144-MBGA	$19.00
ADSP-2185NBST-320	16K/16K	80	128-LQFP	$9.50
ADSP-2185NBCA-320	16K/16K	80	144-MBGA	$12.00
ADSP-2186NBST-320	8K/8K	80	128-LQFP	$7.25
ADSP-2186NBCA-320	8K/8K	80	144-MBGA	$9.25
ADSP-2184NBST-320	4K/4K	80	128-LQFP	$5.75
ADSP-2184NBCA-320	4K/4K	80	144-MBGA	$7.75
ADSP-2188MBST-266	48K/56K	75	128-LQFP	$28.00
ADSP-2188MBCA-266	48K/56K	75	144-MBGA	$30.00
ADSP-2189MBST-266	32K/48K	75	128-LQFP	$23.00
ADSP-2189MBCA-266	32K/48K	75	144-MBGA	$25.00
ADSP-2185MBST-266	16K/16K	75	128-LQFP	$10.00
ADSP-2185MBCA-266	16K/16K	75	144-MBGA	$12.00
ADSP-2186MBST-266	8K/8K	75	128-LQFP	$7.50
ADSP-2186MBCA-266	8K/8K	75	144-MBGA	$9.50
ADSP-2188NKST-320	48K/56K	80	128-LQFP	$26.00
ADSP-2188NKCA-320	48K/56K	80	144-MBGA	$28.00
ADSP-2189NKST-320	32K/48K	80	128-LQFP	$21.00
ADSP-2189NKCA-320	32K/48K	80	144-MBGA	$23.00
ADSP-2187NKST-320	32K/32K	80	128-LQFP	$17.00
ADSP-2187NKCA-320	32K/32K	80	144-MBGA	$19.00
ADSP-2185NKST-320	16K/16K	80	128-LQFP	$9.50
ADSP-2185NKCA-320	16K/16K	80	144-MBGA	$12.00
ADSP-2186NKST-320	8K/8K	80	128-LQFP	$7.25
ADSP-2186NKCA-320	8K/8K	80	144-MBGA	$9.25
ADSP-2184NKST-320	4K/4K	80	128-LQFP	$5.75
ADSP-2184NKCA-320	4K/4K	80	144-MBGA	$7.75
ADSP-2188MKST-300	48K/56K	75	128-LQFP	$28.00
ADSP-2188MKCA-300	48K/56K	75	144-MBGA	$30.00
ADSP-2189MKST-300	32K/48K	75	128-LQFP	$23.00
ADSP-2189MKCA-300	32K/48K	75	144-MBGA	$25.00
ADSP-2185MKST-300	16K/16K	75	128-LQFP	$10.00
ADSP-2185MKCA-300	16K/16K	75	144-MBGA	$11.50
ADSP-2186MKST-300	8K/8K	75	128-LQFP	$7.50
ADSP-2186MKCA-300	8K/8K	75	144-MBGA	$9.50

N indicates 1.8 volt operation
M indicates 2.5 volt operation
B = Industrial Temp (-40ºC to +85ºC ambient)
K = Commercial Temp (0ºC to +70ºC ambient)
* All pricing is budgetary – subject to change

16-Bit DSP Competitor Cross Reference Guide

Competition					ADI Suggested Functional Competitive Device
Device Part Number	MMACS	RAM (Kwords)	Operating Voltage (Core, I/O)	Smallest Package	
Texas Instruments C54X Family					
TMS320VC5441	532	640	1.6V/3.3V	179BGA	ADSP-21535P
TMS320VC5421	200	256	1.8V/3.3V	144BGA	ADSP-21535P
TMS320VC5420	200	200	1.8V, 3.3V	144BGA	ADSP-21535P ADSP-2191M
TMS320VC5416	160	128	1.5V,3.3V	144BGA	ADSP-2191M ADSP-2188N
TMS320VC5410A	160	64	1.6V/3.3V	144BGA	ADSP-2191M
TMS320VC5409A	160	32	1.6V/3.3V	144BGA	ADSP-2195M
TMS320VC5402A	160	16	1.6V/3.3V	144BGA	ADSP-2196M
TMS320VC5407	120	40	1.5V/3.3V	144BGA	ADSP-2195M
TMS320VC5404	120	16	1.5V/3.3V	144BGA	ADSP-2196M
TMS320UC5409	80	32	1.8V - 3.6V	144BGA	ADSP-2185N
TMS320UC5402	80	16	1.8V - 3.6V	144BGA	ADSP-2186N
TMS320VC5401	50	8	1.8V/3.3V	144BGA	ADSP-2184N
Texas Instruments C55X Family					
TMS320VC5510	400	160	1.6V/3.3V	240BGA	ADSP-21535P
TMS320VC5509	400	128	1.5V/3.3V	176BGA	ADSP-21535P
TMS320VC5502	400	32	1.5V/3.3V	176BGA	ADSP-21532S
Texas Instruments C62X Family					
TMS320C6203C	600	448	1.2V/3.3V	352BGA	ADSP-21535P
TMS320C6202B	500	192	1.5V/3.3V	352BGA	ADSP-21535P
TMS320C6201	400	64	1.8V/3.3V	352BGA	ADSP-21532S
TMS320C6204	400	64	1.5V/3.3V	288BGA	ADSP-21532S
TMS320C6205	400	64	1.5V/3.3V	288BGA	ADSP-21532S
TMS320C6211B	334	36	1.8V/3.3V	384BGA	ADSP-21532S
Analog Devices					
ADSP-21535P	600	154	1.5V/3.3V	260BGA	
ADSP-21532S	600	58	2.25 - 3.6V*	160BGA	
ADSP-2191M	160	64	2.5/3.3V	144BGA	
ADSP-2195M	160	32	2.5/3.3V	144BGA	
ADSP-2196M	160	16	2.5/3.3V	144BGA	
ADSP-2188N	80	104	1.8V,2.5-3.6V	144BGA	
ADSP-2189N	80	80	1.8V,2.5-3.6V	144BGA	
ADSP-2187N	80	64	1.8V,2.5-3.6V	144BGA	
ADSP-2185N	80	32	1.8V,2.5-3.6V	144BGA	
ADSP-2186N	80	16	1.8V,2.5-3.6V	144BGA	
ADSP-2184N	80	8	1.8V,2.5-3.6V	144BGA	
ADSP-2188M	75	104	2.5V, 2.5V-3.3V	144BGA	
ADSP-2189M	75	80	2.5V, 2.5V-3.3V	144BGA	
ADSP-2185M	75	32	2.5V, 2.5V-3.3V	144BGA	
ADSP-2186M	75	16	2.5V, 2.5V-3.3V	144BGA	

* External voltage range -- Core voltage regulation on-chip

SHARC® DSP Family
Real-Time, Multiprocessing Leader

The Analog Devices SHARC® DSP family features a "super" Harvard architecture optimized to enable a variety of real-time embedded applications. These 32-bit DSPs allow users to program with equal efficiency in both fixed-point and floating-point arithmetic. The unique memory architecture – two large on-chip, dual-ported SRAM blocks coupled with the sophisticated I/O processor – gives the SHARC DSPs the bandwidth for sustained high-speed computations for real-time embedded DSP development.

Code-compatibility helps to keep development time at a minimum, and maximize our customers' software investments.

The original Single-Instruction, Single-Data (SISD) SHARC DSPs feature a broad range of memory sizes and price points. For very high performance applications, ADI has extended the architecture to a code-compatible, Single-Instruction, Multiple-Data (SIMD) platform.

The next generation TigerSHARC 128-bit DSP combines multiple computation units for floating-point and fixed-point processing, as well as very wide word widths, by using a Multiple-Instruction, Multiple Data (MIMD) platform. Its ultra-high-performance static superscaler architecture is optimized for computationally demanding and multiprocessor applications.

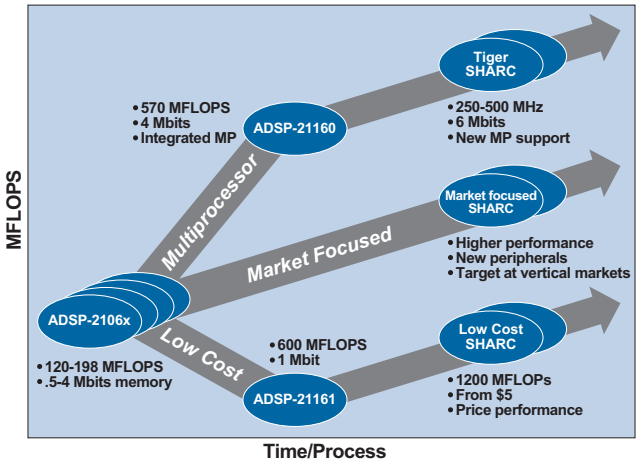
SHARC DSPs are the leader in multiprocessing applications. Patented link port technology has helped establish SHARC as a de facto standard.

Applications

- Prosumer audio
- 3D graphics
- Arcade games
- Imaging
- Video conferencing
- Medical imaging
- Radar and sonar guidance
- Audio equipment
- Call processing
- Speech recognition
- Cellular base stations
- Instrumentation

SHARC Roadmap

Commitment to Code Compatibility into Tomorrow



32-BIT Generic	Package	Max MIPS	Vcc	On-Chip SRAM	Serial Ports	Price* (1000)
ADSP-21160N	B	95	1.9/3.3V	4 Mbits	2	$145.00
ADSP-21160M	B	80	2.5/3.3V	4 Mbits	2	$145.00
ADSP-21161N	CA	100	1.8/3.3V	1 Mbit	2	$24.63
ADSP-21065L	S, CA	66	3.3V	544 Kbits	2	$19.50
ADSP-21062/L	B,S	40	3.3/5V	2 Mbits	2	$100.00
ADSP-21061/L	S	50	3.3/5V	1 Mbit	2	$37.43
ADSP-21060/L	B,S	40	3.3/5V	4 Mbits	2	$249.29
ADSP-TS101S	B	250	1.2/3.3V	6 Mbits	0	$207.00

Package: B = Plastic Ball Grid Array (PBGA) S = Plastic Quad Flat Pack (PQFP)
G = Ceramic Pin Grid Array (PGA) CA = Mini Ball Grid Array (MBGA)

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities
All pricing is budgetary - subject to change

ADSP-TS101
Next Generation SHARC® DSP

The ADSP-TS101 is the newest member of the high performing SHARC® DSP family. Operating at 250 MHz, TigerSHARC DSP offers best-in-class floating-point performance at a minimum power consumption. The TigerSHARC DSP supports arithmetic for 8-, 16-, and 32-bit data, and contains 6 Mbit on-chip SRAM internally organized in three banks with user-defined partitioning. Three internal 128-bit wide internal buses provide a total memory bandwidth of 8.64 Gbytes per second.

Features

- 2 billion 16-bit MACs-per-second
- 550 MFLOP/watt – industry best
- 1.2 volt supply with 3.3 volt I/O
- 4.0 ns instruction cycle time at 250 MHz
- Eight 16-bit MACs/cycle with 40-bit accumulation
- Two 32-bit MACs/cycle with 80-bit accumulation
- 6 Mbit on-chip SRAM
- IEEE floating-point compatible
- 14 DMA channels
- 4 Link ports – 1 GByte/sec transfer rate, aggregate
- 32/64-bit external port – 800 MBytes/sec
- 128 general purpose registers
- Optimizing C/C++ compiler
- Glueless multiprocessing
- 19 x 19 mm or 27 x 27 mm PBGA

Benefits

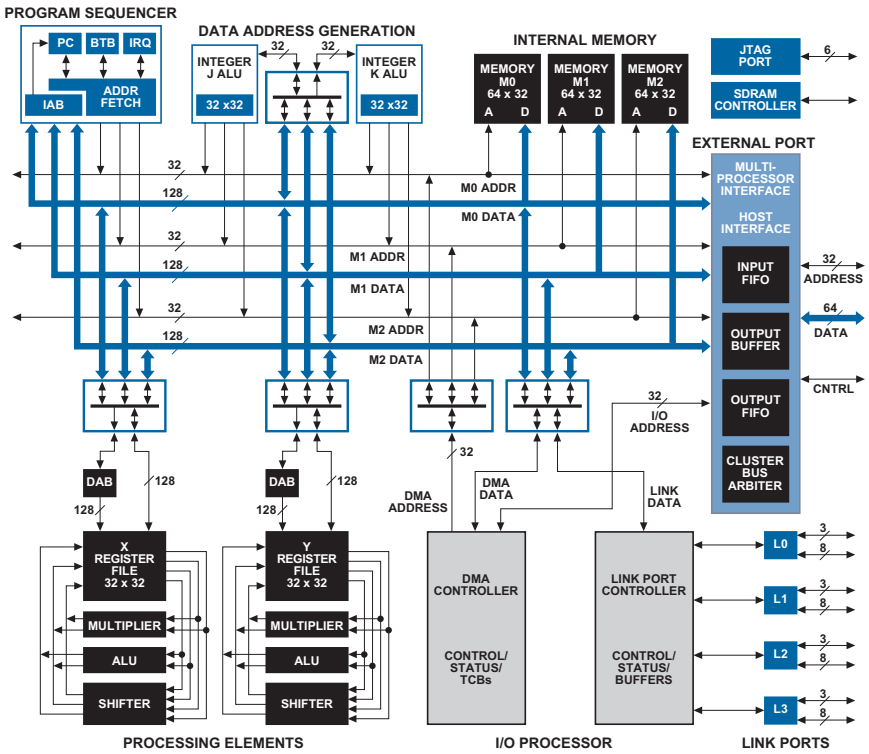
- Flexible development environment that supports both algebraic assembly language and C/C++
- Large on-chip RAM makes reprogramming easy
- 4 Link ports enable direct chip-to-chip connections without the need for complex external circuitry
- VisualDSP++ tools support provides same software interface as other ADI DSPs
- Multiple-instruction, multiple-data (MIMD) instructions
- Fully interruptible with full computation performance

Applications

- Medical, CT, ultrasound
- Sonar systems
- Echo and noise cancellation systems
- Flight simulator
- Infrastructure equipment
- Military smart munitions
- Test equipment
- Imaging, printers, video

Model	MHz	Pkg
ADSP-TS101SKB1250X	250	27 x 27 mm PBGA
ADSP-TS101SKB2250X	250	19 x 19 mm PBGA
K = Commercial Temp (-40ºC to +85ºC case)		

Development Tools	
ADDS-TS101S-EZLITE	Evaluation Kit
VDSP-TS-PC-FULL	VisualDSP++
VDSP-TS-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator



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ANALOG DEVICES

ADSP-21161N

Low-Cost, Single-Instruction, Multiple-Data (SIMD) SHARC®

The ADSP-21161N is the newest member of the high performing SIMD SHARC DSP family. This device offers the industry's highest 32-bit DSP performance at a price that will support consumer applications.

Features

- 3.3 Volt external/1.8 volt internal
- 1 Mbit on-chip SRAM
- 14 zero-overhead DMA channels
- SPI-compatible port for serial host and peripheral control
- 4 SPORTs supporting 128 channel TDM and I²S
- 12 general purpose I/O lines, 4 IRQ lines,1 timer
- Code-compatible to all other SHARC family DSPs
- Single-Instruction, Multiple-Data (SIMD) computational architecture – two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file
- 100 MHz (10 ns) core instruction rate 600 MFLOPS peak and 400 MFLOPs sustained performance
- Dual Data Address Generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- 225-ball 17 mm x 17 mm PBGA package

Model	MHz	Pin/Pkg	Price* (1000)
ADSP-21161NKCA-100	100	225-MBGA	$24.63
ADSP-21161NCCA-100	100	225-MBGA	$29.55

N indicates 1.8 volt operation
K = Commercial Temp (0ºC to +85ºC case)
C = Industrial Temp (-40ºC to +105ºC case)
* All pricing is budgetary – subject to change

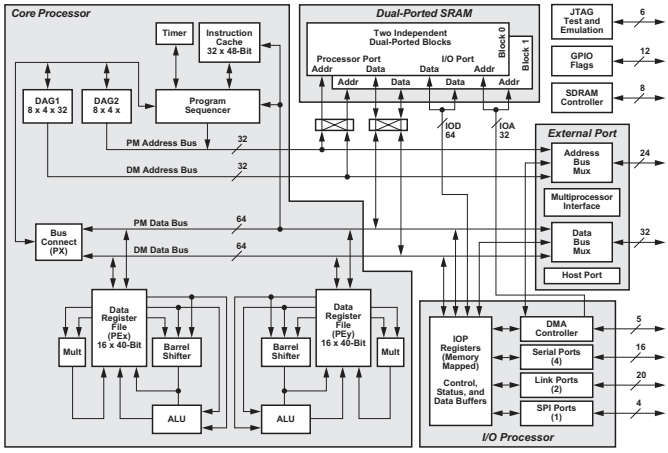
Development Tools	
ADDS-2116X-WKSHP	DSP Workshop
ADDS-21161N-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator

Benefits

- Two 100 Mbyte/S link ports simplify connection and communication in multiprocessing systems
- 14 zero-overhead DMA channels mean no cycles stolen from the core to move data on and off chip
- Cluster multiprocessing enables universally addressable memory system
- SDRAM controller for controlling large banks of DRAM
- 4 serial ports allow for 16 channels of data to be transferred in/out of the DSP

Applications

- High-end consumer audio
- Professional audio
- Automatic car systems
- Finger print recognition
- Medical equipment
- ADSL/cable test equipment
- Multi access motor control
- Voice recognition
- Global positioning
- Power line modems
- Telephony
- MP3 encoder
- Video phones
- Digital broadcast radio



ADSP-21160
Single-Instruction, Multiple-Data (SIMD) SHARC®

Features

- 540 MFLOPS (32-bit floating-point) peak operation
- 540 MOPS (32-bit fixed-point) peak operation
- 90 MHz core operation, 11 ns cycle time
- 92 µs 1024-point comlex FFT benchmark with bit reversal
- Code compatible with first generation SHARC
- SIMD core includes 2 multipliers, 2 ALUs, 2 shifters, and 2 register files
- 4 Mbits on-chip dual-ported SRAM
- Division of SRAM between program and data memory is selectable
- Core can fetch four 32-bit words from memory in a single processor cycle using two 64-bit wide buses
- Dual data address generators with modulo and bit-reverse addressing
- Efficient program sequencing with zero-overhead looping—single-cycle loop setup
- IEEE JTAG standard 1149.1 test access port and on-chip emulation
- 32-bit single-precision IEEE floating-point data type and 40-bit extended precision floating-point data type support
- 32-bit fixed-point formats, integer and fractional, with 80-bit accumulators in both processing elements
- 14 channels of zero-overhead DMA
- Glueless connection for scaleable DSP multiprocessing architectures
- Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-21160s plus host
- Six 100 Mbytes/sec link ports for point-to-point connectivity and array multi-processing
- 2.5 volt core, 3.3 volt I/O (80 MHz ADSP-21160M)
- 1.9 volt core, 3.3 volt I/O (95 MHz ADSP-21160N)

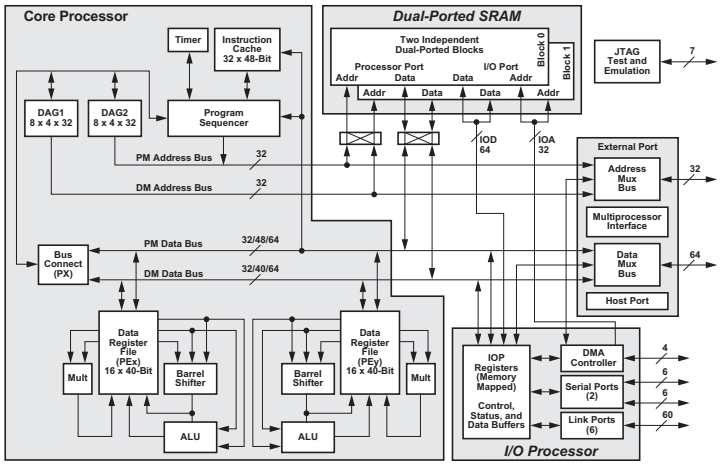
Applications

- Cellular base stations
- Call processing
- Speech recognition
- Instrumentation
- 3D graphics acceleration for workstations and arcade video games
- Imaging
- High-end audio
- Radar and sonar

Model	MHz	Pin/Pkg	Price* (1000)
ADSP-21160MKB-80	80	400-PBGA	$145.00
ADSP-21160NKB-95	95	400-PBGA	$145.00

M indicates 2.5V operation
N indicates 1.9V operation
K = Commercial Temp (0ºC to +85ºC case)
* All pricing is budgetary – subject to change

Development Tools	
ADDS-2116X-WKSHP	DSP Workshop
ADDS-21160-EZLITE	Evaluation Kit for “M”
ADDS-21160N-EZLITE	Evaluation Kit for “N”
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator



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ANALOG DEVICES

ADSP-21160 vs. TMS320C6x
Comparison

Features	TMS320C62x	TMS320C67x	ADSP-21160 SHARC
IEEE 32-bit floating-point support	No	Yes	Yes
Native 32-bit fixed-point support	No	No	Yes
Dual-ported internal memory	No	No	Yes
Built-in multiprocessing support	No	No	Cluster and link
Number of DMA channels	4	4	14
Zero-overhead DMA support[1]	No	No	Yes
Number of registers	32	32	128
Accumulator size	40 bits	40 bits	80 bits
64-bit product support	No	Yes	Yes
Memory bandwidth[2]	64 bits/cycle	128 bits/cycle	128 bits/cycle
Software loop support	No interrupts for compact loops	No interrupts for compact loops	Interrupts allowed in compact loops
Assembly complexity[3]	Highly complex	Highly complex	Algebraic assembly language
Number of circular buffers supported[4]	8	8	32
Conditional execution support	Requires extra register	Requires extra register	Dedicated conditional logic
FIR filter code size[5]	100 instructions	100 instructions	25 instructions
Package size	35mm, 352 ball	35mm, 352 ball	27mm, 400 ball

1 The TMS320C6x does DMA by stealing cycles from the core.
2 “Memory bandwidth” refers to the data path widths between the register file and memory.
3 Hand-optimized TMS320C6x assembly language must be written in a highly-complex, non-single assignment form.
4 The TMS320C6x only allows two different lengths of circular buffers and the lengths must be power of two.
5 TMS32062xx Programmer’s Guide page 4-112.

ADSP-21065L
Low-Cost Entry-Point to the SHARC® DSP Family

Features

- 16K 32-bit dual-ported on-chip memory (544 KBits configurable)
- 64M x 32-bit word external address space
- 198 MFLOPS (32-bit floating-point)
- 198 MOPS (32-bit fixed-point)
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I²S mode supports up to 16 channels
- 2 timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with 2 ADSP-21065L's
- Code compatible with all SHARC family members
- 3.3 volt, 208-pin MQFP, 196 MBGA

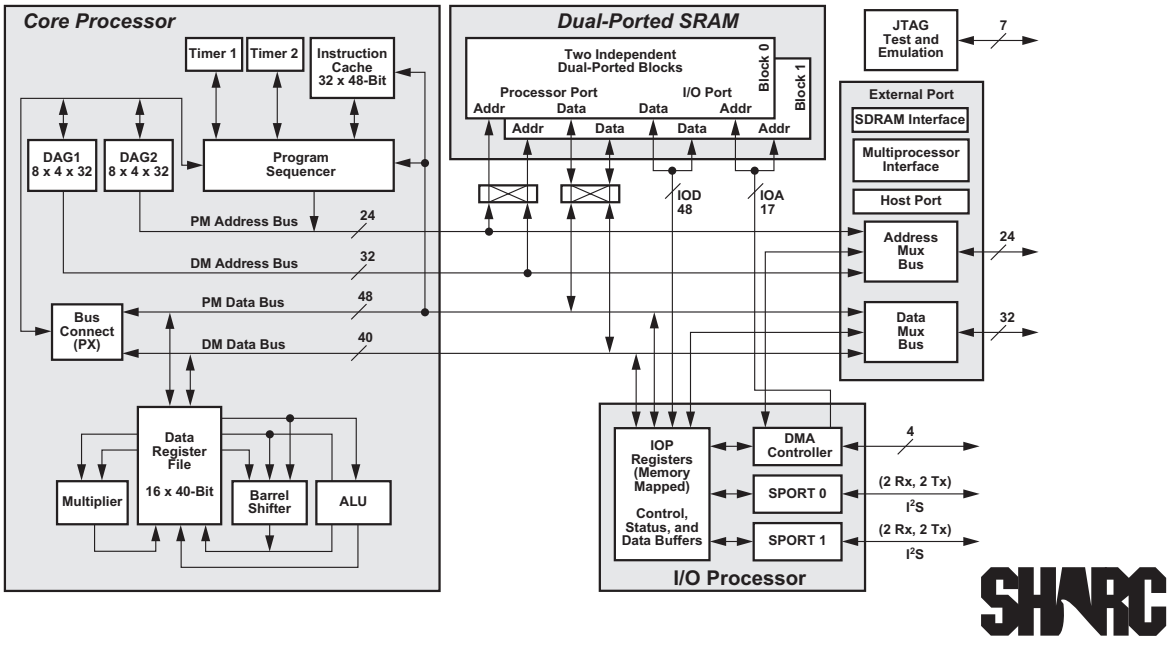
Applications

- Digital audio
- Keyless entry using voice analysis/recognition
- Bar code scanners
- Imaging
- Ultrasound equipment
- Digital oscilloscopes
- Fingerprint recognition

Model	MHz	Pin/Pkg	Price* (1000)
ADSP-21065LKS-240*	60	208-MQFP	$19.50
ADSP-21065LKS-264	66	208-MQFP	$37.50
ADSP-21065LKCA-240	60	196-MBGA	$38.00
ADSP-21065LKCA-264	66	196-MBGA	$39.50
ADSP-21065LCS-240	60	208-MQFP	$37.50

L Indicates 3.3 Volt Operation
K = Commercial Temp (0ºC to +85ºC case)
C = Industrial Temp (-40ºC to +100ºC case)
*All pricing is budgetary – subject to change

Development Tools	
ADDS-2106X-WKSHP	DSP Workshop
ADDS-21065L-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	VisualDSP++
VDSP-SHARC-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator



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ANALOG DEVICES

ADSP-2199x Family
Mixed Signal DSPs

The ADSP-2199x family of mixed-signal DSPs provides a single-chip high-performance solution with signal processing and mixed-signal integration for both current and future embedded control and signal processing applications. These products combine the ADSP-219x code-compatible DSP core, multichannel, high-resolution analog/ digital conversion, the right mix of embedded control peripherals, and comprehensive development tools. A variety of memory sizes address emerging market requirements with power efficient and high-performance solutions.

Development Tools

All ADSP-219x products, including the ADSP-2199x series are supported by ADI's CROSSCORE™ software and hardware development tools. The development tools suite includes the VisualDSP++™ integrated software development environment with the C/C++ compiler, VisualDSP++ Kernel (VDK), advanced plotting tools and statistical profiling to quickly identify bottlenecks and reduce development time. The tools suite also includes a low-cost EZ-KIT Lite™ evaluation platform. The EZ-KIT Lite can also be extended with JTAG In-circuit Emulation (ICE) for full control of software debugging. PCI and USB versions are of the emulator available.

Development Tools	
ADDS-21990-EZLITE	Evaluation Kit
VDSP-21XX-PC-FULL	VisualDSP++
VDSP-21XX-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator

Embedded Control applications support can be obtained at mcgapps@analog.com. Users can also obtain additional support, free software upgrades, and sample code by visiting the Motor Control Web site at www.analog.com/motorcontrol

Device	Package	Max MIPS	Program RAM Words	Data RAM Words	ADC	Status
ADSP-21990	ST, BC	160	4K	4K	14-Bit 20 MSPS	Samples Now Release 2Q02
ADSP-21991	ST, BC	160	32K	8K	14-Bit 20 MSPS	Samples 3Q02 Release 4Q02

Packages: ST = Thin Quad Flat Pack (LQFP)
BC = Mini Ball Grid Array (10 x 10 mm)

ADSP-21990
Mixed Signal DSP

Features

- 160 MHz, ADSP-219x DSP core
- 8-Channel, 14-Bit, 20 MSPS ADC
- On-chip voltage reference and power-on-reset
- 4K words program memory RAM
- 4K words data memory RAM
- External memory interface (to 1M Word)
- Embedded Control Peripherals
  - Three-phase PWM generation unit
  - Incremental encoder interface unit
  - Dual auxiliary PWM outputs
  - Watchdog timer
  - Three 32-Bit, general purpose timers
  - 16-Bit general purpose flag I/O port
  - Peripheral interrupt controller
  - Synchronous serial (SPORT) and SPI
  - Communications ports

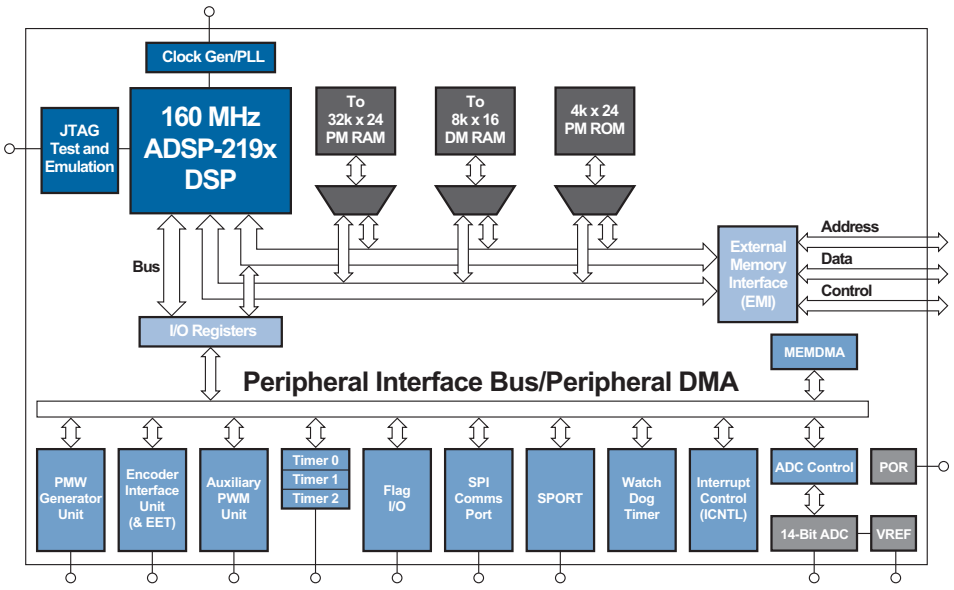
Applications

- Industrial motor drives
- Un-interruptible power supplies
- Optical networking control
- Data acquisition systems
- Test and measurement systems
- Portable Instrumentation
- Intelligent sensors
- Robotic control

Benefits

- ADSP-219x core delivers highest performance mixed-signal DSP for control designs with up to 160 MIPS sustained performance
- Code compatible solution ensures investment protection with lower software cost
- State-of-the-art development tools
- Integrated single-chip pin-compatible solutions facilitate high-performance design with higher reliability, reduces development time with lower overall system cost
- External memory interface provides direct access from DSP to external memory for data or instruction
- Fabricated in high-speed, low power consumption, CMOS process

Development Tools	
ADDS-21990-EZLITE	Evaluation Kit
VDSP-21XX-PC-FULL	VisualDSP++
VDSP-21XX-PCFLOAT	VisualDSP++ Floating License
ADDS-APEX-ICE	USB-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator



Device	Status	Package Description	Pin Count	Temperature Range
ADSP-21990BBC	Pre-Release	Ball Grid Array	196	Industrial
ADSP-21990BST	Pre-Release	Thin LQFP 1.4mm Thick	176	Industrial

http://www.analog.com/motorcontrol

ANALOG DEVICES

ADMC Embedded Control Family
Embedded DSP-Based Controllers

The ADMC family of embedded DSP-based Controllers integrate 16-bit, fixed-point DSPs with software and analog circuitry optimized for motor control applications. All processors are fully code compatible, allowing for additional features and enhanced performance, while protecting the software development investment.

Development Tools

Generic specific evaluation and development tools are available for each ADMCxxx device. Development tool kits include everything required to quickly and easily develop user specific applications including:

- VisualDSP++-based motion control debugger
- Connector board
- Compiler, linker, assembler
- Serial cable
- Example software
- User documentation and reference guides
- Modular processor board

Embedded Control applications support can be obtained at mcgapps@analog.com. Users can also obtain additional support, free software upgrades, and sample code by visiting the Motor Control Web site at: www.analog.com/motorcontrol

Embedded DSP Motor Control Selector Guide

Device	MIPS	Program RAM Words	Program FLASH	Program ROM Words	Data RAM Words	ADC	Embedded Control Peripherals	Package Options
ADMC401	26	2K		2K	1K	8 Channel 12-bit	• 3 Phase PWM • Aux PWM • Encoder Interface	144 Pin LQFP
ADMC341 ADMCF341 ADMC340 ADMCF340	20	512	4K (F34x)	4K (34x)	512	13 Channel 10-bit	• 3 Phase PWM • Aux PWM • 25 Digital I/O	64 Pin LQFP 28 Pin SOIC
ADMC328 ADMCF328 ADMC326 ADMCF326	20	512	4K (F32x)	4K (32x)	512	6 Channel 10-bit	• 3 Phase PWM • Aux PWM	28 Pin SOIC
ADMC331	26	2K		2K	1K	7 Channel 10-bit	• 3 Phase PWM • Aux PWM • 24 PIOS	80 Pin LQFP
ADMC300	25	4K		2K	1K	5 Channel 12-bit Sigma Delta	• 3 Phase PWM • Aux PWM • Encoder Interface	80 Pin LQFP

ADMCF34x/ADMC34x
Embedded DSP Controllers with Flash Memory

Features

- Integrated 10-bit ADC subsystem
  - 13 channels (F340/340)
  - 6 channels (F341/341)
  - Integrated current sense amplifiers
  - Internal voltage reference
- Three phase PWM generation
- Two auxiliary PWM outputs
- 20 MIPS fixed-point DSP core
  - 4K flash memory (ADMCF34x only)
  - 4K program memory ROM (ADMC34x only)
  - 512 program memory RAM
  - 512 data memory RAM
- Up to 24 digital I/O line
- Integrated power-on-reset function
- 28 pin SOIC and 64 QFP packages

Benefits

- ADC subsystems and peripherals tailored for specific motor types to simplify development
- 3 Sector on-chip Flash memory allows for in-circuit programming for software upgrade ability and rapid code development
- Integrated Power-On-Reset and precision volt age reference reduce system costs
- Pin for pin compatible ROM device provide low cost high volume option

Applications

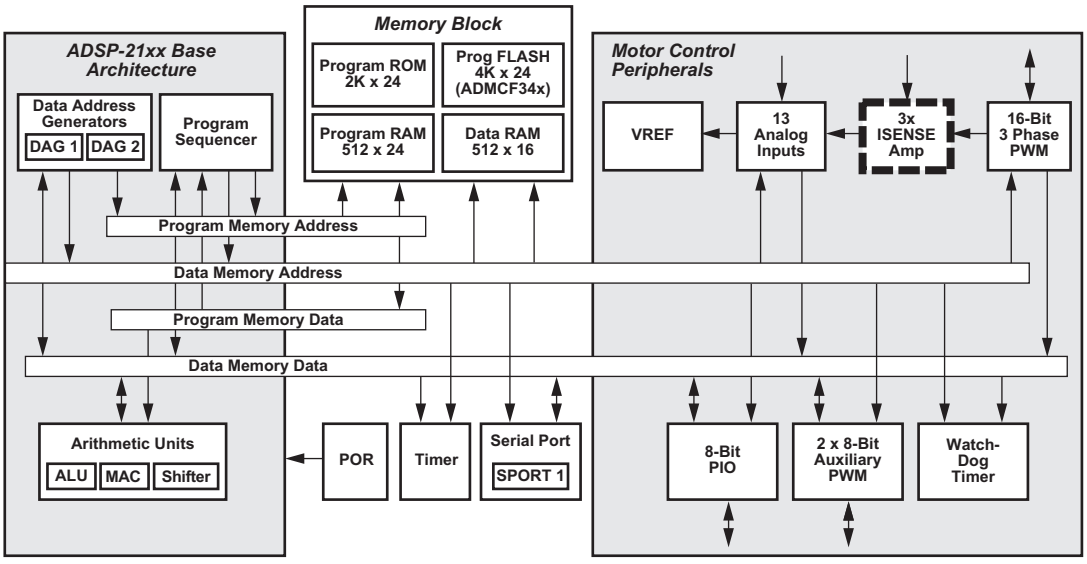
- Motor types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), Switched Reluctance Motors (SRM)
- Industrial variable speed and servo drives
- Uninterruptable power supplies
- Electric vehicles

Model	MHz	Pin/Pkg
ADMCF341BR	20	28 SOIC
ADMCF340BST	20	64 LQFP

B = Industrial Temp (-40ºC to +85ºC ambient)

* Each ROM order requires a 25,000-piece minimum order quantity and a $10,000 NRE charge

Development Tools	Price
ADMCF340-EVALKIT	$395.00
ADMCF341-EVALKIT	$395.00



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ANALOG DEVICES

ADMC401
Single-Chip, High Performance Embedded DSP Controller

Features

- High resolution integrated 12-bit multi-channel ADC (> 70 dB SNR)
  - 8 channel simultaneous sampling (8 channels converted in < 2µ sec)
  - Integrated precision voltage reference
- Three phase 16-bit PWM generation unit
- Two 8-bit auxiliary PWM outputs
- 26 MIPS fixed-point DSP core
  - 2K x 24-bit program memory RAM
  - 2K x 24-bit program memory ROM
  - 1K x 16-bit data memory RAM
  - 14-bit adress bus and 24-bit data bus for external memory expansion
- Incremental encoder interface
- Programmable digital I/O
- Integrated power-on-reset

Benefits

- High performance DSP integrated with fast 12-bit ADC provides for true single chip solution
- Fully code compatible with all ADSP-21xx and ADMCxx family products
- Algebraic assembly language for easy programming
- External address and data bus allows external memory to be added as needed
- Flexible encoder interface unit for position feedback
- Integrated power-on-reset function and voltage reference remove system cost

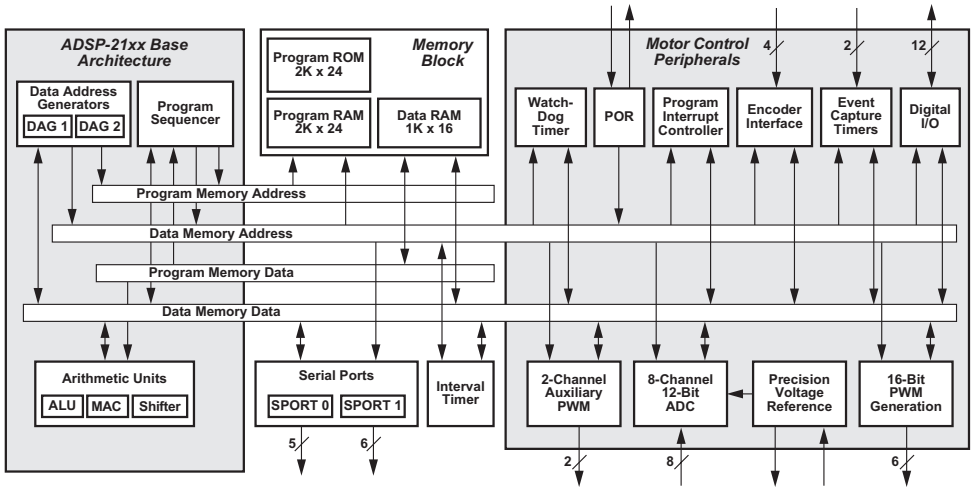
Applications

- Motor types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), Switched Reluctance Motors (SRM)
- Industrial variable speed and servo drives
- Uninterruptable power supplies
- Numerical control machines
- Robotics

Model	MHz	Pin/Pkg	Price* (100-499)
ADMC401BST	26	144 Pin LQFP	$24.95

B = Industrial Temp (-40ºC to +85ºC ambient)
* All pricing is budgetary – subject to change

Development Tools	Price
ADMC401-ADVEVALKIT	$395.00



Quad-SHARCs AD14060/AD14160
480-MFLOP, Single Package Multiprocessor

The **AD14060** Quad-SHARC is a first generation (CQFP) DSP multiprocessor. Using high-density packaging techniques, the module fits four SHARCs in approximately 30% of the space required using discrete packages.

The **AD14160** Quad-SHARC Ceramic Ball Grid Array (CBGA) puts the power of the first generation AD14060 (CQFP) DSP multiprocessor into a very high density ball grid array package, the module fits four SHARCs in approximately 30% of the space required using discrete packages; now with additional link and serial I/O pinned out, beyond that from the CQFP package.

The core of the multiprocessors is the ADSP-21060 DSP Microcomputer. The AD14060/ AD14160 modules have the highest performance-density and lowest cost-performance ratios of any multiprocessors in their class. They are ideal for applications requiring higher levels of performance and/or functionality per unit area.

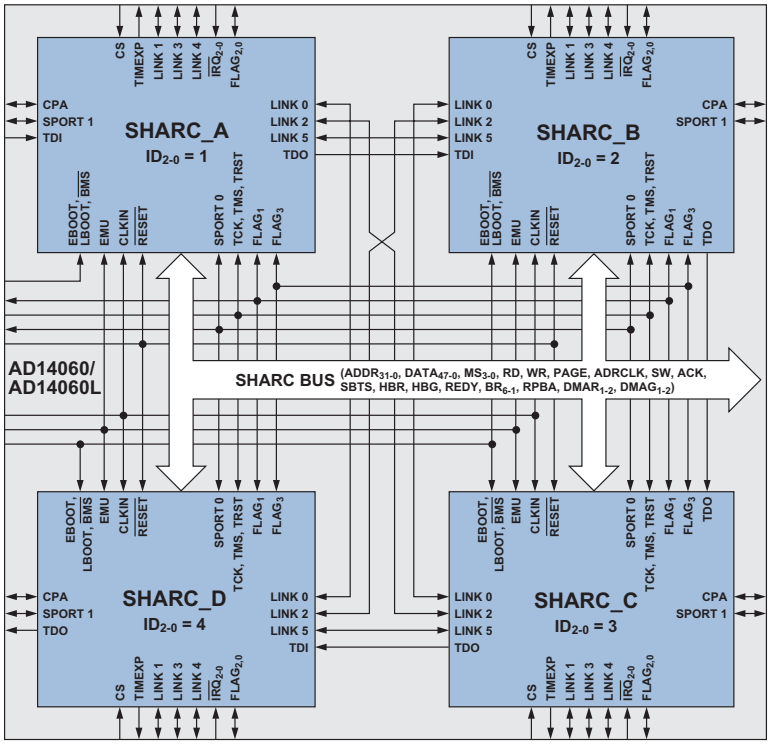
The AD14060/AD14160 take advantage of the built-in multiprocessing features of the ADSP-21060, to achieve 480 peak MFLOPS with a single chip type, in a single package. The on-chip SRAM of the DSPs provides 16 Mbits of on-module shared SRAM. The complete shared bus (48-bit data, 32-address) is also brought off-module for interfacing with expansion memory and/or other peripherals.

Applications

Multi-SHARC designs with tight area/volume constraints, such as large array and image processors, smart missiles, avionics, and others will benefit. The AD14060/AD14160 are available as both industrial and MIL-SMD grade parts in 5V (AD14060/AD14160) or 3.3V (AD14060L/AD14160L) versions.

Competition

With 480 MFLOPS of throughput, the AD14060/AD14160 have no competition. TI's Dual C40 MCM provides a similar function, but delivers only 80 MFLOPS in a significantly larger package, and roughly equivalent cost. The Quad-SHARC AD14060/AD14160 is targeted to be priced such that users can take advantage of system cost advantages of using MCMs.



AD14060 Functional Block Diagram

http://www.analog.com/milsystems

ANALOG DEVICES

Quad-SHARCs AD14060/AD14160

Development Tools

Both the AD14060 and AD14160 are supported with a complete set of software and hardware development tools, including an ADSP-21061 EZ-KIT Lite, and development software.

Features

- ADSP-21060 core processor (. . . x4)
- 480 MFLOPS Peak, 320 MFLOPS sustained
- 25 ns instruction rate, single-cycle instruction execution - each of 4 processors
- 16 Mbit shared SRAM (internal to SHARC's)
- 4 gigawords addressable off - module memory
- 48-bit shared memory bus, 48-bit data bus
- Full 32-bit address bus
- Interrupts, flag pins, and timers are also avail able as I/O
- 32-Bit single precision and 40-Bit extended precision IEEE floating-point data formats, or 32-Bit fixed-point data format
- User configurable boot modes, bus priority, and other features with control lines
- IEEE JTAG standard 1149.1 test access port and on-chip emulation

AD14060

– Twelve 40 Mbyte/s link ports (3 per SHARC) accessible to/from the outside world
– Four link ports connected internally in a ring configuration
– Four 40 Mbit/s independent serial ports (one from each SHARC)
– One 40 Mbit/s common serial port
– Ceramic quad flat pack with enhanced I/O
– Low-profile 2.05" 308 lead ceramic quad flat pack package

AD14160

– Sixteen 40 Mbyte/s link ports (per SHARC) accessible to/from the outside world
– Eight link ports connected internally in ring configuration
– Eight 40 Mbit/s independent serial ports (two from each SHARC) available from outside
– Ceramic ball grid array QUAD-SHARC with enhanced I/O
– Low-profile 1.85" ceramic ball grid array package

For any further inquiries, please contact MCP Marketing in Greensboro, NC at 336-668-9511

http://www.analog.com/milsystems

Software and Systems Technologies (SST)

Marketplace pressures of the newest technologies, faster time to market, and ever-lower systems costs drive leading OEMs to look for the newest, fastest ways to introduce their products to their customers.

To meet this need, Analog Devices Inc. offers numerous chipset and algorithm reference designs and third party support in emerging and high growth market segments.

SST-Melody-32
For High Volume Multi-Channel Digital Audio Processing

Features

- 32-bit implementation of industry standard audio formats on new DSP platform
- Decodes up to 8 channels of multiplexed audio: scaleable between 1 and 8 channels, with 6.1 core channels and 2 extended channels
- Sufficient computing power for custom OEM applications such as speaker equalizers and surround fields

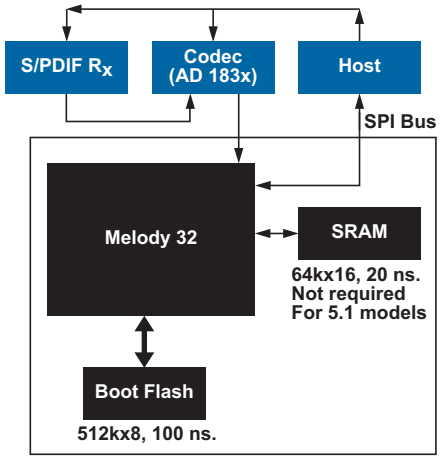
Benefits

- Melody 32 offers end-to-end 32-bit precision of decode & post-processing for leading digital audio formats in real-time.
- The Melody reference design decodes up to 7.1 channels of DTS ES Extended Surround, Dolby Digital, Dolby Pro Logic II, AAC, MP3, and includes THX Surround EX, Bass Management, Delay Management, and automatic detection of the incoming audio bit-stream.
- Decoder supports all bit rates (up to 1,536 kbps), compression ratios (up to 40:1) and sampling frequencies (32, 44.1, and 48 kHz per channel) specified by the DTS (Digital Theater Systems) and Dolby audio standards. It also supports fea tures specified by the DTS standard -- including Dynamic Range Control, Down-Mixing, and Re-equalization of all channels independently.

Applications

- Home theater AVR systems
- Automotive audio
- DVD players
- Video game consoles
- Set Top boxes

Reference Block Diagram



Chipsets

ADSST-MEL-20: Bundled chipset that includes the high performance of the ADSST-MEL322 processor with a high performance audio codec. It includes decoding / post processing for Dolby Digital EX, Dolby Pro Logic II, AAC (LC), DTS ES (Discrete and Matrix), DTS Neo:6.

ADSST-MEL-30: Includes decoding / post process-ing for Dolby Digital EX, Dolby Pro Logic II, DTS ES (Discrete and Matrix), DTS Neo:6, THX EX, SRS Circle Surround II, TruBass codes. The chipset includes ADI Surround modes, Speaker EQ as well as Bass Management and Delay.

ADSST-MEL-40: Features of the ADSST-MEL-30 but without THX processing.

ADSST-MEL-50: Includes decoding / post process-ing for Dolby Digital EX, Dolby Pro Logic II, DTS ES (Discrete and Matrix), DTS Neo:6 and SRS Circle Surround II codes. The chipset includes Wavesurround Headphone and Loudspeaker Virtualizer modes, Bass Management and Delay.

SST-Melody-SU
Highest Performance Multi-Channel Audio Processing

Features

- 32-Bit floating-point implementation for decoding the leading encoded audio content .
- Decoders operate in real-time with the ability to auto-detect and display bit stream information
- Decoders support all of the bit rates (up to 6,144 kbps) and sampling frequencies (32, 44.1, 48, 88.2, 96 and 192 kHz per channel) specified by the encoding standards

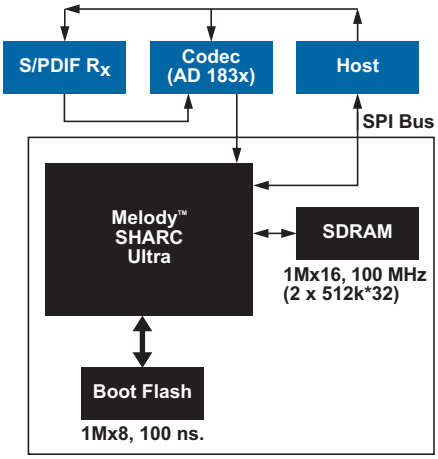
Benefits

- This enables OEMs to produce high-quality, low-cost designs featuring decoder algorithms and post processors for :
  - DTS-ES Extended Surround (including both DTS ES Discrete 6.1 and DTS ES Matrix 6.1)
  - DTS 96/24
  - DTS Neo:6
  - Dolby Digital, Dolby Pro Logic II, Dolby Headphone
  - THX, THX Surround EX, THX Ultra2
  - HDCD
  - MPEG1 Audio Layer III (also known as MP3)
  - MPEG AAC (both MP and LC versions)
  - SRS Circle Surround II, SRS 3D Sound, SRS TruSurround, SRS Focus and SRS TruBass
  - MLP

Applications

- Multi-channel audio decoders and post-processors for digital audio designs using DSPs (Digital Signal Processors) in home theater
- Automotive audio receivers
- DVD players

Reference Block Diagram



Models

Model ADSST-AUDIO-7060: is a twin combination chipset and includes decoding/post-processing for Dolby Digital, Dolby Pro Logic II, DTS, THX, DTS ES-Matrix, Bass Management and Delay.

Model ADSST-AUDIO-7070: Includes Dolby Digital and Dolby Pro Logic codes.

Model ADSST-AUDIO-7075: includes Dolby Digital, Dolby Pro Logic and DTS 5.1 codes.

Model ADSST-AUDIO-7085: Includes Dolby Digital, Dolby Pro Logic II, DTS ES, DTS 6.1, DTS 96/24, DTS Neo:6, AAC LC and MP, THX Ultra2, Bass Management and Delay Management.

Model ADSST-AUDIO-7090: Includes Dolby Digital, DTS ES, DTS 6.1, DTS 96/24, MPEG2 BC, MPEG2 AAC LC and MP, Dolby Pro Logic II, DTS Neo:6.

Model ADSST-AUDIO 7095: Includes Dolby EX, DTS ES Matrix, Bass Management, THX Ultra2, Delay Management and Dolby Headphone.

SST-NAV-GPS
NAV2400 Global Positioning Satellite Receiver Chipset

Features

- L1 band GPS standard positioning service
- Twelve parallel channels
- Computes user's position and velocity and time
- Efficient algorithms for very low time to first fix even without almanac
- Soft solution approach for correlation
- TTL output through serial link
- NMEA0183 compatible message format for host communication
- Real time executive based software architecture
- Differential GPS compatibility
- Power down features for extremely low power operation

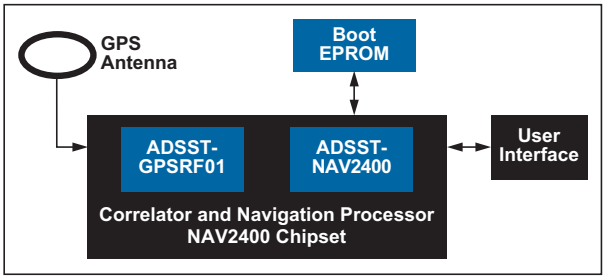
Benefits

- NAV2400 with its spare processing power becomes an ideal building block for a variety of OEM applications. This approach minimizes the additional processing hardware requirements for integrated GPS based OEM applications resulting in a cost-effective end product.

Applications

- Car telematics
- Fleet management
- Asset management
- Recreational tracking
- Navigation

Reference Block Diagram



GPS receiver based on NAV2400 chipset

Models

Model ADSST-NAV2400: Includes ADSST-GPSRF01 RF Front End and ADSST-NAV2400 Correlation and Navigation Processor to form a GPS receiver.

Model ADSST-NAV24-SDK: Includes NAV2400 chipset as part of a software development kit and evaluation platform.

http://www.analog.com/solutions

http://www.analog.com/milsystems

dspConverter™
Integrated DSP and Data Converter for Voice

ADI's dspConverters feature our industry leading data converters, 16-bit fixed-point DSPs and flash memory all packed into one small (14 mm x 22 mm) BGA package.

The analog front ends are based on our AD733xx family which include 16-bit linear codecs, input/output conditioning circuitry and a flexible serial interface. The DSPs are based on the ADSP-218x family.

Analog Front Ends (AFEs)

The analog front ends are much more than codecs. Each channel includes:

- Sigma-delta DAC
- Sigma-delta ADC
- PGA for each encoder and decoder
- Input conditioning circuitry
- Reference
- SPORT

No Digital Feedthrough Problems

One of the critical aspects of mixed-signal design is digital feedthrough from high-speed processors to high-resolution analog circuitry. This is fully addressed in our dspConverters with careful circuit layout and synchronization of clocks. Test results have verified that clock noise is absent from the digitized analog spectrum even when the DSP is running at full speed.

Converter Performance and Group Delay

The converters are fully specified with SNR+THD figures of 78 dB for the encoders and 77 dB for the decoders. A notable feature of the performance specification is it's clarity.

Group delay can be critical in noise cancellation applications. It's important to cancel the noise as close to the source as possible. Delays increase modeling errors, require larger filters and inhibit random noise cancellation systems. All analog front ends in the family offer group delays, which are 25 µs for the encoder and 50 µs for the decoder.

dspConverter Selection Table

Generic	AFE Channels	DSP	Program Memory	Data Memory	Price*
AD73411-40	1	52 MIPS	8K	8K	$17.65
AD73411-80	1	52 MIPS	16K	16K	$21.18
AD73422-40	2	52 MIPS	8K	8K	$20.41
AD73422-80	2	52 MIPS	16K	16K	$23.47
AD73460-80	6-Ch ADC	52 MIPS	16K	16K	$23.47

* US Dollars. Lowest grade suggested resale price per unit in 100 unit quantities
All pricing is budgetary – subject to change

AD73411
Low Power Analog Front End with DSP

Features

AFE PERFORMANCE
- 16-Bit A/D converter
- 16-Bit D/A converter
- Programmable input/output sample rates
- 76 dB ADC SNR
- 77 dB DAC SNR
- 64 kS/s maximum sample rate
- –90 dB crosstalk
- Low group delay (25 µs typ per ADC channel, 50 µs typ per DAC channel)
- Programmable input/output gain
- On-chip reference

DSP PERFORMANCE
- 19 ns instruction cycle time @ 3.3 Volts, 52 MIPS performance
- Single-cycle instruction execution
- Single-cycle context switch
- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Power-down mode featuring low CMOS standby
- Power dissipation with 400 cycle recovery from power-down condition
- Low power dissipation in idle mode

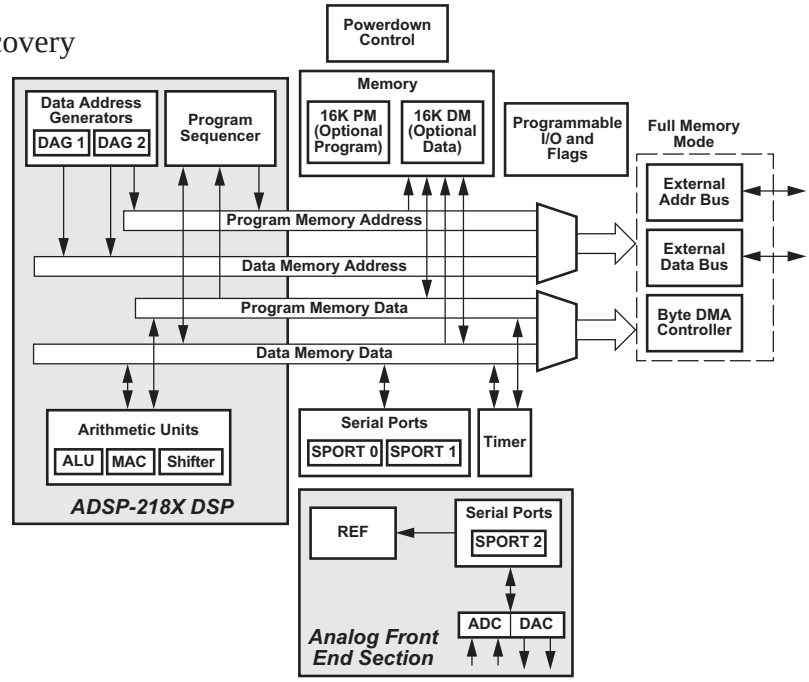
Benefits

- Extensive analog front ends include A/Ds, D/A, PGAs, reference and input conditioning circuitry
- Reduced design risk – all the interface design work is done
- Programmable, high-speed DSP based on ADSP-218x Family

Applications

- General purpose analog I/O
- Speech processing
- Cordless and personal communications
- Telephony
- Wireless local loop
- Active control of sound and vibration
- Data communications

Model	AFE CHNS	Prog Data Memory	Pin/Pkg
AD73411-40	1	8/8K	119 PBGA
AD73411-80	1	16/16K	119 PBGA



AD73422
Dual Low Power Analog Front End with DSP

Features

AFE PERFORMANCE
- 16-Bit A/D converter
- 16-Bit D/A converter
- Programmable input/output sample rates
- 76 dB ADC SNR
- 77 dB DAC SNR
- 64 kS/s maximum sample rate
- –90 dB crosstalk
- Low group delay (25 µs typ per ADC channel, 50 µs typ per DAC channel)
- Programmable input/output gain
- On-chip reference

DSP PERFORMANCE
- 19 ns instruction cycle time @ 3.3 Volts, 52 MIPS performance
- Single-cycle instruction execution
- Single-cycle context switch
- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Power-down mode featuring low CMOS standby
- Power dissipation with 400 cycle recovery from power-down condition
- Low power dissipation in idle mode

http://www.analog.com/dspconverter

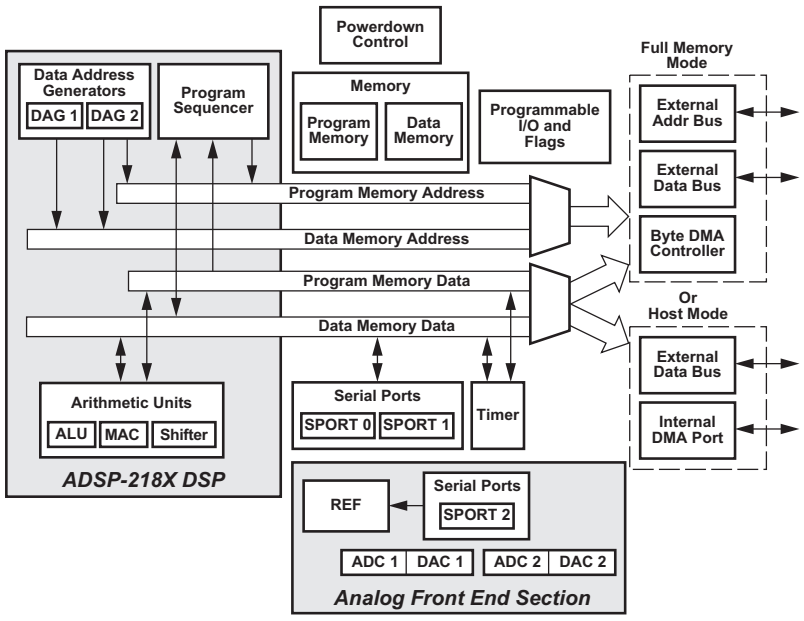
Benefits

- Extensive analog front ends include A/Ds, D/A, PGAs, reference and input conditioning circuitry
- Reduced design risk – all the interface design work is done
- Programmable, high-speed DSP based on ADSP-218x Family

Applications

- General purpose analog I/O
- Speech processing
- Cordless and personal communications
- Telephony
- Wireless local loop
- Active control of sound and vibration
- Data communications

Model	AFE CHNS	Prog Data Memory	Pin/Pkg
AD73422-40	2	8/8K	119 PBGA
AD73422-80	2	16/16K	119 PBGA



AD73460
Low Power, Six-Channel ADC with DSP

Features

AFE PERFORMANCE
- Six 16-Bit A/D converters
- Programmable input sample rate
- 72 dB ADC SNR
- 64 kS/s maximum sample rate
- –80 dB crosstalk
- Low group delay (25 µs typ per ADC channel)
- Programmable input gain
- Single supply operation
- On-chip reference

DSP PERFORMANCE
- 19 ns instruction cycle time @ 3.3 Volts, 52 MIPS sustained performance
- Single-cycle instruction execution
- Single-cycle context switch
- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Power-down mode featuring low CMOS standby
- Power dissipation with 400 cycle recovery from power-down condition
- Low power dissipation in idle mode

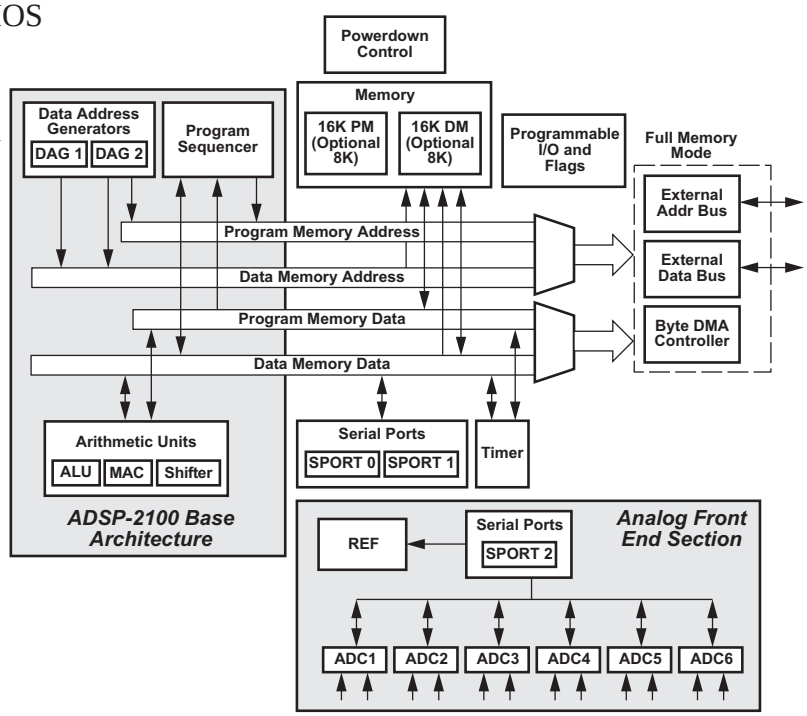
Benefits

- Extensive analog front ends include A/Ds, D/As, PGAs, reference and input conditioning circuitry
- Reduced design risk – all the interface design work is done
- Programmable, high-speed DSP based on ADSP-218x Family

Applications

- General purpose I/O
- Industrial metering
- Active control of sound and vibration
- Speech processing
- Data communications

Model	AFE CHNS	Prog Data Memory	Pin/Pkg
AD73460BB-40	6	8/8K	119 PBGA
AD73460BB-80	6	16/16K	119 PBGA



ADI Support for Universities

The ADI DSP University Program provides the next generation of engineers with DSP knowledge to help them compete in the industry of tomorrow.

The ADI DSP University Program offers:

- Complete DSP Software and Hardware Tools to set up a DSP LAB
- Teaching material to help design experiments
- Priority technical support to professors

Analog Devices DSP technology is easy to teach:

- DSP architectures that are the simplest to program in the industry
- Simple instruction sets
- High levels of SRAM integration

Hundreds of universities in 37 countries use ADI DSPs for teaching and research.

To request a University discount or learn more, go to:

http://www.analog.com/dsp/university

DSP Literature Selection Guide

Title	Where to Order	Publication Number	Price
ADSP-21xx Development Board and Emulator Publications			
ADSP-218x DSP family and ADSP-2192 EZ-KIT Lite Installation Procedure	www.analog.com/dsp		NC
ADSP-2191 EZ-KIT Lite Manual	www.analog.com/dsp		NC
ADSP-2192-12 EZ-KIT Lite Manual	www.analog.com/dsp		NC
ADSP-2181 EZ-KIT Lite Evaluation Manual	www.analog.com/dsp		NC
ADSP-2189M EZ-KIT Lite Evaluation System Manual	www.analog.com/dsp		NC
ADSP-218X Family EZ-ICE® Hardware Installation Guide	www.analog.com/dsp		NC
Summit-ICE™ Emulator Hardware User's Guide	www.analog.com/dsp		NC
Apex-ICE™ USB Emulator Hardware Installation Guide	www.analog.com/dsp		NC
VisualDSP++ for the ADSP-21xx			
Complete Set of ADSP-21xx VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-21XX-MAN-FULL	$100.00
VisualDSP++ Getting Started Guide for ADSP-21xx DSPs	www.analog.com/dsp		NC
VisualDSP++ User's Guide for ADSP-21xx DSPs	www.analog.com/dsp		NC
VisualDSP++ C Compiler and Library Manual for ADSP-218x DSPs	www.analog.com/dsp		NC
VisualDSP++ C/C++ Compiler and Library Manual for ADSP-219x DSPs	www.analog.com/dsp		NC
VisualDSP++ Assembler and Preprocessor Manual for ADSP-218x DSPs	www.analog.com/dsp		NC
VisualDSP++ Assembler and Preprocessor Manual for ADSP-219x DSPs	www.analog.com/dsp		NC
VisualDSP++ Linker and Utilities Manual for ADSP-21xx DSPs	www.analog.com/dsp		NC
VisualDSP++ Kernel (VDK) User's Guide VisualDSP++ Installation Guide	www.analog.com/dsp		NC
VisualDSP++ for Blackfin DSPs			
Complete Set of ADSP-21xx VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-BLKFN-MAN-FUL	$100.00
VisualDSP++ Getting Started Guide for Blackfin DSPs	www.analog.com/dsp		NC
VisualDSP++ User's Guide for Blackfin DSPs	www.analog.com/dsp		NC
VisualDSP++ C/C++ Compiler and Library Manual for Blackfin DSPs	www.analog.com/dsp		NC
VisualDSP++ Assembler and Preprocessor Manual for Blackfin DSPs	www.analog.com/dsp		NC
VisualDSP++ Linker and Utilities Manual for Blackfin DSPs	www.analog.com/dsp		NC
VisualDSP++ Kernel (VDK) User's Guide (Second Revision	www.analog.com/dsp		NC
VisualDSP++ Installation Guide	www.analog.com/dsp		NC
ADSP-21xx Publications			
ADSP-2100 Family User's Manual	Lit Center	82-000780-03	NC
ADSP-218x DSP Hardware Reference Manual	Lit Center	82-002010-01	NC
ADSP-218x DSP Instruction Set Reference	Lit Center	82-002000-01	NC
ADSP-219x/2191 DSP Hardware Reference Manual	Lit Center	82-000390-06	NC
ADSP-219x/2192 DSP Hardware Reference Manual	Lit Center	82-002001-01	NC
ADSP-219x DSP Instruction Set Reference	Lit Center	82-000390-07	NC
ADSP-21xx Data Sheets			
ADSP-2181	www.analog.com/dsp		NC
ADSP-2183	www.analog.com/dsp		NC
ADSP-2185M	www.analog.com/dsp		NC
ADSP-2186M	www.analog.com/dsp		NC
ADSP-2188M	www.analog.com/dsp		NC
ADSP-2189M	www.analog.com/dsp		NC
ADSP-218xN Series	www.analog.com/dsp		NC
ADSP-2191M	www.analog.com/dsp		NC
ADSP-2192	www.analog.com/dsp		NC
Blackfin DSP Publications			
ADSP-21535 Blackfin DSP Hardware Reference, Preliminary Edition	www.analog.com/dsp	Preliminary	NC
Blackfin DSP Instruction Set Reference, Preliminary Edition	www.analog.com/dsp	Preliminary	NC
Blackfin DSP Data Sheets			
ADSP-21532	www.analog.com/dsp	Preliminary	NC
ADSP-21535	www.analog.com/dsp	Preliminary	NC

DSP Literature Selection Guide

Title	Where to Order	Publication Number	Price
SHARC DSP Development Board and Emulator Publications			
ADSP-21061 EZ-KIT Lite Manual	www.analog.com/dsp		NC
ADSP-21065L EZ-KIT Lite Manual	www.analog.com/dsp		NC
ADSP-21161N EZ-KIT Lite Manual	www.analog.com/dsp		NC
Apex-ICE™ USB Emulator Hardware Installation Guide	www.analog.com/dsp		NC
Summit-ICE™ Emulator Hardware User's Guide	www.analog.com/dsp		NC
VisualDSP++ for SHARC DSPs			
Complete Set of SHARC VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-SHARC-MAN-FUL	$100.00
VisualDSP++ Getting Started Guide	www.analog.com/dsp		NC
VisualDSP++ User's Guide for the ADSP-21xxx Family DSPs	www.analog.com/dsp		NC
Assembler and Preprocessor Manual for the ADSP-21xxx Family DSPs	www.analog.com/dsp		NC
C/C++ Compiler & Library Manual for the ADSP-21xxx Family DSPs	www.analog.com/dsp		NC
Linker & Utilities Manual for the ADSP-21xxx Family DSPs	www.analog.com/dsp		NC
VisualDSP++ Kernel (VDK) User's Guide	www.analog.com/dsp		NC
VisualDSP++ Installation Guide	www.analog.com/dsp		NC
VisualDSP++ for TigerSHARC DSPs			
Complete Set of TigerSHARC VisualDSP++ Manuals - includes the following:	From ADI Sales and Dist.	VDSP-TS-MAN-FULL	$100.00
VisualDSP++ User's Guide for TigerSHARC DSPs	www.analog.com/dsp		NC
VisualDSP++ Assembler and Preprocessor Manual for TigerSHARC DSPs	www.analog.com/dsp		NC
VisualDSP++ C/C++ Compiler and Library Manual for TigerSHARC DSPs	www.analog.com/dsp		NC
VisualDSP++ Linker and Utilities Manual for TigerSHARC DSPs	www.analog.com/dsp		NC
VisualDSP++ Kernel (VDK) User's Guide	www.analog.com/dsp		NC
VisualDSP++ Installation Guide	www.analog.com/dsp		NC
SHARC DSP and TigerSHARC DSP Publications			
ADSP-2106x SHARC Family User's Manual, 2nd Edition	Lit Center	E2003a-16-5/97	NC
ADSP-21065L User's Manual & Technical Reference	Lit Center	82-001833-01	NC
ADSP-21160 SHARC Hardware Reference	Lit Center	82-001966-01	NC
ADSP-21160 SHARC Instruction Set Reference	Lit Center	82-001967-01	NC
ADSP-21161 SHARC Hardware Reference	Lit Center	82-001944-01	NC
ADSP-21000 Family Applications Handbook	www.analog.com/dsp		NC
TigerSHARC ADSP-TS101S Hardware Specification Rev 1.01, July 2001	www.analog.com/dsp		NC
TigerSHARC Instruction Specification ADSP-TS101S Revision 1.0, July 2001	www.analog.com/dsp		NC
SHARC DSP and TigerSHARC DSP Data Sheets			
ADSP-21060/ADSP-21060L	www.analog.com/dsp		NC
ADSP-21061/ADSP-21061L	www.analog.com/dsp		NC
ADSP-21062/ADSP-21062L	www.analog.com/dsp		NC
ADSP-21065L	www.analog.com/dsp		NC
ADSP-21060C/ADSP-21060LC	www.analog.com/dsp		NC
ADSP-21160M	www.analog.com/dsp		NC
ADSP-21160N	www.analog.com/dsp		NC
ADSP-21161N	www.analog.com/dsp		NC
ADSP-TS101S	www.analog.com/dsp		NC

* NC = No charge

** Data Sheets and Manuals can also be downloaded from the ADI DSP website

http://www.analog.com/dsp/tech_doc

DSP Technical Training Workshops

Description

The DSP System Development and Programming workshops are comprehensive, hands-on workshops. The workshops are geared towards people who have a working knowledge of microprocessors and want to learn how to use Analog Devices DSPs. These courses cover the DSP architecture, assembly language syntax, I/O interface, hardware and software development tools. Throughout the workshop, attendees learn how easy it is to use Analog Devices' DSPs from lecture sessions and hands-on exercises.

Locations and Schedules

The workshops are offered monthly in North America. Workshop schedules and more details on DSP workshops are also available on the web site.

http://www.analog.com/dsp/training

How to Register

To enroll, customers should register online at the Analog Devices web site at:
http://www.analog.com/dsp/training
You will be notified when your seat is confirmed.

ADSP-218x Workshop

This is a 3-day workshop which covers the ADSP-218x family of DSPs and development tools. For registration and price, contact Momentum Data Systems via e-mail at sales@mds.com, or by phone at 714-378-5805.

Part Number: ADDS-218X-WKSP Price: Contact Momentum

ADSP-2106x Workshop

This is a 3.5 day workshop which covers all the ADSP-2106x DSPs including the ADSP-21065L and development tools. For registration and price, contact Melinda Rosauro at bEST Inc, at MRosauro@bbd.ca or 905-821-7800 X3330.

Part Number: ADDS-2106X-WKSP Price: Contact bEST

ADSP-2116x Workshop

This is a 3.5 day workshop which covers ADSP-21160 and development tools. For registration and price, contact Melinda Rosauro at bEST Inc, at MRosauro@bbd.ca or 905-821-7800 X3330.

Part Number: ADDS-2116X-WKSP Price: Contact bEST

ADSP-219x Workshop

This is a 3.5 day workshop which covers the ADSP-219x family of DSPs and development tools. For registration and price, contact Melinda Rosauro at bEST Inc, at MRosauro@bbd.ca or 905-821-7800 X3330.

Part Number: ADDS-219X-WKSP Price: Contact bEST

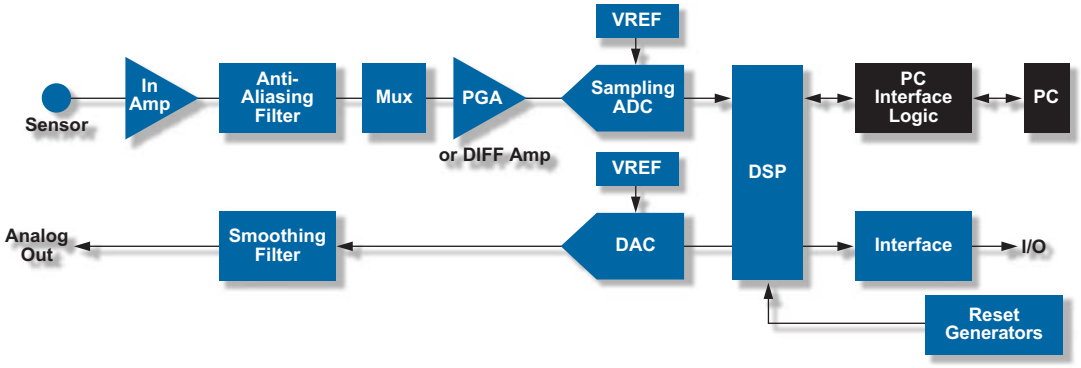
* Analog Devices also offers workshops in France, Germany, Italy, Scandinavia, UK, and Spain. The schedule of classes can be viewed online at **http://www.analog.com/technology/dsp/training/events/schedule.html**

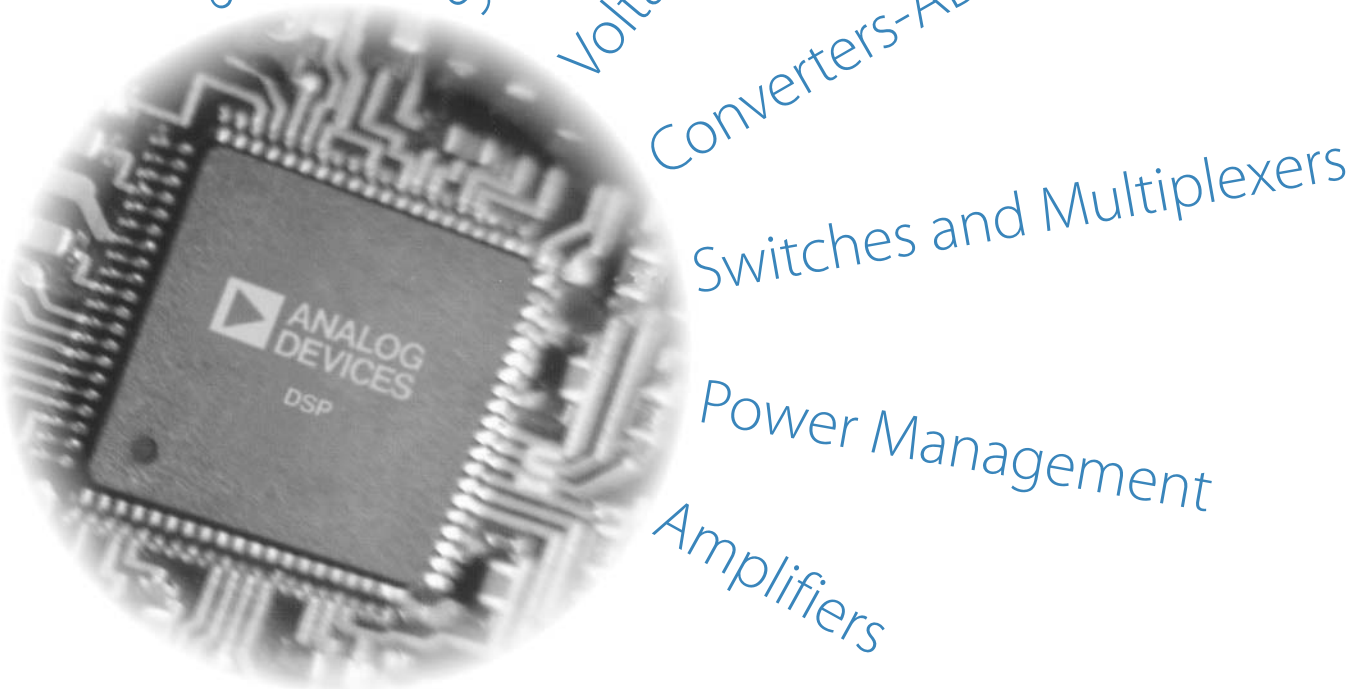
ADI DSP-Power Management Guide

ADSP-21xx Platform			Recommended ADI Power Management Devices for Maximum DSP Core and I/O Currents			
			1 DSP		2 or More DSPs	
DSP Family	DSP Supply Voltage (nominal)	Max Supply Current	LDO	DC/DC Switching Regulator or Controller	LDO	DC/DC Switching Regulator or Controller
	1.8V core	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2184N	3.3V I/O	14 mA	ADP3309	ADP3088	ADP3309	ADP3088
	2.5V core	38 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2185M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8V core	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2185N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	38 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2186M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2186N	3.3V I/O	14 mA	ADP3330	ADP3088	ADP3309	ADP3088
	1.8Vcore	26 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2187N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	44 mA	ADP3309	ADP3088	ADP3309	ADP3088
ADSP-2188M	3.3V I/O	12 mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	25 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2188N	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5Vcore	32 mA	ADP3309	ADP3088	ADP3331	ADP3088
ADSP-2189M	3.3V I/O	15mA	ADP3300	ADP3088	ADP3309	ADP3088
	1.8Vcore	26 mA	ADP3331	ADP3088	ADP3331	ADP3088
ADSP-2189N	3.3V I/O	14 mA	ADP3330	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2191M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2195M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
	2.5V core	184 mA	ADP3330	ADP3088	ADP3335	ADP3088
ADSP-2196M	3.3V I/O	14 mA	ADP3300	ADP3088	ADP3309	ADP3088
ADSP-21xxx SHARC Platform						
	3.3Vcore	275 mA	ADP3333	ADP3088	ADP3338	ADP3088
ADSP-21065L	3.3V I/O	21 mA	ADP3309	ADP3088	ADP3309	ADP3088
	2.5Vcore	875 mA	ADP3338/9	ADP3088	-	-
ADSP-21160M	3.3V I/O	41 mA	ADP3309	ADP3088	ADP3309	ADP3088
	1.8V core	875 mA	ADP3338/9	ADP3088	-	-
ADSP-21160N	3.3V I/O	72 mA	ADP3309	ADP3088	ADP3330	ADP3088
	1.8V core	550 mA	ADP3338	ADP3088	-	ADP3050
ADSP-21161N	3.3V I/O	56 mA	ADP3309	ADP3088	ADP3330	ADP3088

Remember …

Analog Devices Offers Products and Solutions for the Entire Signal Chain





…and much, much more

http://www.analog.com

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