BY IAN DENNIS • PRISM SOUND GROUP

Audio-converter-subsystem design challenges in the 21st century

SOME KEY STRATEGIES ENABLE YOU TO ACHIEVE OPTIMUM AUDIO-CONVERTER PERFORMANCE.

The habitat of audio converters is ever-changing. Designers built early converters into stand-alone digital-audio equipment. Later, they built them as stand-alone conversion devices with dedicated digital-audio connectivity. Nowadays, converters are increasingly available as peripherals for PCs or computer networks. Meanwhile, performance targets have been rising. In some ways, these changes have affected audio-converter design; in other ways, it's business as usual.

It seems that the plan of campaign for most engineers setting out to design an audio-converter subsystem—that is, a stand-alone converter or that part of the equipment that deals with audio conversion—is as follows: First, choose a data-converter device—an ADC, a DAC, or a codec chip—which will meet the project's requirements for performance, channel count, cost, and features. Then, implement a design around the device using the manufacturer's application note plus whatever additional features and interfaces the design requires. Most converter subsystems, however, either always or sometimes perform somewhat below the potential of their chosen data converter—usually because of several issues: clocking, unruly switch-mode power supplies, low-quality analog-signal paths, lack of attention to the voltage reference, and digital parts that go awry.

When digital audio was new, the data converter itself was almost the only consideration because it was impossible to build one with as much dynamic range and linearity as the professional or high-end consumer user required in analog equipment. Designers asked only, "What chip is in it?" Nowadays, workmanlike data converters can exceed a dynamic range of 130 dB and total harmonic distortion plus noise of 110 dB rms, unweighted, in the audio band. The weak link in a conversion system is most often elsewhere. No case exists for applying design effort or budget to the data converter itself, except in the most exacting of applications, and where it has already been applied in great measure to the rest of the converter subsystem. To get the best from your chosen data converter, you must apply painstaking design and relentless assessment.

TYPICAL ADC AND DAC SUBSYSTEMS

Figures 1 and **2** show typical ADC and DAC subsystems. You must take special care of the analog bits; several parts of the subsystem will try to make that task difficult. A dashed line indicates where you might consider isolating the analog and

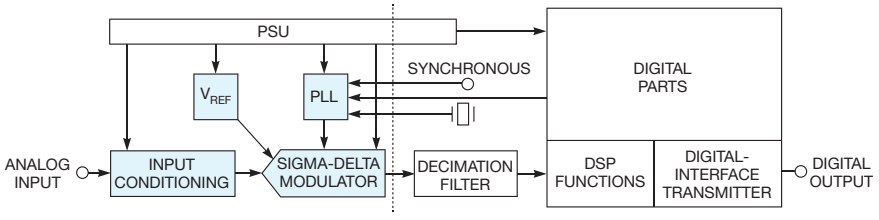

Figure 1 In a typical ADC, you must take special care of the analog bits (blue shading); several parts of the subsystem will try to make that task difficult.

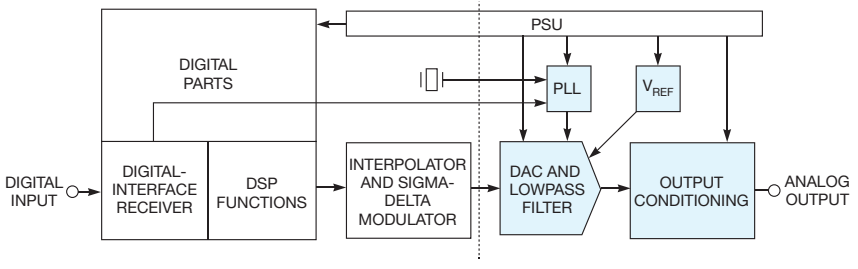

Figure 2 In a typical DAC system, the dashed line indicates where you might consider isolating the analog parts (blue shading) and the digital parts, but many ways are available for doing so, or you can opt not to isolate the parts.

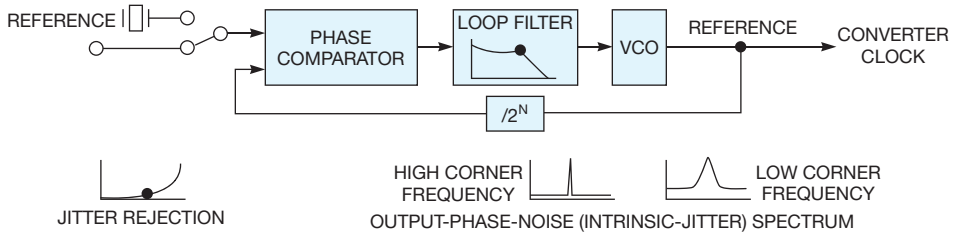

Figure 3 You might use a conventional analog PLL to lock a converter to a reference clock.

the digital parts, but many ways are available for doing so, or you can opt not to isolate the parts.

CLOCK RECOVERY

The conversion clock of a data converter is critical to its linearity because any variation in the regularity of the clock results in sampling jitter, which causes phase modulation of the converted signal (**Reference 1**). You can most easily assess this parameter by passing a high-amplitude, high-frequency signal through the converter and looking for phase-modulation sidebands or skirts in the spectrum of the output.

Converter clocks are usually derived from phase-locked loops rather than local oscillators; it is unusual for a device to be able to always be the system-clock master. It must be able to lock to an external reference or to its digital-audio or computer interface. To lock to all references, the lock range may need to be as wide as ±1000 ppm and must usually accommodate different sample rates (**Reference 2**).

The need to lock converter clocks to various wide-ranging references and to maintain low jitter tends to be among the most difficult challenges in converter design because it embodies some tough trade-offs. Although other applications, such as telecommunications, had somewhat solved this problem before digital audio emerged, audio engineers had to start from scratch, and it's taken a couple of decades to reinvent a good approach. The situation has become more challenging now that you must lock to software-generated syncs and time stamps arriving over computer interfaces because they can embody large amounts of jitter with uncontrolled spectrum and may not come around as often as you'd like (**Reference 3**).

Figure 3 shows a conventional analog PLL that you might use to lock a converter to a reference clock. A phase comparator continually compares the external reference with the regenerated version, and decides whether you should speed up or slow down the voltage-controlled oscillator to make them match in frequency and phase. You need to respond in a leisurely fashion; otherwise, you'll track any incoming jitter. Smooth out the up/down requests with a lowpass loop filter before passing them to the control input of the VCO.

The tough trade-offs, however, are mostly about choosing the right loop-filter characteristics and the right VCO. The design must reject incoming jitter down to low frequencies so that it does not become prey to audible sampling jitter. That requirement also potentially allows you to accommodate a low comparison frequency, such as a reference comprising infrequent software time stamps or a video sync that lines up with an audio sample only every few seconds.

Unfortunately, a low loop-filter corner frequency makes the PLL slow to lock up. Worse, though, it prevents suppression of the phase noise of the VCO around the loop. To avoid unacceptable intrinsic jitter, you must keep the loop filter's corner frequency high, or choose a VCO with low phase noise in the first place.

A good low-noise oscillator is a quartz VCXO. Because of their high-Q factor, however, you can't pull them far from their natural frequency, so they may have a pull range of only ±100 ppm, which may be insufficient for your requirements. On the other hand, a humble RC multivibrator VCO can have all the pull range you need but is essentially untuned, so it has large phase noise and is prey to all manner of interference. A few other VCO options exist between these extremes. To solve the pull-range problem with quartz, you could commission some VCXOs made of a special material with a lower Q, such as LGS (langasite) or lithium tantalate, which are expensive.

You could use a tuned-circuit LC VCO, which has a lower-Q factor than that of crystals, but at least it has a Q factor, so it can be designed with lower phase noise than a multivibrator. These circuits' wide range can cover both 44.1- and 48-kHz rates and can easily accommodate ±1000-ppm reference inaccuracy. Overall, this circuit is not a bad choice; if you're

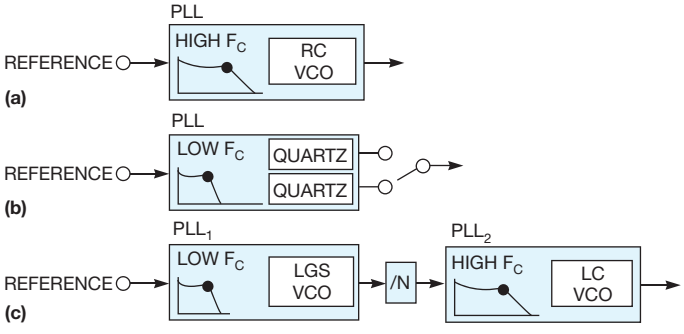

Figure 4 Three analog PLL examples are shown. A basic PLL chip operates in a digital-audio-interface receiver (a). A purpose-designed PLL provides converter-clock recovery, with a higher-Q VCO and a low loop-filter corner frequency (b). Two cascaded PLLs—the first, with an LGS VCXO for wide lock range and a low-corner-frequency filter, which rejects jitter, and the second, with a tuned-circuit VCO and a high loop-filter corner frequency to cover all sample-rate multiples—provide good intrinsic jitter (c).

picky, though, the intrinsic jitter won't be top-class if the corner frequency of the loop is dropped to where you'd like it.

In considering these trade-offs, it is helpful to look at some real-world examples of applying analog PLL technology to converter subsystems (**Figure 4**). The circuit in **Figure 4a** uses a basic PLL chip or, for an AES3 (Audio Engineering Society 3) or SPDIF (Sony/Philips-digital-interface) DAC, uses the PLL in the digital-audio-interface receiver. The VCO, however, has a low-Q factor and high phase noise, usually in the form of an RC multivibrator, which is vulnerable to all sorts of interference, especially power-rail and ground noise, and the corner frequency of the loop filter is high. These problems result in high intrinsic jitter and poor jitter rejection at audible frequencies.

The circuit in **Figure 4b** uses a purpose-designed PLL for converter-clock recovery, with a higher-Q VCO and a low loop-filter corner frequency. This setup results in good intrinsic jitter and jitter rejection, but the pull range may be insufficient, and you must carry the cost of two or more VCXOs.

The circuit in **Figure 4c** uses two cascaded PLLs—the first, with an LGS VCXO for wide lock range and a low corner-frequency filter, which rejects jitter, and the second, with a tuned-circuit VCO and a high loop-filter corner frequency to cover all sample-rate multiples. This circuit has no jitter so it requires no jitter rejection. If you make the LGS VCXO frequency 44.1 and 48 kHz, you can provide a sample-rate reference for the second PLL with a simple programmable divider. This approach has good intrinsic jitter and jitter rejection, works for all sample-rate multiples of 44.1 and 48 kHz, and has a wide lock range. Even with one VCXO, though, it's still expensive, and it still may have questionable performance at low comparison rates.

An even better approach is to adapt the dual-loop architecture as a hybrid PLL by implementing the first PLL in the digital domain, thus eliminating the trade-off of phase noise versus low corner frequency because the loop filter and the VCO are both entirely digital. The VCO—now an "NCO"—is jittery because it is a varying integer division of a fixed master clock, but inclusion of a sigma-delta modulator in the loop means that you can confine its jitter to high frequencies.

It is therefore straightforward to cascade the NCO's output into an analog PLL with a high corner frequency, which can then use an inexpensive VCO without intrinsic jitter. Furthermore, you can change the corner frequency in software to achieve fast lock and then extreme jitter rejection. The hybrid PLL is inexpensive because it requires no resonator-based VCO. Similar approaches are now available for audio use from a number of vendors, including Cirrus Logic (**Reference 4** and **Figure 5**). Some manufacturers even built them into data converters.

Another way to approach this problem is to use modern, low-cost SRC (sample-rate-converter) chips, which are achieving performance that can exceed that of the data converter itself. You might elect to operate the conversion element at a fixed rate provided by a local crystal, thus eliminating sampling jitter, and to convert the converter's input or output data rate. This approach can lead to other issues and places the responsibility on the SRC to achieve jitter rejection that matches the same standard as in the PLL model while also protecting the quality of your audio components.

POWER SUPPLIES

High-quality line-powered audio equipment has traditionally employed linear PSUs, but these devices have disadvantages of size, weight, heat, and cost and may need a manual line-voltage selector. Properly designed PSUs do have the advantage of not providing a source of high-frequency interference into the analog circuits. An SMPS eliminates these

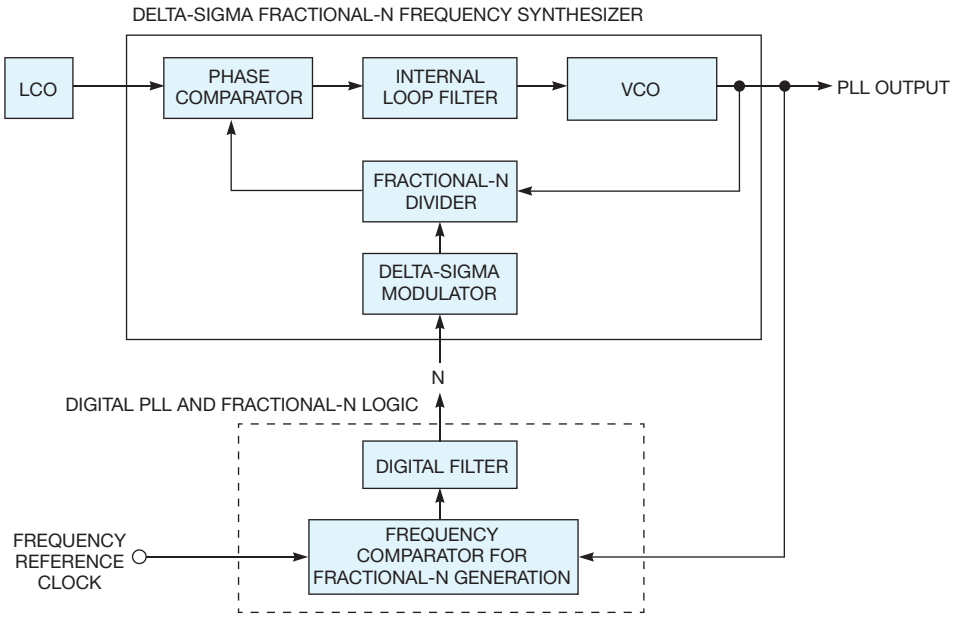

Figure 5 Cirrus Logic's C2000 hybrid PLL is inexpensive because it requires no resonator-based VCO.

disadvantages, but it must be carefully designed if it is not to become a major source of hostile switching noise. High-end-audio designers have traditionally shied away from using SMPSs.

You must design an SMPS in any type of equipment to meet the appropriate electromagnetic-compatibility standards for conducted and radiated emissions. Nowadays, this task is not difficult, with SMPS controller vendors providing application circuits that comply with these standards—usually, just meeting compliance requirements to save the costs of filter components. Unfortunately, the same sorts of misbehaviors that might cause an SMPS to be noncompliant can wreak havoc with audio performance, even at much lower levels. Thus, SMPS design for audio applications can be elaborate.

DRAWBACKS OF LOW-COST SMPSs

Converter systems often need a large number of power rails and may benefit from isolation between the digital and the analog parts, so a flyback architecture is a popular choice because it conveniently offers these benefits, which may also be useful in dc-powered situations. A variety of other simple SMPS architectures can be used instead; the problem for the uninitiated is generally how to choose among them.

In a flyback converter, dc—either directly input or rectified from the ac-line voltage—is switched through the primary of the flyback transformer by a transistor under the control of a device that regulates the duty cycle of a train of switching pulses to regulate the various secondary outputs. Rectified and filtered secondaries provide the power rails.

Figure 6 shows a flyback converter and its switching waveform. Stray capacitance, C_D, across the switch and the leakage inductance of inductor L_{LK} causes the high-frequency oscillation at the point at which the switch turns off. This oscillation is a largely unavoidable source of hostile RF. You can control its amplitude with snubbers to protect the switch, but this approach can make the interference even worse. The low-frequency oscillation before the switch turns on is a consequence of the stray capacitance and the primary inductance, L_P. The switch interrupts the oscillation at a random voltage, causing potential interference from the large switching voltage and current.

The main problem, then, with the basic flyback topology—and with most other basic topologies—is that the transistor switches hard and randomly, causing high levels of radiated and conducted interference to invade the analog audio parts. You are now on a slippery slope, and can't do much to reduce the source of the problem. You can keep the switching loops as small as possible to reduce radiation, you can optimize the ground topology and make critical tracks wider to reduce ground noise, and you can tame the edge times with snubbers, but only at the cost of reduced efficiency and increased heat. So you end up having to take disproportionate steps in the vulnerable parts to make sure that the audio remains clean. These steps can include the use of screening cans, split grounds, or galvanic isolation.

Another problem is the random frequency of the SMPS controller, which can produce interference at the beat frequency between itself and, for example, the audio sample rate, thus making it impossible to confine it to some inconspicuous part of the spectrum. A possible approach is to lock the switching frequency to some multiple of the sample rate to remove the beat frequency, but this approach can be problematic. The regulatory variation of the duty cycle can cause its own beat, and some types of SMPS controllers vary the switching frequency to effect regulation. You could even introduce a situation in which a software bug or a wayward sample rate could collapse the power rails. It's easy to see why designers are reluctant to use SMPSs in high-performance audio equipment, but they often have no choice in dc-powered situations, and SMPSs are small and inexpensive.

RESONANT AND QUASIRESONANT SMPSs

Ideally, to combine the benefits of a linear supply and an SMPS, you would like to find a way of passing a high-frequen-

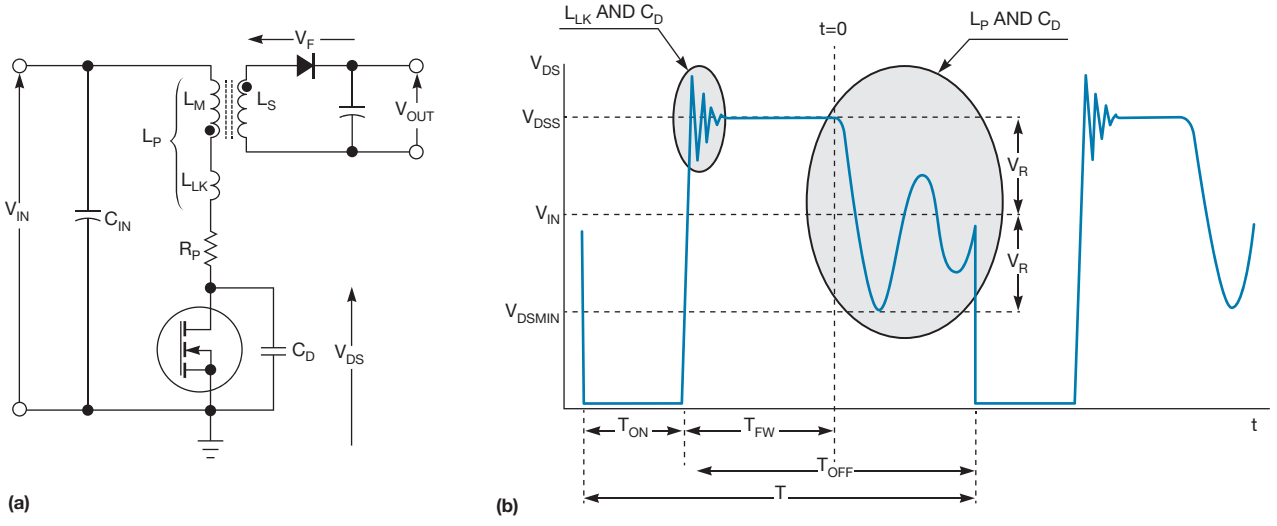

Figure 6 In a flyback converter (a) and its switching waveform (b), stray capacitance, C_D, across the switch and the leakage inductance of inductor L_{LK} causes the high-frequency oscillation at the point at which the switch turns off.

cy sine wave through the transformer. An approximation to such an approach is a resonant SMPS. To losslessly achieve this architecture, it is usual to generate the sine wave by placing a resonant LC-tank circuit in the primary; a neat trick is to use the primary inductance as the inductor. The stimulus for the waveform is still a hard-switching transistor under clever control, but the resonant circuit tunes the primary waveform to an approximation of a simple sine wave, with the switching happening at 0V or 0A moments, all of which leads to less hostile switching noise.

On the other hand, resonant designs tend to be somewhat more costly and larger than flyback designs. A major drawback with many resonant architectures is that you must tailor the LC-tank circuit to the switching frequency and dc input voltage to maintain resonant and zero-switching operation, which makes offline universal input design problematic unless you incorporate power-factor correction.

A good compromise is a quasiresonant converter. The idea here is that, because the problems in a simple flyback converter happen only at the moments of switching, it is necessary to find a way of creating a resonant waveform only at the switching points. You can achieve this goal by simply introducing primary resonance into an ordinary flyback topology and making the controller clever about deciding when to switch. **Figure 7** shows a zero-voltage-switching, or valley-switching, quasiresonant converter, which is a low-cost way to cut SMPS emissions at their source (**Reference 5**).

In this case, you create the tank circuit by simply adding a large capacitor across the switch. The tank circuit slows the switch-off rise time, and the controller arranges the switch-on instant to coincide with a valley in the low-frequency oscillation; this approach inherently makes the cycle period variable with an attendant spread-spectrum effect, which can improve interference and which increases EMC margins (**Figure 8** and **Reference 6**).

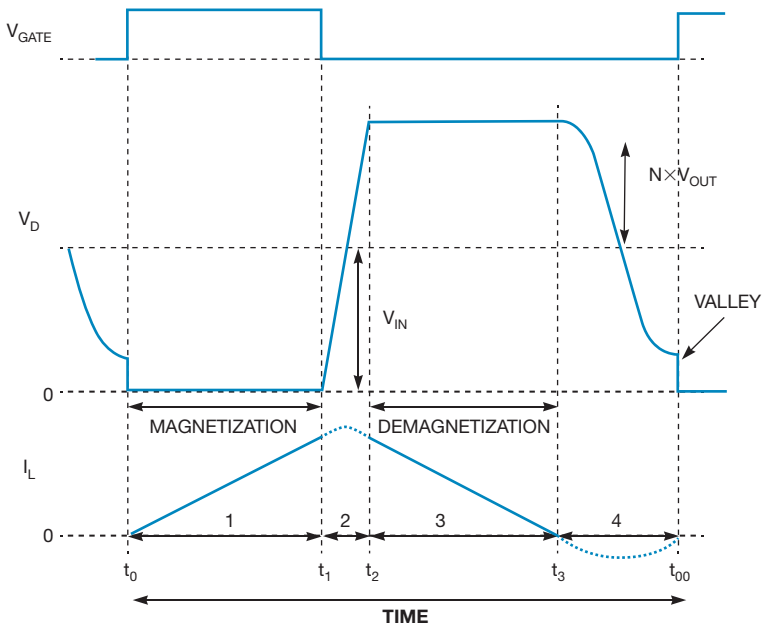

Figure 7 A zero-voltage-switching, or valley-switching, quasiresonant converter is a low-cost way to cut SMPS emissions at their source.

SMPS SELECTION

It is often difficult for the uninitiated to make the correct choice of SMPS architecture for audio because most SMPS-controller vendors organize their selection tables by power capability. They assume that audio designers, like other designers, will want to choose the cheapest approach for their power requirement. The recommended SMPS for low-power applications such as this one—say, less than 20W—is usually a basic, hard-switching type because the power is low enough for its emissions to remain below statutory EMC limits with minimal filtering and for the losses resulting from its indiscriminate switching to be insufficient to set it on fire.

Higher-power applications in which you must control switching noises and losses require the use of resonant and quasiresonant topologies. For audio, however, it's often a good idea to make a low-power implementation of a high-power topology in the interest of achieving minimum emissions; you can usually make up for the extra cost by not having to armor-plate the audio parts.

OTHER CONSIDERATIONS

Cross-regulation—varying load conditions on individual rails—can cause the voltages of other rails to vary and is often a problem with multirail-SMPS designs because the regulatory mechanism of the controller can generally operate on only one rail. In performance-critical applications, it may be necessary to provide linear postregulation on analog-power rails from the SMPS. If so, take care to provide adequate cooling for the linear regulators. Linear regulators can usually regulate over only a limited frequency range, and the switching products from the SMPS can easily exceed this range, causing them to pass straight through the regulator. It is therefore a good idea to use ferrite beads ahead of linear postregulators.

Line-powered linear and SMPS equipment usually draws current from the mains only during voltage peaks, which can cause distortion to the power line, with possible detriment to the performance of other sensitive audio equipment. It may be beneficial to incorporate PFC into your SMPS design to cause the least possible distortion to the power waveform. You can be sure, however, that all the other equipment around the SMPS will probably be causing distortion anyway. Some PFC schemes allow tight control of the rectified voltage ahead of the SMPS, which can allow you to further reduce switching noise in resonant and quasiresonant designs by ensuring no switching for any input voltage.

As well as applicable safety, EMC, and disposal legislation, line-powered equipment is subject to or will become subject to various territorial legislation for standby-power consumption, when applicable, and operating efficiency—for example, under the European Union's Ecodesign Directive and the voluntary US EnergyStar program. Although territorial legislations vary,

maximum standby-power consumption of 0.5W and minimum operating efficiency of approximately 80% are typical for a 20W device.

ANALOG-SIGNAL PATH

Analog performance is the limiting factor in many converter designs. Somewhere along the line, perhaps you forgot some of this wisdom. All of the buffer amplifiers, gain stages, and other components between the outside world and the ADC and between the DAC and the outside world are obvious areas in which good design practice will pay dividends. It is no mean feat to maintain the performance of a flagship data converter through the analog circuits, particularly if you must incorporate significantly high performance.

In general, use a ground plane for analog circuits and take advantage of the small surface-mount-technology packages that are now available. Lay things down instead of standing them up. These measures are free and will reduce susceptibility to interference and crosstalk.

Of particular importance are the buffer circuits, which drive by the input of the ADC or are driven by the output of the DAC. In general, the safest policy is to stick with the exact circuit topology and components that the converter manufacturer recommends. The vendor will have spent a long time coaxing the best out of the device by tweaking its buffer. However, this scenario is not always true. With experience and care, it is sometimes possible to exceed the application-note performance. On the other hand, if cost is important, you can often scrimp a bit on op-amp types.

Sigma-delta ADC inputs often have a nonlinear-input characteristic and produce aliasing components if subject to high frequency, so an ideal ADC buffer must achieve a lot of high-frequency roll-off—but without compromising in-band flatness—and a low output impedance. It's better to avoid the passive pole between the output of the buffer and the input of the converter and to instead use, for example, an analog-input buffer (**Reference 7**).

Many high-quality DACs have current outputs, requiring an outboard current-to-voltage-converter circuit. Sigma-delta DACs often produce significant out-of-band noise, and the IVC must filter, cancel, or both filter and cancel this noise in the first instance. Therefore, to maintain in-band linearity, the IVC must behave linearly at frequencies well above the audio band. If you are tempted to stray from the manufacturer's recommended IVC design, bear in mind the bandwidth requirement and note that the data converter's output loading will probably have to be similar to that of the application circuit for optimum performance.

As for the rest of the analog-signal path, it is important to choose the right components and circuit topologies. The most straightforward way is to use op amps. This approach is currently a good policy except in a few situations, such as microphone/phonograph preamps and high-current outputs. It will pay to familiarize yourself with the noise models for op-amp circuits, such as those that **Reference 8** describes, and to implement a spreadsheet to calculate noise levels for your circuit. A simpler but less versatile approach is to use op-amp manufacturers' noise-reckoning tools (**Reference 9**). The best approach is to use a full-blown Spice simulator (**Reference 10**).

You will find that your choice of op amps in each stage is generally restricted to relatively few that have the requisite voltage-noise, current-noise, or both voltage- and current-noise performance. The world is full of op amps, most of which are not good for audio. On the other hand, beware the best-audio-op-amp syndrome.

No op amp will behave best in every audio stage. In each case, you must select the right one for the job. Usually, you can make this selection from looking at available data or by trading off requirements against cost, power, and other factors. But don't be afraid to use trial and error in the end, although doing so requires some determination and good eyesight in this age of SMT. With some dexterity, you can persuade dual-inline sockets onto the SOIC sites in your prototype. In general, it's a good idea to use dual-op-amp sites because doing so is a good trade-off of cost and choice and allows tight layout in balanced circuits.

Designers generally prefer inverting-op-amp topologies over noninverting models because the inverting devices' input terminals operate at virtual earth. The dynamic input-common-mode voltage of noninverting configurations

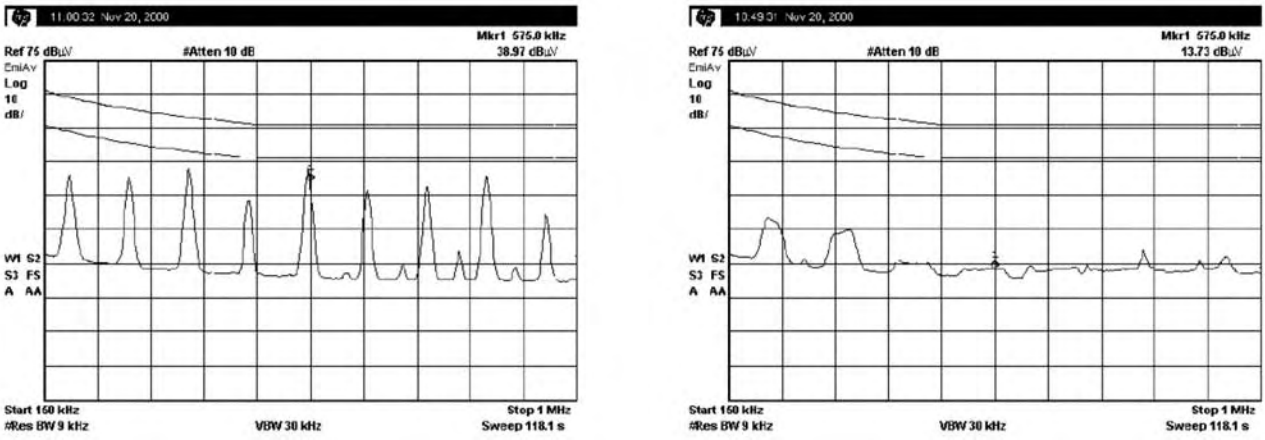

Figure 8 The tank circuit slows the switch-off rise time (a), and the controller arranges the switch-on instant to coincide with a valley in the low-frequency oscillation (b).

may add distortion, particularly at high frequencies with some op amps. Consider adopting a fully balanced topology end to end—perhaps using a "symmetrizer" in the ADC's case to achieve balance through the channel even with unbalanced inputs. Avoid mode-conversion types, however. Using a fully balanced topology not only reduces interference and crosstalk but also can achieve higher performance because distortion mechanisms often tend to cancel. Most high-end data converters operate in a balanced mode anyway.

It is important to select a gain structure that maximizes the dynamic range, or SNR, and thus minimizes the need for excessively low-noise design, with its attendant cost. Even so, resistor values must be low enough for their thermal noise to be out of the picture but not low enough to bring problems of overdissipation or circuit loading.

The linearity of resistors and capacitors is also important. Resistors must be metal-film or thin-film types, not the usual chip resistors, which change resistance according to voltage and the seasons. Capacitors must be low-k ceramic types, such as C0G and NP0 types, or low-loss plastic, such as polystyrene. Failure to observe these rules leads to nonlinearity and distortion in most circuit topologies. Keep electrolytics out of the signal path; there are other ways to ensure extended low-frequency response.

PCB layout of the channel circuits is critical for minimizing both interference and interchannel crosstalk. Make sure that the op amp's output and the ground nodes of the stages are outermost and that the op amp's input nodes are innermost in your channel-strip layout.

Pay attention to the bandwidth of your stages. It's not always better to go for a dc-to-light approach. Limiting the bandwidth at the top end reduces susceptibility to interference, and the presence of excessive high frequency, even if inaudible, does no good to the in-band signal. Limiting the bandwidth at the bottom end removes wandering dc, which can cause problems with mixing and switching, as well as the risk of unexpected overload. On the other hand, keep a healthy disrespect for the –3-dB, 20- to 20-kHz approach. Extend the top and the bottom end beyond the bare essentials when possible and strive to keep the area between flat; you will notice the difference.

REFERENCE VOLTAGE

Nearly all data converters have at least one accessible reference-voltage pin, reference-current pin, or both. The reference multiplies the input to the converter to produce the output, so how you handle the reference is just as important as the analog-signal path. Any noise or interference on the reference modulates the converter's output. You must filter internally generated voltage references by placing suitable capacitors close to the pins. This approach usually requires an assortment of low-value, high-frequency, large electrolytic or tantalum capacitors.

In some cases, you may want to drive a voltage reference externally from a well-regulated and filtered source. Some converter devices require both high and low reference voltages to define their operating range, and some require separate references per channel. Although users can sometimes to some degree modify the reference voltages, manufacturers often optimize converter performance at a particular voltage, and it's best to stick with that voltage. When your design has distortion or noise problems, remember to look at the reference. If modulation issues, such as sidebands or noise skirts around the signal frequency, get worse with increasing signal frequency, it's jitter. If those issues don't get worse, then the problem is most likely the reference voltage (**Reference 11**).

DIGITAL PARTS

Any low-quality digital processing in the signal path can undo all of your good work in the analog domain. Make sure that your design has enough precision everywhere and that algorithms are beyond reproach. Culprits often include dithering, noise-shaping, and dynamics processing. Remember, too, those parts of the digital-signal path that designers often overlook. For computer interfaces, the driver or parts of the operating system that you thought you had bypassed sometimes let you down. You must be able to test your entire signal path, so make

sure that your dual-domain audio-test equipment can work in the computer domain, directly interfacing with your driver layers.

In the old days, it was almost possible to keep all of the digital parts of a converter system ticking at some multiple of the sample rate. Consider the simple case of an AES3-interfaced converter with no DSP and no microcontroller. Nowadays, though, you must have a boxload of computers, including DSPs, RISC processors, and FPGAs, all running asynchronously, and probably a computer interface buzzing away across the entire spectrum. Although lower operating power, lower core voltages, and smaller dice and packages contribute to reducing the hostile intent of digital electronics, a designer can do little to fix it beyond observing good EMC design at ports and good power decoupling and filtering.

You must make some fundamental decisions at the outset of your design. These decisions include the choice between line power and dc power, as well as choices regarding whether you can put your design into its own metal box, whether it must cohabit with digital parts, or whether it must reside in a host computer. You also must decide whether you need and whether you can afford screening cans. Another decision comes up when you consider construction: Can you use a multilayer PCB with groundplanes, a small SMT device, or another configuration? What about isolation? Can you galvanically isolate the analog and digital domains using optical or magnetic isolators? This isolation can be beneficial in computer or computer-interface cases, in which the digital ground can be toxic. You also need to weigh EMC compliance and efficiency. Project requirements and component budget probably dictate the answers to these questions.

The objective assessment of converter systems, both during design and in general, is a complex subject and the subject of many international standards, such as IEC 61606-3 and AES17-1998 (**references 12**, **13**, and **14**). It is useful, however, in many situations to make a simpler assessment. For many engineers, this assessment involves instead using listening tests to determine audibility. The debate about whether measuring or listening is better will rage forever. However, developing high-performance audio requires both methods. Some engineers believe that it is better to use measurement to debug the design and to worry about listening tests after that.

For debugging, first equip yourself with an audio analyzer, which can stimulate and measure in the analog, digital, and computer domains. Analyzers should be able to display a continuous high-resolution FFT, and they should be user-programmable so that you can automatically hop among key measurements. You must be able to define all of the key measurement parameters when you set up the debugger. Make a lead to connect a pair of small probes to the analog analyzer's input so that you can measure between all the stages. SMPS and computer-based devices also need a means of seeing the wideband spectrum, which EMC precompliance also requires. **Table 1**, available with the Web version of this article at http://bit.ly/w29NCL, provides a guide to the most important audio-performance parameters that apply to conversion systems. **EDN**

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AUTHOR'S BIOGRAPHY

Ian Dennis is technical director of the Prism Sound Group, a manufacturer of audio converters, test-and-measurement equipment, audio workstations, and media servers. He has been designing audio equipment since the early 1980s. At Prism Sound, he focuses on R&D and production activities but also works on a few design projects now and then. Current interests include audio conversion, audio-test equipment and methods, media-streaming devices, and audio networking. Dennis is vice chairman of the Audio Engineering Society SC-02-01 Standards Committee for audio test and measurement and also works on standards development within the BSi and International Electrotechnical Commission, most recently contributing to IEC 61606-3 test methods for professional digital-audio equipment and ITU BS.1770 loudness metering.