GETTING THE FULL POTENTIAL FROM YOUR ADC

By John Austin

Many of today's high-resolution ADCs (Analog-to-Digital Converters) are operating from a single supply and utilize fully differential inputs. This can be a problem for single-ended signals that are bipolar relative to common. This article will illustrate circuit configurations that will preserve the full-scale input range by utilizing modern features, such as Programmable Gain Amplifiers (PGAs) and internal voltage reference. It will also discuss issues that the designer must consider when selecting components utilizing these signal-conditioning circuits.

The differential inputs provide common-mode rejection eliminating much of the system noise imposed on the input signal. In most converters, the reference inputs determine the full-scale analog input range as well as the position of bipolar zero of the analog input signal.

For truly differential input ADCs without a built-in PGA, Figure 1 is a proposed solution.

The transfer equations are derived using basic circuit analysis and general op amp theory. See Appendix A for the detailed derivation.

$$\frac{R_2}{R_1} = G_{(U1)}$$

$$\frac{R_6}{R_5} = G_{(U2)} \qquad (1)$$

$$\frac{R_3}{R_3 + R_4} = \frac{V_{BIAS}}{V_{REF}\left(G_{(U1)} + 1\right)} = \frac{1}{\left(G_{(U1)} + 1\right)}$$

For example, assuming a converter requires a full-scale differential input of 2.5Vp-p referenced at 2.5V DC operating from a single 5V supply. Knowing the DC bias value, the gain/attenuation, and the power supply, the resistor values are calculated using the equations provided. The input signal V_{IN} = 5Vp-p (bipolar).

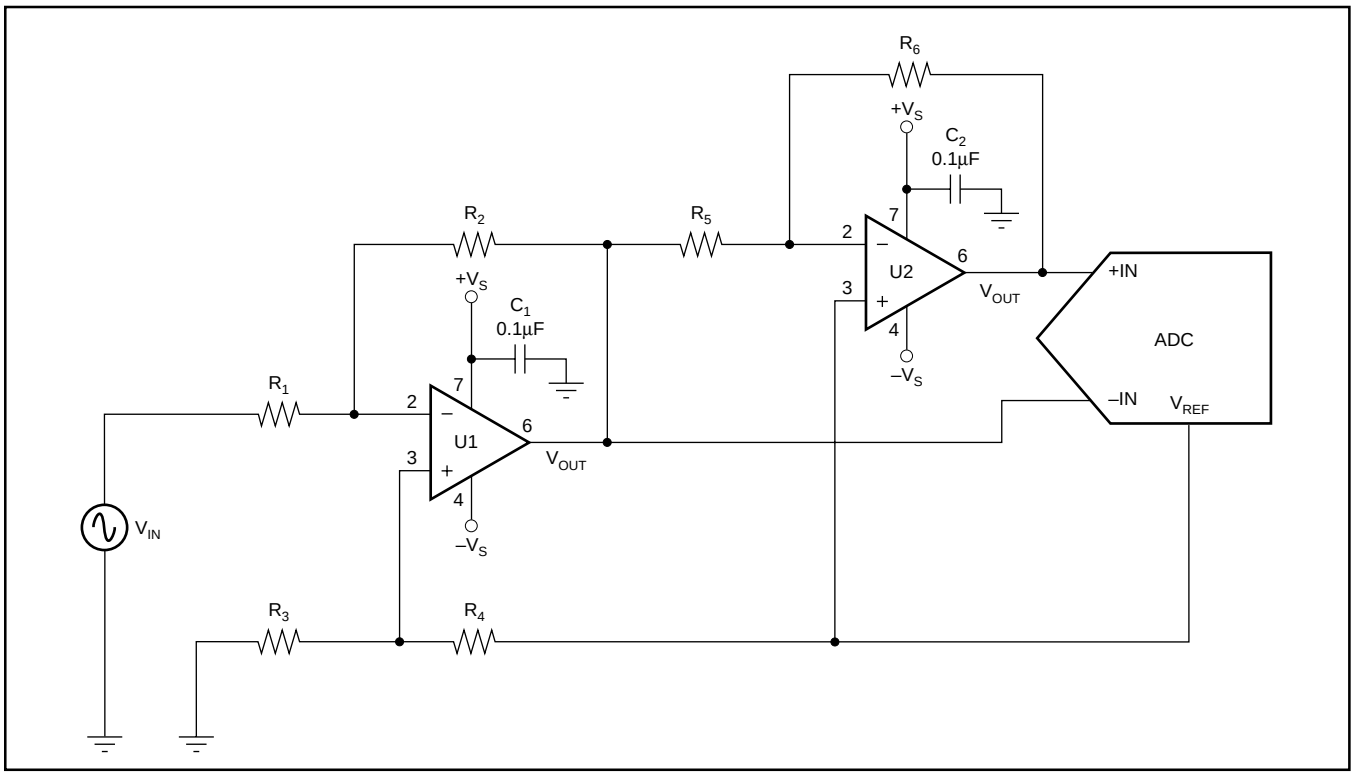

FIGURE 1. Circuit Schematic to Convert a Single-Ended Bipolar Input to a Unipolar Differential Output.

The required resistor ratios, corresponding to Figure 1, are calculated as follows:

$$\frac{R_2}{R_1} = G_{(U1)} = 1/2$$
$$\frac{R_6}{R_5} = G_{(U2)} = 1 \qquad (2)$$
$$\frac{R_3}{R_3 + R_4} = \frac{V_{BIAS\ (U1)}}{V_S\left(G_{(U1)} + 1\right)} = (2.5) / \left[5\left(1/2 + 1\right)\right] = 1/3$$

From these ratios we can determine resistor values. The resistor values used for this example were $R_1 = R_4 = R_5 = R_6 = 300k\Omega$ and $R_2 = R_3 = 150k\Omega$. Figure 2 displays the input signal (V_{IN} = 5Vp-p bipolar) and the differential output (V_{OUT+} and V_{OUT-}). The output corresponds to a 2.5Vp-p differential signal DC biased at 2.5V.

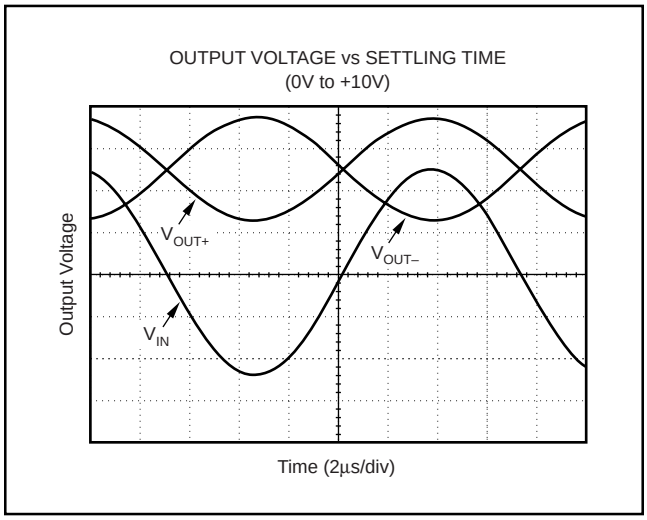

FIGURE 2. Scope Trace (circuit of Figure 1), V_{IN} = 5Vp-p (bipolar), with a Corresponding Differential Output, (V_{OUT+}, V_{OUT-}) = 2.5Vp-p Biased at 2.5V DC.

If the ADC does not have an internal voltage reference, one might assume that a simple resistor divider from the power supply would suffice for the reference input to the ADC. The designer must keep in mind that any change on the voltage reference will cause a one-to-one change in the output of the converter. Resistors tend to drift and are the cause of unwanted noise. Utilizing a precision, low-drift, low-noise voltage reference is always a good design practice.

The new multi-feature ADCs, such as the ADS7870, ADS1210/ADS1211, ADS1212, and ADS1250 from Texas Instruments offer both a PGA and internal voltage reference. Figure 3 implements these features providing a simple resistor network as a possible solution.

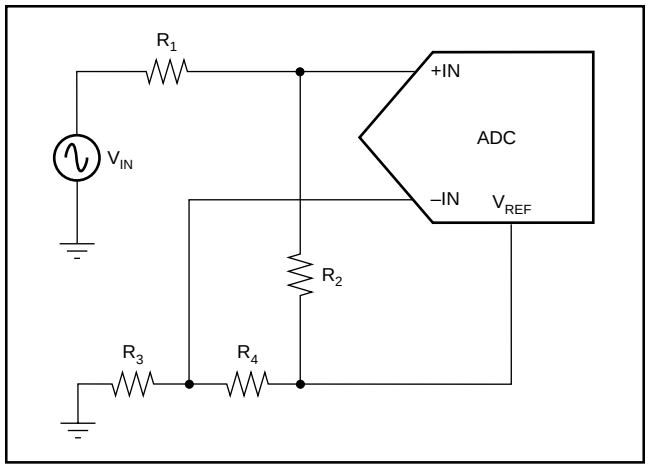

FIGURE 3. Utilizing a Resistive Network to Achieve Attenuation and DC Bias of the Input Signal.

This configuration can provide more accurate results and minimize the number of components. One could assume that this would not provide any better accuracy and would only bring a similar gain circuit into the ADC. Certainly this circuit would minimize components and lower cost, which would be a benefit to the designer.

The transfer equations are as follows. See appendix A for a detailed derivation.

$$\frac{R_2}{R_1 + R_2} = \frac{+In}{V_{IN}} = 1/2$$
$$\frac{R_3}{R_3 + R_4} = \frac{R_2}{R_1 + R_2} = 1/2 \qquad (3)$$

From these ratios the resistor values were chosen to be $R_1 = R_2 = R_3 = R_4 = 150k\Omega$. The pseudo-differential value, (+In – (–In)), corresponds to a 2.5Vp-p. Utilizing a PGA setting of 2 effectively utilizes the full-scale input range.

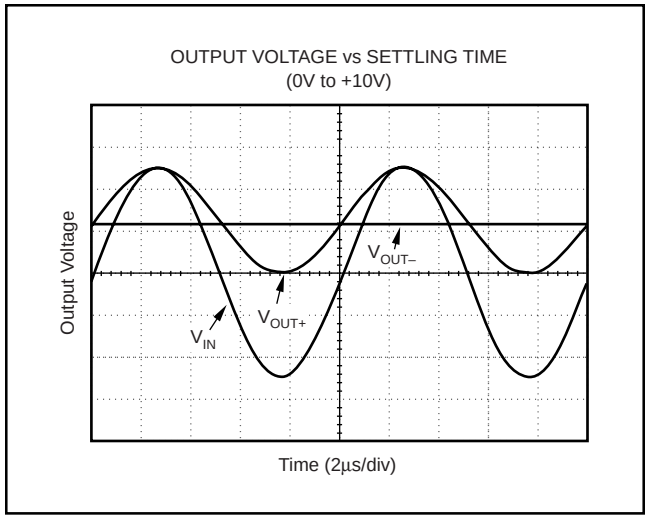

FIGURE 4. Scope Trace (circuit of Figure 4), V_{IN} = 5Vp-p V_{IN} = 5Vp-p (bipolar), with a Corresponding Output, V_{OUT+} = 2.5Vp-p Biased at 2.5V DC, V_{OUT-} = 2.5V DC.

Loading the reference can cause undesired drift of the reference voltage. The designer must also consider the input impedance of the ADC. Low input impedance may cause signal loss. If this becomes an issue, Figure 5 can be implemented.

R_4/R_3 provides the DC bias while R_2/R_1 provides the attenuation/gain. The PGA amplifies the differential signal (+In – (–In)), effectively preserving the full-scale input range of the device.

$$\frac{R_2}{R_1} = G_{(U1)} = 1/2$$
$$\frac{R_3}{R_3 + R_4} = \frac{1}{G_{(U1)} + 1} = \frac{1}{\frac{1}{2} + 1} = \frac{2}{3} \quad (4)$$

From these ratios the resistor values were chosen to be $R_1 = R_3 = 100k\Omega$, $R_2 = R_4 = 200k\Omega$. The pseudo-differential value, (+In – (–In)), corresponds to a 2.5Vp-p. A PGA setting of 2 maintains the full-scale range of this device. Without the PGA this circuit ((+In) – (–In)) would only make use of half of the full-scale input range.

Component selection is critical when dealing with high-resolution applications. The main selection criteria for the op amp includes offset voltage drift and noise. DC offset, such as gain error and input offset voltage, can be taken out through software calibration or by internal calibration of the ADC.

The lowest drift amplifiers are those that are chopper stabilized, such as the Texas Instruments TLC2652. This amplifier has a supply range of ±1.9V to ±8V, offering very low offset voltage (1mV) and low offset voltage drift (3nV/°C). These amplifiers have limited bandwidth and generate more noise than other amplifier architectures. The TLC2652 has a maximum voltage noise of $35nV/\sqrt{Hz}$ (at 1kHz) and a typical unity-gain bandwidth of 1.9MHz. This amplifier is more suitable for low-frequency applications.

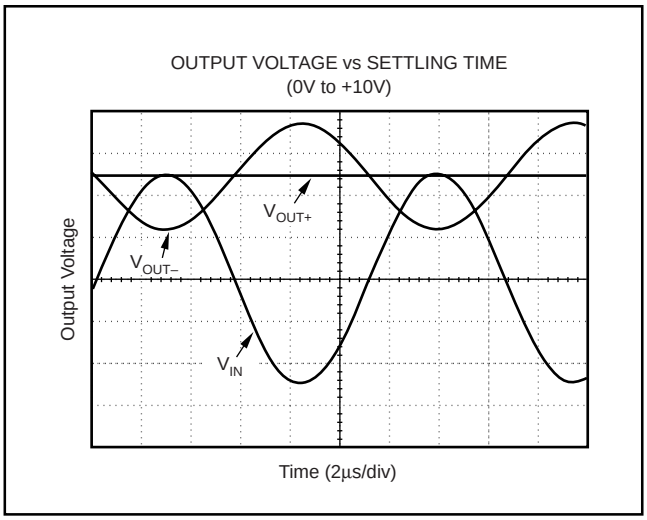

FIGURE 6. Scope Trace, V_{IN} = 5Vp-p V_{IN} (bipolar), with a Corresponding Output, V_{OUT+} = 2.5V DC V_{OUT-} = 2.5Vp-p Biased at 2.5V DC.

DIFET amplifiers offer low-voltage drift (100s of nV/°C), have very low noise (less that $10nV/\sqrt{Hz}$) and offer higher unity-gain bandwidth than chopper-stabilized op amps. These would be considered for higher frequency applications where noise might become a larger factor than voltage drift. The major drawback is cost.

Amplifiers implementing a bipolar process can offer good precision, higher unity-gain bandwidth, and maintain low noise at a relatively low cost. An example would be the OPA227 family of op amps. This op amp has low voltage drift (300nV/°C (max)) and very low voltage noise ($3nV/\sqrt{Hz}$ (max)). This amplifier has an 8MHz unity-gain bandwidth (min) and a slew rate of 2.3V/µs (min) and would be a good choice for high-frequency applications. It also provides a cost-effective solution at a price well under a dollar per channel.

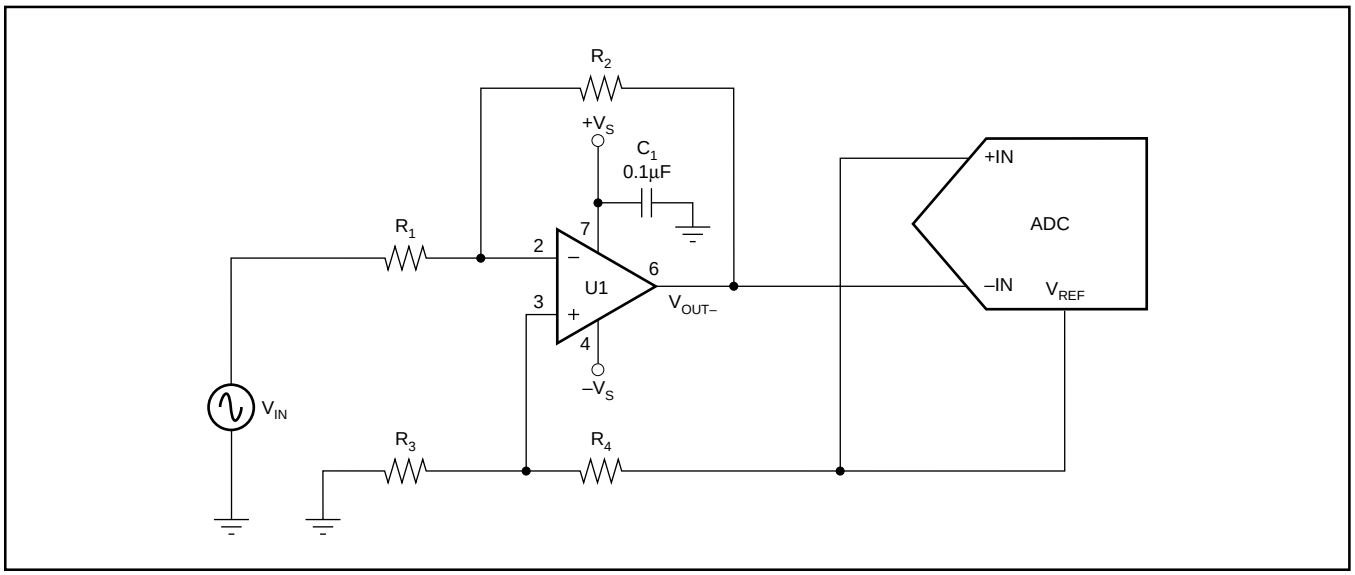

FIGURE 5. Circuit Schematic Utilizing the Programmable Gain Amplifier and Output Voltage Reference.

CMOS amplifiers are probably the most inaccurate but the most cost effective. These are typically single-supply amplifiers. A good example is the OPA340 series from Texas Instruments. These are single-supply 2.7V to 5.5V amplifiers with an input voltage range of 300mV beyond the supply rails and an output voltage that can swing to within 1mV of the supply rails. These devices tend to have higher noise characteristics (25nV/$\sqrt{Hz}$ (max)) and larger voltage drift (2.5µV/0°C (max)). They should be used in lower resolution applications where cost is of more concern than resolution.

This document has provided three signal-conditioning circuits that allow the designer to make use of a fully-differential ADC when utilizing a single-ended signal source. Op amp architectures discussed have both benefits and pitfalls to consider and weigh according to the specifics of the application. The accuracy provided by these circuits is directly related to the component selection and the parameters discussed. Other design considerations are board layout, power-supply selection, and good filtering techniques.

APPENDIX A:

Derivation of the transfer equations for the circuit of Figure 1.

From the model for an ideal op amp, we assume infinite input impedance. This implies there is no current into the op amp.

$$I_{R1} = I_{R2} \tag{1}$$

$$\frac{V_{IN} - V_{2(U1)}}{R_1} = \frac{V_{2(U1)} - V_{OUT}}{R_2} \tag{2}$$

Combining terms and solving for V_{OUT-} yields:

$$V_{OUT-}\frac{R_2}{R_1}V_{IN} = V_{2(U1)}\left(\frac{R_2}{R_1}+1\right) \tag{3}$$

Making the substitution that the voltage at pin 2 is equal to the voltage at pin 3 gives:

$$V_{OUT-} = -\frac{R_2}{R_1}V_{IN} + \left(\frac{R_2}{R_1}+1\right)\left(V_{3(U1)}\right) \tag{4}$$

The voltage at pin 3 can easily be calculated by a voltage divider.

$$V_{3(U1)} = \frac{R_3}{R_3+R_4}(V_S) \tag{5}$$

Combining equation 5 with equation 4 yields:

$$V_{OUT-} = -\frac{R_2}{R_1}V_{IN} + V_S\left(\frac{R_2}{R_1}+1\right)\left(\frac{\frac{R_3}{R_3}}{R_3+R_4}\right) \tag{6}$$

Where the DC bias value is:

$$V_{BIAS(U1)} = \left[\left(\frac{R_2}{R_1}+1\right)\left(\frac{R_3}{R_3+R_4}\right)\right] V_{REF} \tag{7}$$

Equation 6 provides the final transfer equation for op amp U1. The input signal is inverted with a gain/attenuation of (R_2/R_1) and a DC bias corresponding to equation 7. If we let (R_2/R_1) = $G_{(U1)}$ (gain) and solve for the resistor ratio $R_3/(R_3 + R_4)$, equation 7 yields:

$$\frac{R_3}{R_3+R_4} = \frac{V_{BIAS}}{\left(V_S\left(G_{(U1)}+1\right)\right)} = \frac{1}{\left(G_{(U1)}+1\right)} \tag{8}$$

Derivation of transfer equations for the circuit of Figure 3

The input $+I_N$ can be calculated by:

$$+I_N = \frac{R_2}{R_1+R_2}V_{IN} + \frac{R_1}{R_1+R_2}V_{REF}$$

$-I_N$ requires the same DC voltage as the DC bias voltage of $+I_N$. This requires the resistor ratios be the same:

$$\frac{R_1}{R_1+R_2} = \frac{R_3}{R_3+R_4}$$

Solving for the resistor ratios yields:

$$\frac{R_2}{R_1+R_2} = \frac{+In}{V_{IN}}$$

$$\frac{R_3}{R_3+R_4} = \frac{R_2}{R_1+R_2}$$

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