MEETING YOUR CUSTOMER'S HIGH-AVAILABILITY GOALS MEANS TROUBLESHOOTING AND REPLACING BOARDS WHILE YOUR SYSTEM IS OPERATING. FOLLOW THESE LIVE-INSERTION BOARD-DESIGN GUIDELINES TO KEEP THE SPARKS FROM FLYING.

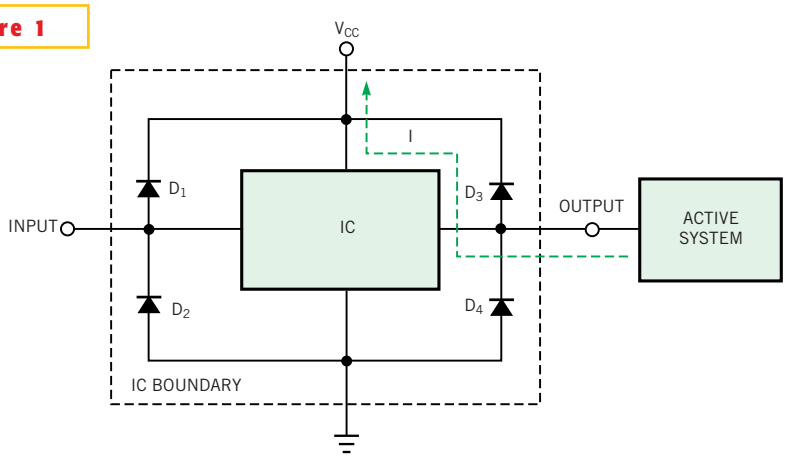
Hot-swap your way to high availability

High-availability systems, such as telecomm, real-time-transaction-processing, air-traffic-control, and fault-tolerant-computing equipment—increasingly require you to insert and remove pc boards without turning off the power. Such systems can only have minimal downtime, so the ability to exchange hardware without affecting the system is important. Implementing this "live-insertion," "hot-plugging," or "hot-swapping" capability requires careful hardware and software design. Various logic and bus-switch families have different capabilities and design considerations when you use them in live-insertion applications.

MAINTAINING DATA INTEGRITY

A key issue during live insertion is maintaining data integrity on the system bus while preventing damage to the components of the host system or the components of the live-inserted pc board. Components must meet one of the three levels of bus isolation. In the first level, the construction of the components is such that when the components are unpowered you do not damage them when you connect them to a live bus. Further, to prevent a component's input or output pins, which are connected to the interface, from loading down the system bus, the components' outputs must remain in a high-impedance state, have a "power-off-disable" feature, and support partial- power-down mode. The second level requires that hot-swap components support partial-power-down mode and include circuitry to keep their outputs in a high-impedance state during power-up or -down. A power-up/-down, three-state circuit prevents loading and conflicts on a live bus. System software must be able to detect the live-in-

Figure 1



D_1 and D_2 are clamp diodes, and D_3 and D_4 are parasitic diodes. If you connect either the input or output of this IC to a live bus while the device is unpowered, current can flow through D_1 or D_3, possibly damaging the active system or causing bus glitches.

sertion event, detect and correct any bus errors, and reinitialize the bus as needed. The third level of isolation includes the previous two levels and adds circuitry to precharge to a preset voltage level the bus of the pc board you are inserting. The precharge voltage reduces glitches that the bus's impedance and capacitance at the live-insertion interface cause.

IC CONSTRUCTION

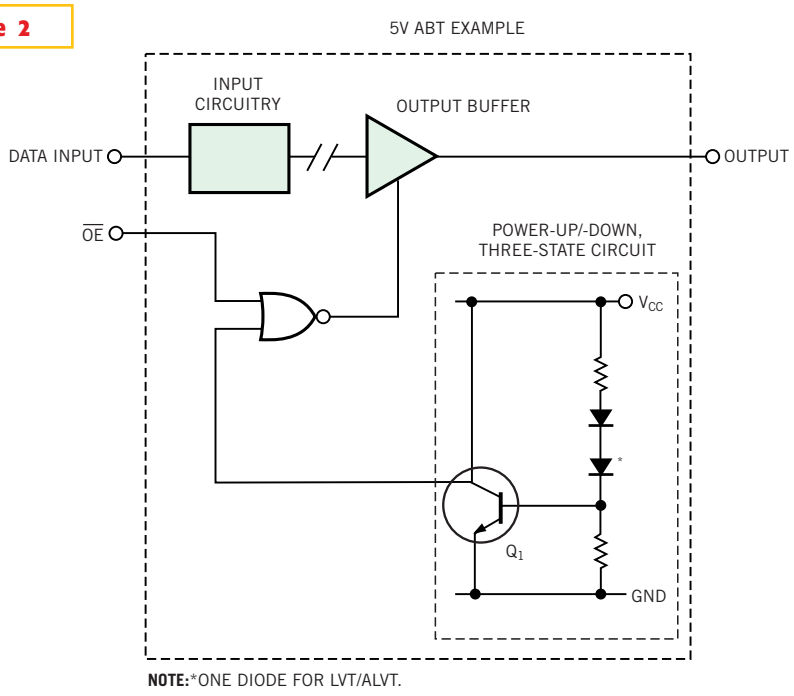
Understanding IC construction can help you in selecting components that prevent live-insertion problems. For example, circuits with protection diodes on their inputs and outputs can present a problem during insertion into a live bus. **Figure 1** shows a simplified construction of an IC. In a classic CMOS circuit, D_1 acts as an overshoot clamp. It is absent in bipolar and BiCMOS circuits. You implement D_2 in most circuits to limit undershoot or provide ESD protection. D_3 is a parasitic diode intrinsic to CMOS outputs. D_4 is a collector-to-substrate or drain-to-substrate parasitic diode. In bipolar devices, you can add a Schottky diode to limit undershoot.

If the device in **Figure 1** is unpowered and you plug either its input or output into an active bus, current flows through D_1 or D_3, possibly damaging them or the active system. This occurrence can also momentarily pull down the host system's bus voltage, possibly disrupting the host system. Likewise, during extraction or power-down, those diodes present a path to V_{CC} and can pull down the bus voltage to the decaying V_{CC} level. You must eliminate the diodes or current path to facilitate live insertion. Further, output circuits must remain in a high-impedance state during power-up or -down so that they don't drive or pull down the active bus.

Some newer CMOS and BiCMOS logic families from Philips Semiconductor address these issues with modified I/O circuitry. V_{CC} clamp diodes have been removed on input circuits. Power-off disable circuitry protects the output's parasitic diodes during power-down. The power-off disable feature (shown as I_{OFF} in the dc-characteristics section of the data sheets) is available in the ABT, LVC, LVT, ALVT, AVC, ABTE, FCT, LPT, and LCX product families. These families meet the first level of isolation required for live insertion.

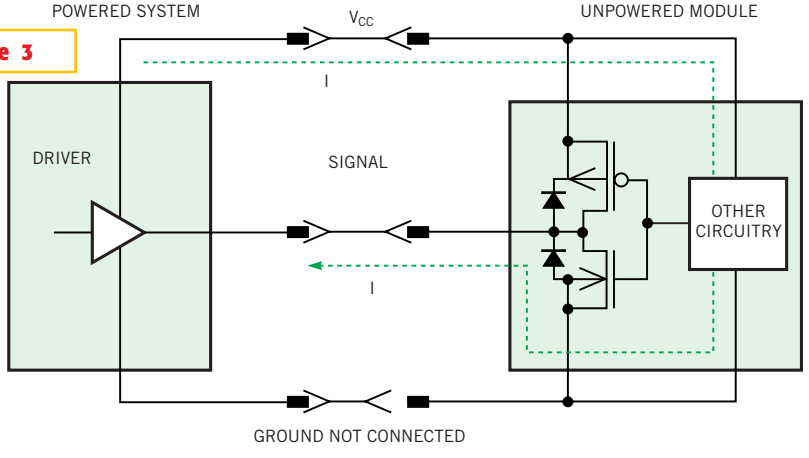
In addition to power-off isolation on inputs and outputs, some BiCMOS families employ a power-up/-down, three-state circuit to keep the outputs in a high-impedance state during power sequencing (**Figure 2**). The power-up/-down, three-state feature (shown as I_{PU}/I_{PD} in the dc-characteristics section of

Figure 2



Some BiCMOS families employ a power-up/-down, three-state circuit to keep the outputs in a high-impedance state during power sequencing. During power-up, Q_1's collector follows V_{CC}, which the input of the NOR gate interprets as a high. This high disables the output buffer regardless of the voltage on the enable or data pins until V_{CC} rises, forward biasing Q_1's base-to-emitter junction, which pulls the input of the NOR gate low.

Figure 3



If the ground pin of a pc board does not make contact first with the mating pin when you insert the pc board into a connector, current can flow from V_{CC} to an output.

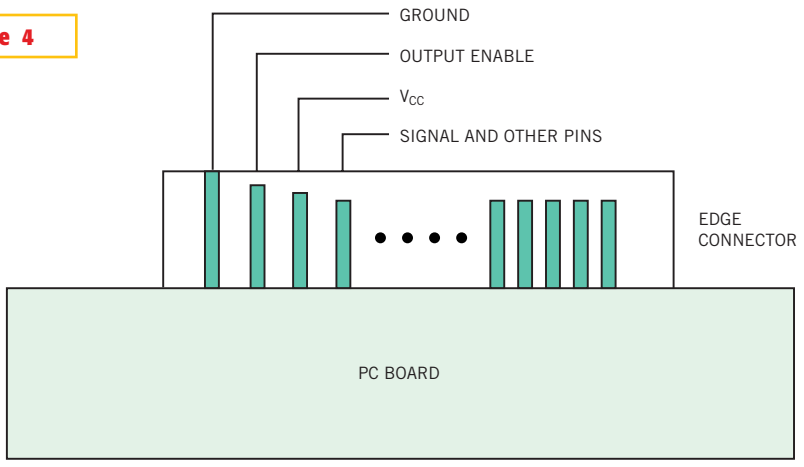
the data sheets) provides the second level of isolation required for live insertion. ABT, LVT, and ALVT families have this feature. ABTE products provide this level of isolation by having internal pull-up resistors that disable outputs during power-up and power-down.

During power-up, Q_1's collector follows V_{CC},which the input of the NOR gate interprets as a high. This high disables the output buffer regardless of the voltage on the output-enable $\overline{OE}$ or data-input pins. As V_{CC} rises, the Q_1 base-to-emitter junction becomes forward biased. Q_1 turns on, pulling low Q_1's collector and the input of the NOR gate. Depending on the level of the output-enable pin, you can now enable or disable the output buffer. The V_{CC} threshold that turns on Q_1 is 2.1V for ABT devices and 1.2V for LVT and ALVT devices. At greater voltages, the output-enable pin takes control of the high-impedance mode; therefore, you must control the enable pin to guarantee a three-state condition.

During power-down, Q_1 at first remains on, keeping the input to the NOR gate low. When V_{CC} drops below the specified threshold, Q_1 turns off, and the power-up/-down circuit keeps the output buffer disabled.

To guarantee high-impedance outputs during the full ramp-up or -down of V_{CC}, connect the negatively asserted output-enable pins to V_{CC} through an external pullup resistor. For positively asserted output-enable pins, use a pulldown resistor to ground. You can also use these methods with the previously discussed logic families that meet the first level of isolation.

Figure 4



This staggered-pin arrangement of the edge connector's pins ensures that ground connects first to the pins of the mating connector. The output-enable pin contacts the pins next to control disabling the outputs. Then, V_{CC} connects. Finally, the signal and other pins make contact.

PROTECTING CIRCUITRY

When you insert a card into a connector, the ground pins need to make contact first with the ground pins of the connector. This sequence prevents current from flowing from the powered pc board through unexpected return paths (phantom grounds) in the unpowered pc board. **Figure 3** shows how an unconnected ground to the unpowered pc board could allow current to flow from V_{CC} to an output. Devices that have output clamp diodes to ground can present a return path to the powered device. Excessive current may flow through the diode.

One simple way to implement a leading ground connection is with a staggered-pin arrangement of the edge connectors (**Figure 4**). To control disabling the outputs, the output-enable pin should connect next, followed by V_{CC} and, finally, the signal and other pins.

BUS GLITCHES

When you insert an unpowered pc board into an active backplane, the pc board's capacitance charging through the line impedance of the backplane's bus, causes a glitch. This glitch occurs even though an unpowered driver's output is off and in a high-impedance state. If the amplitude and width of the glitch are sufficient, a receiver can interpret the glitch as a valid signal and bus errors can occur. **Figure 5** shows a capacitive approximation that models a live-insertion event.

C is the capacitance of the unpowered pc board's driver, traces, and connector. V_I is the initial voltage of the pc-board connector pin. V_Q is the quiescent voltage on the backplane before live insertion. R_{EQ} is the effective backplane impedance with other cards inserted. The

glitch amplitude at the backplane is:

$$V(T) = V_Q - (V_Q - V_I)e^{\frac{-T}{R_{EQ}C}}.$$

Therefore, the glitch pulse width in the receiver's threshold-input region is:

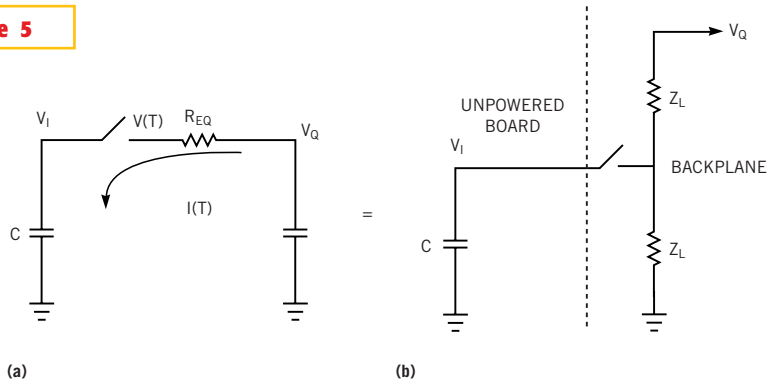
$$T = L_N\left(\frac{V_Q - V_{TH}}{V_Q - V_I}\right)R_{EQ}C.$$

Figure 6 shows the waveform of the live-insertion glitch. The size and duration of the glitch depends partially on the voltage difference between the backplane and the pc-board pin. To minimize this difference, you can apply a precharge voltage to the backplane side of the bus as you insert the pc board into the active bus. Because the backplane's voltage level, V_Q, can be either a high or a low, a precharge voltage near the middle of those levels is the best choice.

The glitch's width also depends on the RC time constant of the backplane's impedance and the combined capacitance of the driver, traces, and connector. Keeping the driver's output capacitance low can reduce the glitch's width.

Products that include precharge circuitry are BTL families, such as FB and FBL, which are used in BTL backplanes. ABTE products also have precharge circuitry. The ABTE family complies with the VME64 ETL specification. All of these products that have the precharge circuitry meet the third level of isolation for live insertion.

Figure 5



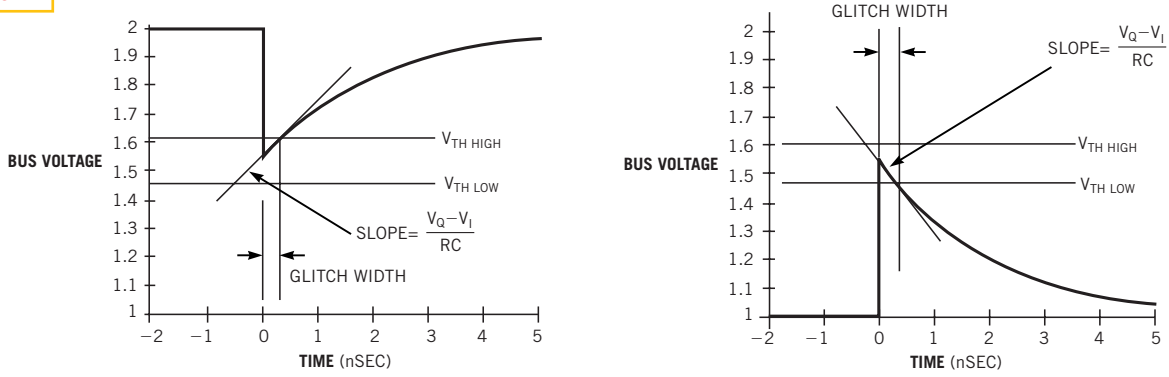
The capacitive approximation in (a) can model the live-insertion event in (b). C is the capacitance of the unpowered pc board's driver, traces, and connector. V_I is the initial voltage of the pc board's connector pin. V_Q is the quiescent voltage on the backplane prior to live insertion. R_{EQ} is the effective backplane impedance with other cards inserted.

You can use bus switches as an alternative to logic devices for live insertion. Bus switches are becoming popular devices to provide a hot-plug interface when drive current is not needed, and they require only a fast bus connect/disconnect. Philips Semiconductors' (www.philips.com) CBT6800 and CBT6810 are 10-bit bus switches, and the CBT6820 is a 20-bit bus switch. All three switches have precharge output circuitry for glitch reduction, and the CBT6810 and the CBT6820 include Schottky clamp diodes for undershoot protection. You can use these parts for PCI hot-plug applications. Other suppliers, such as Texas Instruments, Integrated Device Technology, Pericom, and Fairchild, offer bus switches as part of their portfolios that include the precharge circuitry for hot plugging.□

AUTHOR'S BIOGRAPHY

Mike Magdaluyo has worked in the electronics industry for 23 years at Underwriters Laboratories and Philips Semiconductors. He has worked as a lab technician, technical-report writer, product engineer, and quality engineer. He is currently an application engineer in the Logic Products Group at Philips Semiconductors. Mike has a BS in Industrial Technology from San Jose State University (San Jose, CA). He enjoys weightlifting, autocross racing, music, Latin dancing, and bike riding.

Figure 6



Using the equations derived from the model in Figure 5, these graphs illustrate how a glitch from a live insertion–if it persists long enough–can look like a valid signal to the system.