APPLICATION NOTE 103 - THE dbx 2150 VOLTAGE CONTROLLED AMPLIFIER

I. DESCRIPTION

A. GENERAL

The dbx 2150 integrated circuit VCA is a current in, current out device with a voltage sensitive control port. Both positive and negative control ports are available. The recommended supply voltage is ±12V. However, non-symmetrical supplies and other voltages may be accommodated.

B. INPUT

The input port of the VCA (pin 1) is a virtual ground which accepts current determined via an external resistor. The input port must be AC coupled in order to insure that DC offsets of the preceding stages will not be varied by the varying gain of the VCA. The input port must be connected to a source impedance of less than 20kΩ at high frequencies (above 100 kHz) in order to insure stability. Maximum input current varies with the gain setting and the bias current programmed. At the recommended biasing levels (3mA) the maximum input current should not exceed 1.5 mA instantaneous.

C. OUTPUT

The output of the VCA (pin 8) must be connected to a virtual ground for proper operation. An op-amp is used to convert the VCA output current into a voltage. The feedback network of this op-amp must contain a small capacitor, connected directly between the VCA output and the op-amp output for stability.

Any op-amp of convenience may be used as the current-to-voltage converter; a bi-fet type is suggested where only high impedance loads are to be driven, a 5534 type (unity gain compensation) where 600Ω loads are to be driven.

D. CONTROL

The control port takes the form of three pins (2,3,4) which allow positive gain with positive voltage (pins 2 and 4), negative gain with positive voltage (pin 3), and symmetry adjustment (applying a voltage, differential between pins 2 and 4). Pins 2 and 3 should be sourced from a low impedance (<1Ω), Pin 4 should be sourced from 50Ω impedance. The control ports present a high impedance load to the driving circuit.

The control constant is +6mV/dB on pins 2 and 4, and -6 mV/dB on pin 3. This constant has a temperature coefficient of 0.33%/^{o}C.

E. CURRENT PROGRAMMING

The bias current in the VCA IC is set by a resistor from pin 5 to the negative supply. The voltage at pin 5 is normally four diode drops below ground. Nominal bias is 3mA, so with a -12V negative supply, the bias setting resistor is usually 3.3kΩ.

The VCA is capable of going into a latch-up mode if the negative supply voltage is removed when positive supply is present. To prevent this latch up,a circuit is attached to pin 5 which prevents the voltage at pin 5 from going above its nominal -4V_{BE} level. The circuit is described in the (II) CIRCUIT IMPLEMENTATION section of this note. Several VCAs may be served by one circuit.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows the basic VCA IC configuration. R_1 and C_1 provide voltage-to-current conversion and AC coupling of the signal input to the VCA. Additionally, the source impedance is 20kΩ at high frequencies, as required for stability. The input node, pin 1, is a virtual ground, accepting an input current only.

The maximum input current is determined by the input impedance and the input voltages expected. Since output clipping may take place for small input currents with large gains, care must be taken when scaling the input network that total input plus output currents are no greater than $\frac{I_{BIAS} - 0.5mA}{1.4}$ Amps RMS.

B. OUTPUT

The output terminal (pin 8), provides a high impedance current output equal to the desired gain times the input current. To convert this signal to a voltage, pin 8 is connected to the summing junction of an op-amp, as shown in Fig. 1. The feedback resistor around this op-amp, R_3, determines the constant of current-to-voltage conversion taking place.

C_3 is necessary to prevent oscillations of the output op-amp due to the capacitance between pin 8 of the VCA IC and ground. C_3 is normally 33pF, as shown. A small resistor (e.g. 47Ω) may be added between C_3 and R_3 as drawn, and the output taken from the junction of R_3 and C_4. This connection provides isolation from capacitive loads at the output of the op-amp.

C. SUPPLY CONNECTIONS

Pin 7 should be connected directly to the positive supply (nominally +12 V) as shown in Fig. 1. Pin 5, the negative supply terminal for the IC, must be supplied with a current to program the internal bias network. The nominal value of this current is 3mA, but if reduced signal handling capacity is acceptable this current may be reduced proportionate to the allowable reduction in headroom.

Since the maximum voltage which may be applied across the IC is 30V, supply voltages of up to ±24V can be accommodated by appropriate scaling of R_5, R_8, and the R_6/R_7 voltage divider.

The action of the anti-latch circuit is to draw current from pin 5 when the voltage at pin 5 rises high enough to forward bias the Base-Emitter junction of Q_1. Since the normal voltage at pin 5 is ~-2.2V, and the R_6, R_7 network establishes a voltage of -2.55V at the base of Q_1, normally Q_1 and Q_2 are turned off. If, however, the VCA begins to latch, the pin 5 voltage rises as current is internally diverted into the output (pin 8). Q_1 senses this voltage rise and responds by turning on Q_2, drawing enough current from pin 5 to prevent the latch from establishing itself.

The anti-latch circuit may be shared between many VCA ICs. The circuit of Fig. 2 shows the necessary changes to the Q_1 base bias network required to compensate for the added voltage drop of the diodes D_1 - D_n.

D. GAIN CONTROL

Fig. 1 shows the basic configuration with positive voltage causing negative gain. The point labeled E_C accepts control voltage from a low impedance source (<1Ω). Higher source impedances will cause distortion of high level input signals. The opposite control sense is available by grounding pin 3 and applying the gain control signal to pin 2 and the grounded end of R_9. Both senses of control may be used simultaneously.

The R_8, R_9, R_{SYM} network allows adjustment of the relative gain of positive versus negative input currents, thereby controlling. second harmonic distortion. Since pin 2 is always connected to a low source impedance, the setting of R_5 determines the voltage differential across R_9. For R_9 equal to 51Ω, the design center goal of a 50Ω source impedance to pin 4 is satisfied.

The gain control constant is ±6mV/dB (depending on the control port used), with a temperature coefficient of 0.33%/°C. 0dB gain (±1dB) occurs when 0V is present at the control port.

E. DC OFFSET NULLING

When very rapid gain changes are commanded from the control source, a small transient DC offset may be produced at the VCA output. This transient is due to bias shifts in the VCA IC, and may be substantially reduced by adding a single resistor from the gain control port to pin 5 of the VCA. The optimum value for this resistor has been experimentally determined to be 10kΩ. Due to the increase in current through R_5 caused by the added resistor, R_5 should be reduced to 2.7kΩ. The final circuit is shown in Fig. 3.

III. ADJUSTMENT PROCEDURE

A. SYMMETRY CONTROL

The symmetry control is set by observing the distortion in the output at a convenient signal level and unity gain, and adjusting the control for minimum 2nd harmonic distortion. A 1kHz low distortion sine wave should be applied to the input node in Fig. 1, while a distortion analyzer or spectrum analyzer is used to monitor the output of the current-to-voltage convertor op-amp. Adjust R_{SYM} for minimum 2kHz product in the output. 2nd harmonic distortion should be lower than 0.01% after adjustment.

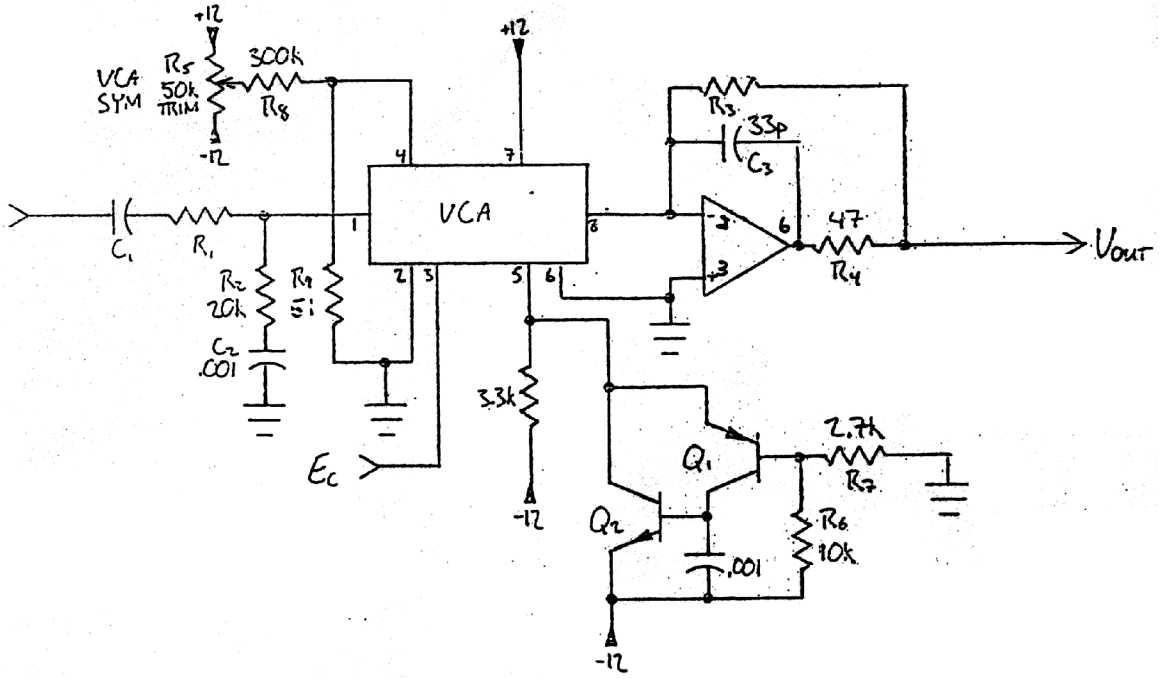

FIGURE 1. BASIC VCA CIRCUIT

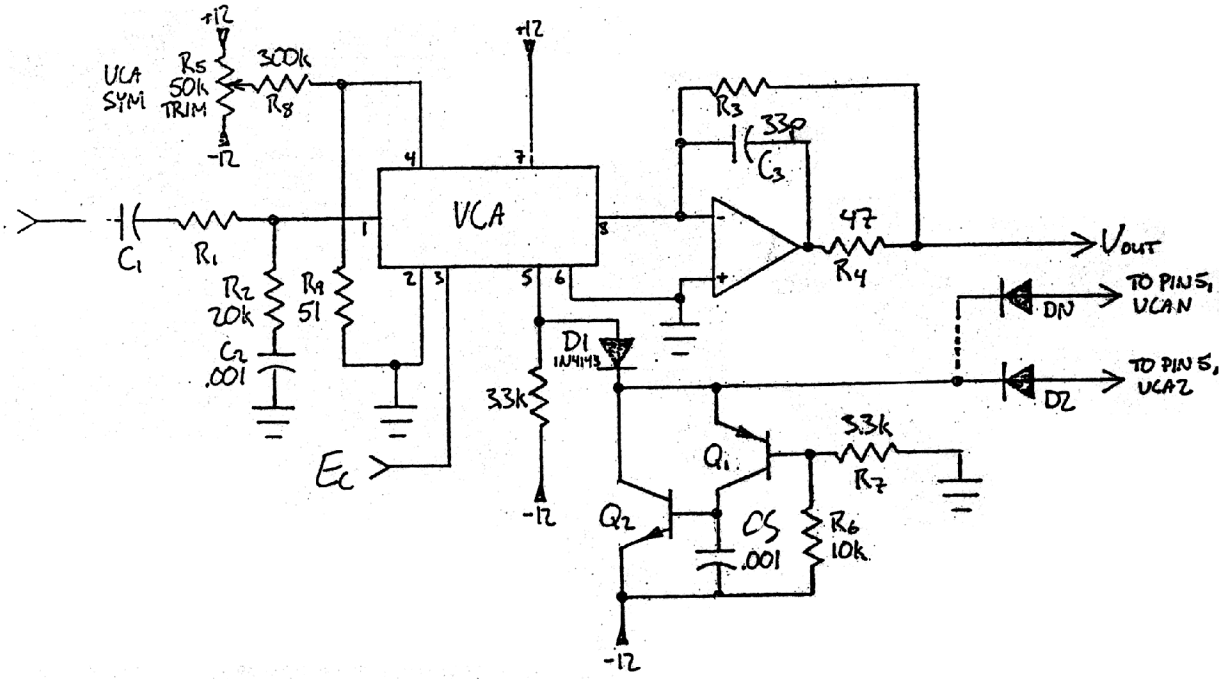

FIGURE 2. ANTI-LATCH CIRCUIT FOR MULTIPLE VCAs

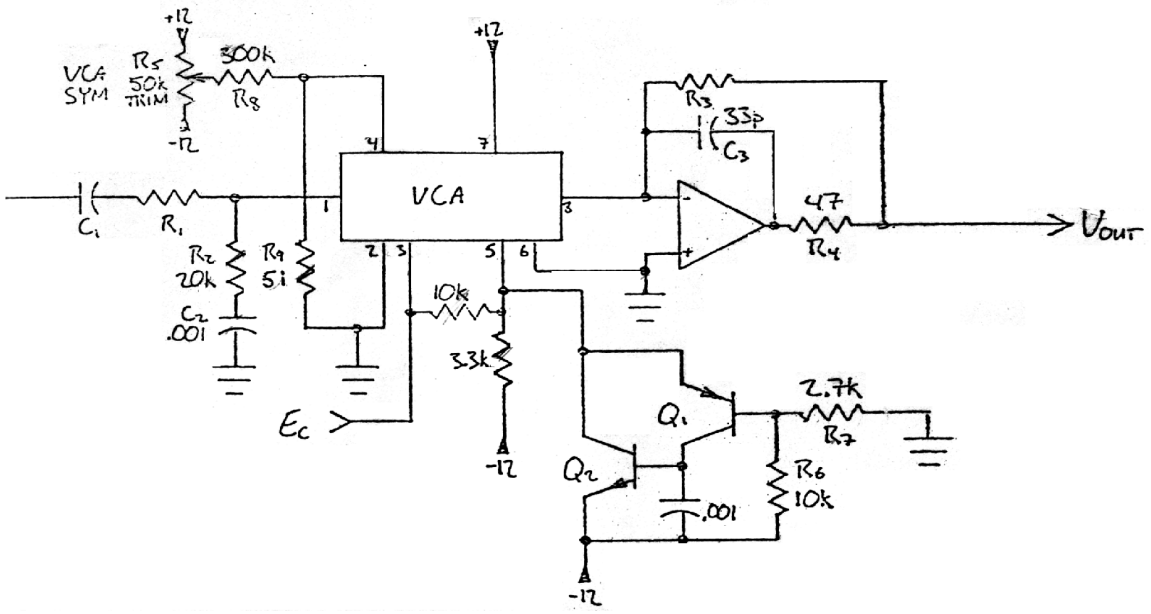

FIGURE 3. VCA CIRCUIT WITH OFFSET NULL RESISTOR

VCA PRELIMINARY SPECIFICATIONS

Power Supply	Nominal bipolar: 12V
	Absolute Max: 30V across I.C.
Gain Range	-100dB to +40dB
Gain Control Constant	+6mV/dB, -6mV/dB
Gain at Ec = 0V	0dB ±ldB
Gain Control Input R	High Z load (>5 kΩ)
	pins 3,4 to be sourced from <1Ω
	pin 2 to be sourced from <50Ω
Tracking Accuracy	±1%, -80dB to +40dB gain
Noise*	-86dBV (CCIR, +15dB programmed gain)
Frequency Response*	20Hz to 20kHz (±.5dB, -40dB to +40dB programmed gain)

*Measured with R_{IN} = 20kΩ, R_{OUT} = 20kΩ, C_{IN} = 1uF, C_{OUT} = 47pF