

### Introduction

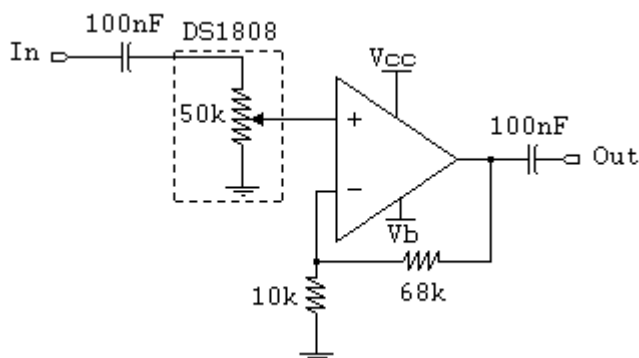
The DS1808 Dual Log Audio Potentiometer was designed to provide superior audio performance in applications that require low levels of THD and cross-talk. By utilizing a  $\pm 12\text{V}$  supply, it offers  $24\text{V}_{\text{pp}}$  of signal swing capability, and it simplifies your design by allowing the low side of the potentiometer to be referenced to ground. The DS1808 features 33 positions that provide attenuation from 0dB to 60dB, and a mute function that provides 90dB of attenuation. It is controlled by a 2-wire interface, which can address up to eight DS1808s on a single 2-wire bus. It is available in a 16-pin SOIC package.

This application note addresses both hardware and software design practices that will allow the DS1808 to work best in a customer's application. When the DS1808 is used according to these practices it is a viable solution for most audio applications.

### Basic Audio Circuit Using a Dual Supply Digital Potentiometer

There are several circuit topologies that can be used to create an audio circuit with a digital potentiometer utilizing a  $\pm 12\text{V}$  supply. Dual supply digital potentiometers can directly replace a mechanical potentiometer in most instances as long as the full range of the signal is within the supply range of the potentiometer, and the output current required at the wiper does not exceed the wiper current specification. A simple audio circuit using the DS1808 is shown in Figure 1.

Figure 1



A Basic Audio Circuit that Could be Built Using the DS1808.

This circuit will work using a DS1808 as long as the input voltages are less than  $V_{\text{CC}}$  and greater than  $V_{\text{B}}$ . The input is AC coupled from the audio source, and the output has a capacitor in series to guarantee that the output will also be AC coupled. Once the audio signal has made it past the input capacitor, it will be attenuated by the DS1808 according to how its registers have been set with the 2-wire bus. The DS1808 has a graduated logarithmic taper with 1dB steps from 0 to 12dB, 2dB steps from 14dB to 36dB, and 3dB steps from 39dB to 60dB. The last register position is mute, which provides greater than 90dB attenuation. The wiper output of the potentiometer will be amplified by a fixed gain of  $7.8\text{V}/\text{V}$  (17.8dB) by the operational amplifier. The amplifier serves as a voltage buffer, which by design keeps the wiper current of the DS1808 below the specified value of 1mA with its high impedance input.

Important notes regarding the circuit:

- The input is a high pass filter with a 3dB cutoff frequency at  $1/2\pi RC$ . In this case, the 3dB frequency is approximately 32Hz. This will noticeably attenuate the low frequency response of the audio range. Since the 50k resistance cannot be easily increased in this case, a larger capacitor could be used to place the cutoff frequency well below 20Hz, and the response due to the input portion of the circuit would be flat over the entire audible range.
- The digital potentiometer, unlike a mechanical potentiometer, can only handle signals within its voltage supply range. In the case you are using a  $\pm 12V$  supply, a 24Vpp signal swing is the maximum that the part will be able to handle. If you lower the supplies to  $\pm 5V$ , it will only be able to handle a 10Vpp signal. If  $V_b$  is grounded, the audio signal would have to remain above ground, and hence would have to carry a DC bias, usually  $V_{CC}/2$ .
- The wiper current must remain below the wiper current limit. Digital potentiometers in general cannot source much current, and the DS1808 has a wiper current limitation of 1mA. As mentioned above, the amplifier provides both the voltage buffering and wiper current limiting to ensure that this specification is adhered to.
- The operational amplifier should be chosen such that it will be able to handle the signal swing that you expect coming out of the DS1808. The amplifier will clip signals that go beyond its supply, and in the event that the amplifier is not a rail-to-rail amplifier, it could clip signals that are within the supply rails as well.
- Because there is another series capacitor between the amplifier and the output, another high pass filter will exist whose cutoff frequency will depend on the load impedance. With a 100nF series output capacitance, the load should have a high input resistance or the signal could potentially be filtered at that point. This circuit was intended to be a preamplifier circuit, and the assumption was made that the output would be going into another amplifier.

## Basic DS1808 Software

The DS1808 is controlled by a 2-wire interface that is easily implemented on a microprocessor. The hardware is simply two open collector I/O lines that are called serial data (SDA) and serial clock (SCL). These lines generally have resistive pull-ups ( $\sim 4.7k\Omega$ ) to a 3V or 5V supply that will pull the lines high during a one and when the bus is not in use. Both the microprocessor and the slave have the ability to place data on the bus, but only a bus master can control the clock rate.

Once low-level code drivers have been written to perform simple tasks such as taking control of the bus (start condition), reading and writing single bytes, handshaking by acknowledging the DS1808, and then releasing the bus (stop condition), any task can be realized that uses 2-wire devices. The DS1808 uses a simple protocol to determine if it has been addressed, and then performs the tasks associated with the commands that follow.

## DS1808 Address and Data Protocol

Since 2-wire allows multiple slaves to exist on the same bus, the protocol must allow some way to address the different parts connected to the bus. Using a unique address byte for each part allows the parts to be differentiated by the master (microprocessor). The address byte will always be the first byte transmitted when a new message is being sent so only the part intended to receive the message will respond to the communications.

The DS1808 is addressed by the address byte shown in Figure 2. Bits 7 to 3 are always “0101” or 5h. The next three bits address a specific DS1808 depending upon the state of the address pins (pins 2, 3, and 5) on the device. Since the state of the external pins can determine a unique address for up to eight DS1808s, it is possible to have up to eight DS1808s on the bus without having to add a second bus. Bit 0 determines if a

read operation or a write operation will occur. After the read/write bit, the DS1808 (slave) will acknowledge by pulling the bus low for one clock cycle. This is the master's signal that a slave has recognized its address, and is processing the information. The master must provide the clock signal according to the datasheet timing, even during the acknowledge pulses. During signaling, all bytes are sent MSB first.

**Figure 2. DS1808 Address Byte**

Bit 7 (MSB)	6	5	4	3	2	1	0	ACK
0	1	0	1	A2	A1	A0	R=1, W=0	Slave ACK

Following the address byte, data will either be sent to or from the DS1808 in the format shown in Figure 3. Bit 7 in the data byte is a place holder, and can technically be either a zero or one with no effect when writing to the part. It is a good idea to leave it zero, since it is reserved for future product releases. Additionally, the DS1808 will always write a zero for this bit when a read operation is performed. Bit 6 is the potentiometer select bit. It will select which potentiometer will be addressed within the DS1808. If it is a zero, potentiometer zero will be addressed, and if it is a one, potentiometer one will be addressed. Bits 5 to 0 will set the potentiometer's position. There are a total of 64 available positions, but the potentiometer only uses the first 34 positions as described above. The remaining positions from 34 to 63 are all equivalent to the mute position. Since the potentiometer select bit determines which potentiometer is being written to it is not necessary to write to both potentiometers during a write attempt. Both can be written to if it is required by the application. The acknowledge pulse is always generated by the device receiving the information. Thus, during a write the slave will acknowledge the master, and during a read the master must acknowledge the slave.

**Figure 3. DS1808 Potentiometer Control Byte Contents**

Bit 7 (MSB)	6	5	4	3	2	1	0	ACK
0	Pot0 = 0, Pot1 = 1	Data						ACK (NACK last byte during read only)

## Writing to a DS1808

A start condition initiates a transaction on the 2-wire bus. A start condition occurs whenever SDA is pulled low while SCL remains high. This is done on purpose at the beginning of a data transmission, but should be avoided until the next time a data transmission is to begin because it will confuse the slave (DS1808). Next, the address byte is written out, most significant bit first, with the timing shown in the datasheet. Since a write operation is being performed, the last bit of the address byte should be a zero. The slave will acknowledge the master, and the master will send one more clock pulse to clock the acknowledge bit. The data is then written out MSB first, and as long as the Fast Mode timing is followed (see data sheet), data rates up to 400kHz can be obtained. After each data byte is written to the slave, the slave will pull the bus low (acknowledge) for one clock cycle (the master clocks all bits, including acknowledge bits) if it is correctly receiving the data. The slave will then release the bus, and the master can continue to send the next data byte. After the last data byte is sent, the slave will acknowledge, and the master generates a stop condition by releasing SDA to go high while SCL is already high. The stop condition will complete the write sequence.

## Reading from a DS1808

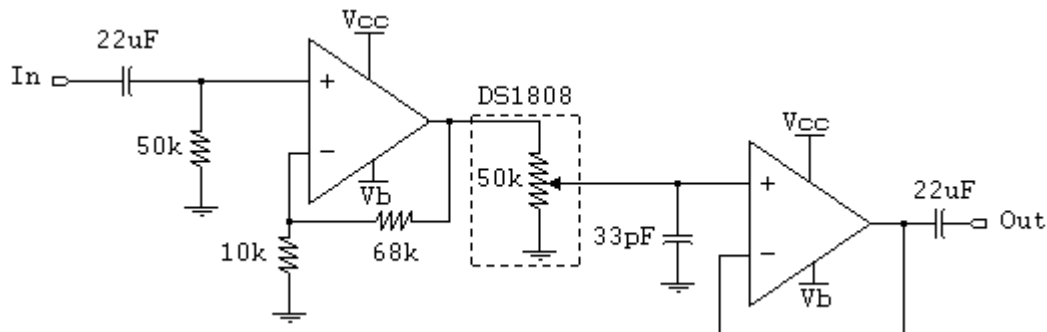
A start condition also initiates a read operation. The part is then addressed with the last bit of the address byte being a one, and the slave will acknowledge the address byte as before. During a read, the slave will place data on to the bus, but it is still the master's (microprocessor) responsibility to clock the bus. The master must also generate an acknowledge every ninth bit (acknowledge clock cycle) during the data transfer if and only if it is going continue to receive data from the slave after the current byte. Once the last byte is received, the master performs a NACK (not acknowledge, clock the bus while SDA is high.) The NACK informs the slave that the master has received all the data that it desires, and the slave should expect a stop condition to follow. Finally, the master will terminate the sequence by generating a stop condition.

## In Depth Look at Designing for the DS1808

The DS1808 is a low THD and cross-talk audio potentiometer. It boasts a Typical THD of 0.0006%, and a typical cross-talk of -105dB at 20kHz. The drawback to the part is that it lacks a zero crossing detector for pop-free switching. This is most evident when making large V/V attenuation changes, and is nearly undeletable with a good hardware design and when the part is changed in single position increments.

Below is a hardware design that has been used with good success. There are a couple of features that make this design work well with the DS1808. The main items are that the gain is present before the DS1808, so any switching noise that may exist will not be amplified by the gain stage. Second, a small capacitor has been placed from the wiper to ground, and it will help to filter any switching noise that may exist. The low pass filter created by the potentiometer and the 33pF capacitor has a 3dB cutoff frequency of approximately 96kHz, so it will not affect the audio frequency response of the circuit.

Figure 4. Practical DS1808 Audio Circuit



This circuit has the same input signal limitations (signal must be between the supply rails or audio signal may be clipped) as the circuit shown in Figure 1; however, it will be a better sounding audio system. Because the operational amplifier has a high impedance input, the 50k $\Omega$  resistor to ground behind the input capacitor is required to provide a DC bias for the input of the amplifier. Without the resistor, the input can float to a non-zero level. It is possible for it to float all the way to a supply rail, and that will cause the audio signal to be clipped. This was not required for the previous circuit because its input had a connection to ground through the digital potentiometer.

Since this particular potentiometer does not have a zero crossing detector, and because the volume changes occur instantaneously, it can cause a popping sound when you change the volume via software. This phenomenon is most apparent when you attenuate the signal a between 0 to 6dB, because the magnitude of the voltage change at lower levels of attenuation is greater in spite of the same V/V signal change. Figures 5 to 7 show the dynamics of switching an audio signal. All three figures show the effects when the audio input is a sine wave. Figure 5 shows the step change that can occur when a large V/V attenuation change is made.

Figure 5

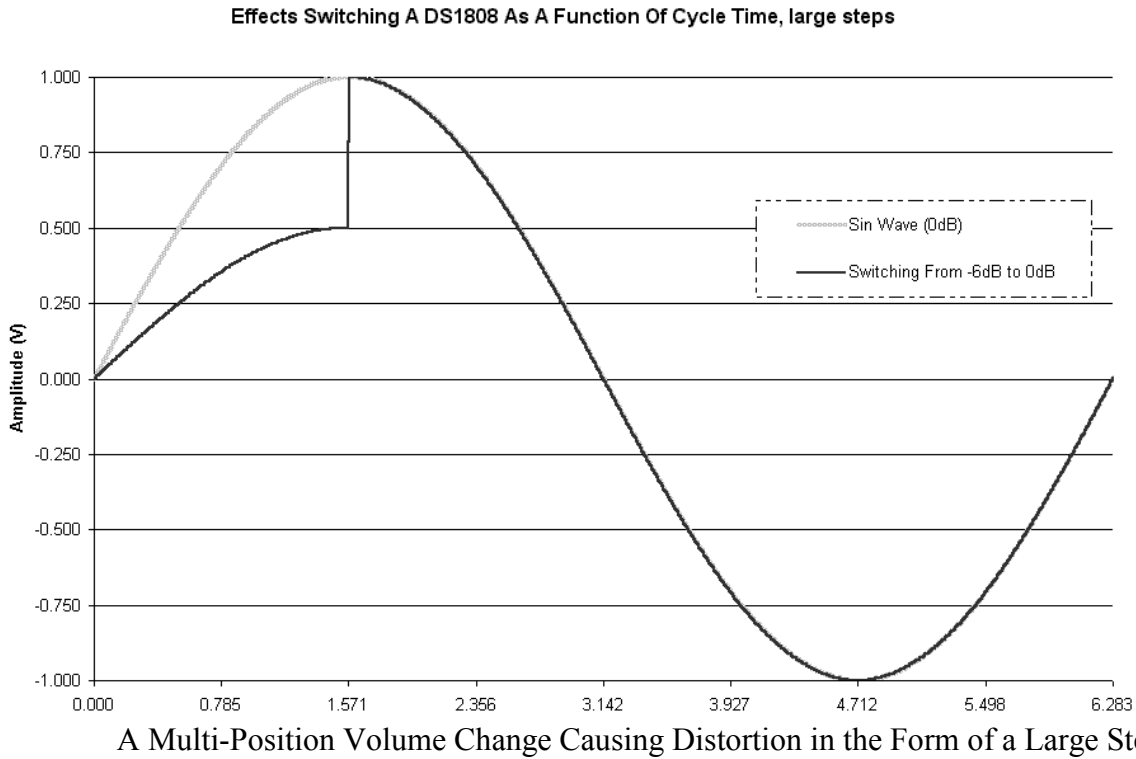


Figure 6 shows a 1dB change from  $-1\text{dB}$  to  $0\text{dB}$ . The potential step change that will be made can be seen in this diagram by looking at the difference between the before and the after signal. If the change is made at a random time, the difference could be as much as 11.2% of the audio signal. This would occur if the change is made while the sine wave is at its full scale (at 90 or 270 degrees) value. It is also possible that the signal's disturbance could be as small as zero if the change is made at 0 or 180 degrees. Zero crossing detectors guarantee that the signal will be at zero when the switch occurs, and hence eliminates the popping. Since this part does not have a zero crossing detector, the next best thing is to avoid large V/V signal changes by administrating limiting the changes to single position increments.

Figure 7 shows a typical mid-attenuation signal change. By observing the difference function that represents the potential step change, it would appear that the consequences for changing the attenuation while in the mid-attenuation range are somewhat benign. However, the signal is still subject to downstream amplification. This seemingly subtle change may be very noticeable if it is followed by a 60dB gain stage. It will always be a less significant change than the  $-1$  to  $0\text{dB}$  step change in the same system, but it is something to keep in mind when designing an audio system.

Figure 6

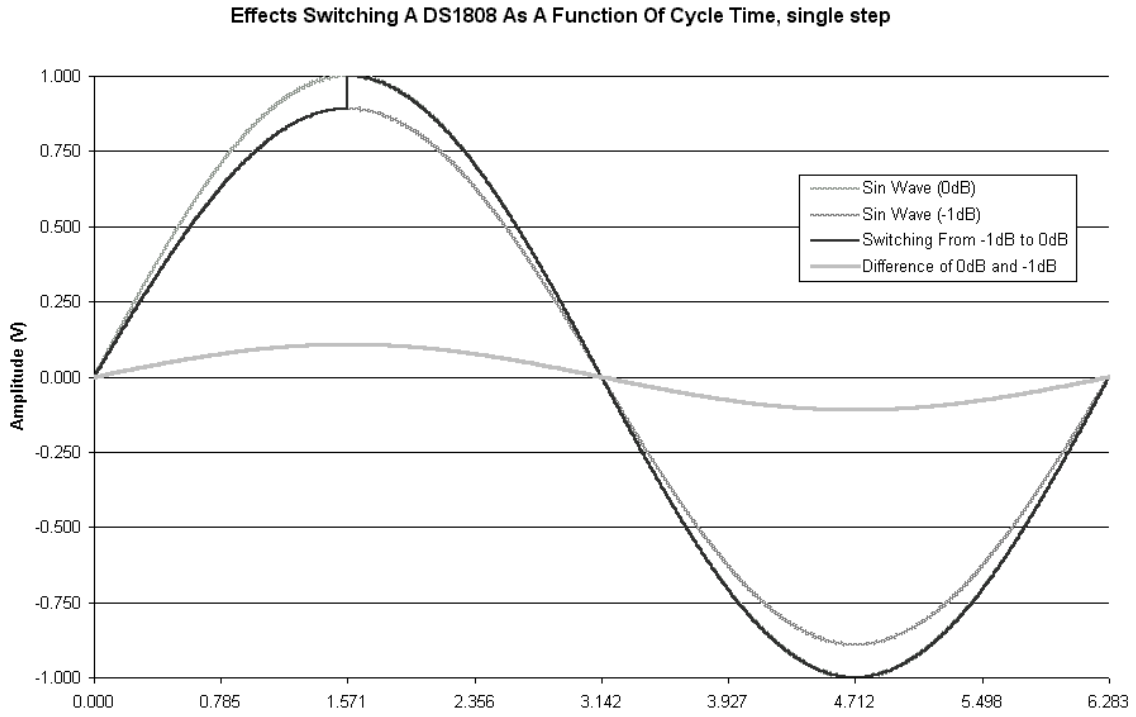
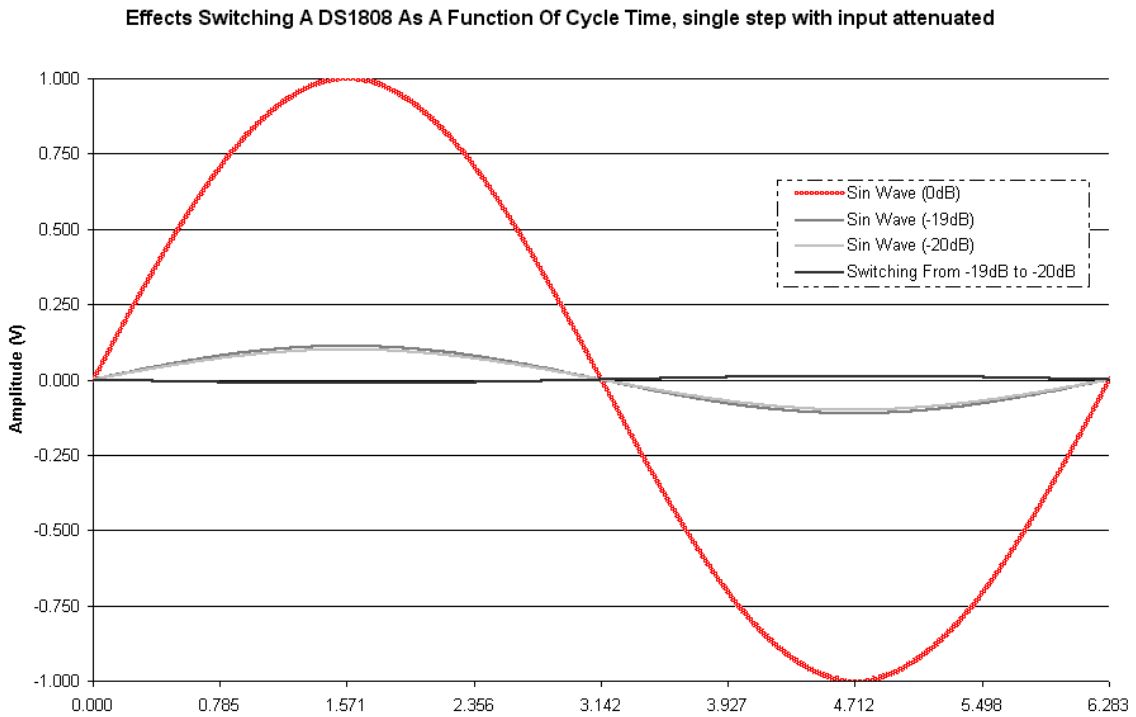


Figure 7



One additional thing to consider is that when a microcontroller is being used change the attenuation, it is possible to make the change from zero attenuation to full attenuation in as little as a few milliseconds while only moving one position at a time. Since it is such a relatively short period of time, the listener will believe that the volume was cut instantaneously. Thus, if possible, it is a recommended practice to make 1dB steps with this particular part.

## Summary of DS1808 Audio Design Guidelines

In most systems, it is preferable to place the DS1808 downstream of the system's amplification. This puts any switching noise downstream of the amplification, and the signal to noise ratio of the system will benefit from this architecture. A small capacitor from the wiper to ground can also be used to filter out some of the switching noise.

Additionally, the DS1808 does not contain a zero-crossing detector. Because of this, it is desirable to change the volume in 1dB increments and decrements. This will avoid large V/V signal changes that may cause a very noticeable pop when the volume is changed.

In the event that you are in need of a similar part with a zero-crossing detector, please contact customer service and ask to speak with an applications engineer about the DS1808. It is a potential future product, and we would be interested in knowing if we have customers that could benefit from the additional functionality. The Maxim/Dallas customer service number is listed below.

## Maxim Integrated Products / Dallas Semiconductor Contact Information

### *Company Addresses:*

Maxim Integrated Products, Inc  
120 San Gabriel Drive  
Sunnyvale, CA 94086  
Tel: 408-737-7600  
Fax: 408-737-7194

### *World Wide Web Site:*

[www.maxim-ic.com](http://www.maxim-ic.com)

### *Product Information:*

<http://www.maxim-ic.com/MaximProducts/products.htm>

Dallas Semiconductor  
4401 S. Beltwood Parkway  
Dallas, TX 75244  
Tel: 972-371-4448  
Fax: 972-371-4799

### *Ordering Information:*

<http://www.maxim-ic.com/BuyMaxim/Sales.htm>

### *FTP Site:*

<ftp://ftp.dalsemi.com>

### *Product Literature / Samples Requests:*

(800) 998 – 8800

### *Sales and Customer Service:*

(408) 737 - 7600