This digital potentiometer circuit is a hybrid analogue and digital design offering push-button controlled programmable attenuation as well as high to low impedance conversion by means of a single active device. Digital noise is eliminated as effectively as possible through galvanic isolation of digital and analogue parts in the input attenuator.

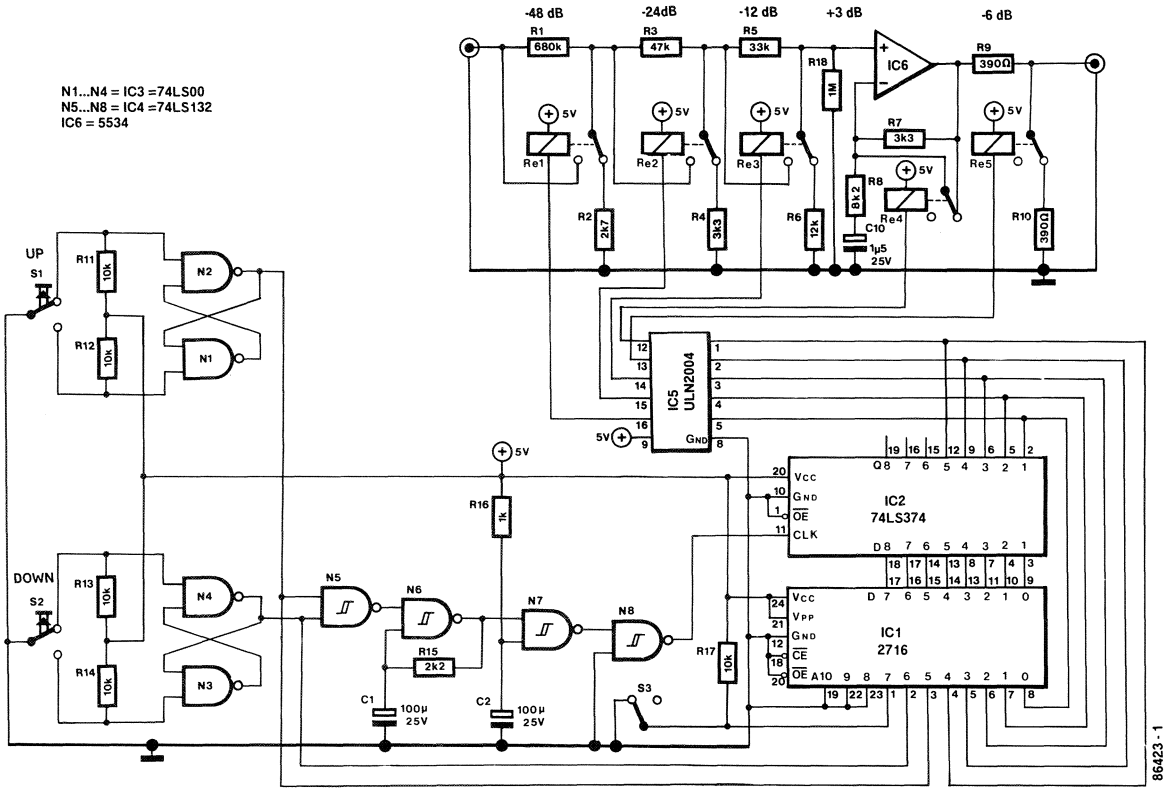
At the heart of the digital control section is a Type 2716 EPROM, which can be programmed either as shown in Table 1 or to individual requirements, as will be detailed below. At power-on, debouncer bistables N_1-N_2 and N_3-N_4 force logic low levels onto EPROM address lines A_5 and A_6 respectively, selecting a programmed address range that supplies the digitally coded, initial volume settng. R-C network R_{16}-C_2 causes gates N_7 and N_8 to generate a clock pulse for IC_2, which latches the 8-bit word from IC_1, passes this information to driver IC_5, and thus determines which relay(s) is/are energized, thereby fixing the attenuation before the AF signal is applied to opamp IC_6. Depression of S_1 (up) or S_2 (down) causes the corresponding address line A_5 or A_6 to go low, selecting a certain address range in the EPROM. The exact address location is determined by the value last latched into IC_2 after either key has been released. It is readily seen that the five available databits at the $Q_1 \ldots Q_5$ outputs of IC_2 allow 32 (2^5) simulated potentiometer settings.

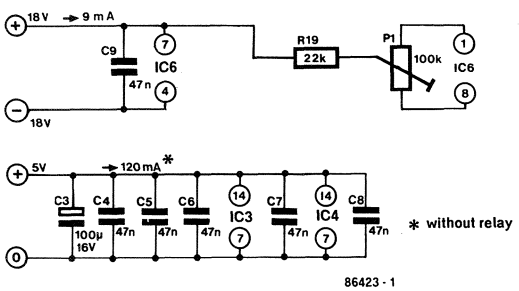
The digital control section has been designed to offer an auto-repeat function when either one of the step control keys is kept depressed; oscillator gate N_6 then provides a clock pulse train to N_7-N_8, and so causes successive addresses in IC_1 to be scanned automatically, until either the lowest or highest possible volume setting is reached, at which moment the circuit forces itself to a hold state, which can also be selected at any time by simultaneously depressing the up and down key.

S_3 enables the user to select a further address block, programmed with another set of volume steps; the circuit as shown, along with the data from Table 1 arranges for 3 dB steps.

Table 1

0000	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
0010	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0020	00	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
0030	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E
0040	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
0050	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	1F
0060	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E
0070	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E
0080	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
0090	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
00A0	00	00	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D
00B0	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
00C0	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
00D0	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	1F	1F
00E0	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E
00F0	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E





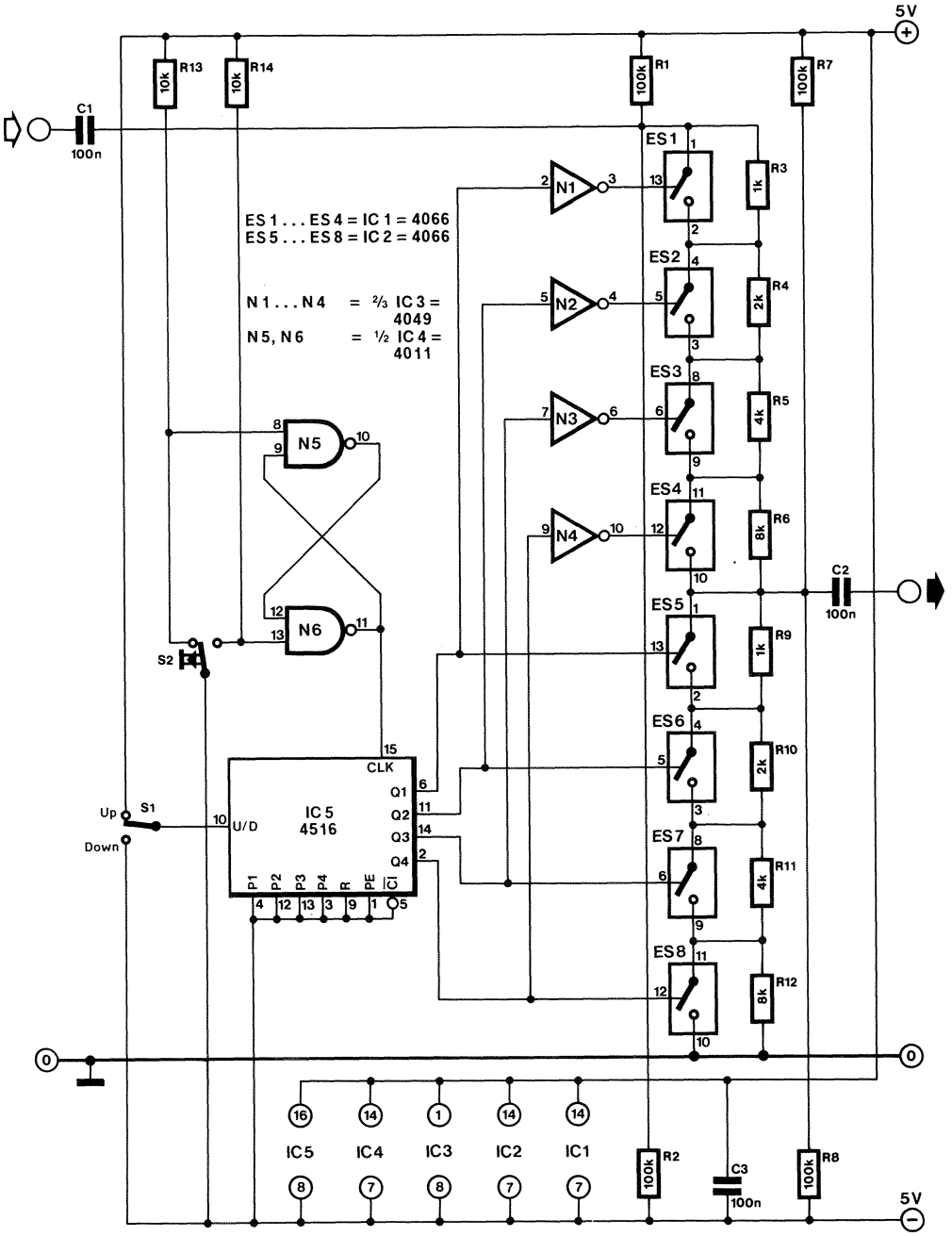
The analogue section of the circuit is basically a four-section, relay-controlled attenuator composed of resistor networks to achieve a signal attenuation in 3 dB increments, as defined with the relevant bit pattern at the $Q_1 \ldots Q_5$ outputs of IC_2. Re_4 (Q_5), if deactivated, enables IC_6 to amplify its input signal by 3 dB. The inset resistor and preset combination may be used take over the function of C_{10}, since the latter should be a high stability foil type, which may be a rather difficult to obtain part. Both circuit alternatives function as click suppressors when stepping through the available range of volume settings. The preset, if used, should be set for zero offset voltage at pin 6 of the opamp; replace C_{10} with a wire link.

It is suggested to use miniature DIL relay types in the $Re_1 \ldots Re_5$ positions, while all resistors in the attenuator are preferably close tolerance (1%), high stability types. Also observe that the supply voltages to analogue and digital section are kept well apart and decoupled so as to preclude introducing switching pulses and digital interference in the sensitive attenuator sections as well as the opamp output stage.

Finally, Table 1 offers a suggestion for programming the EPROM with data to achieve circuit operation as set out above.

008 DIGITAL VOLUME CONTROL II

Many of today's hi-fi amplifiers feature a "clicking" volume control, but this is only rarely a real stepped attenuator based on a wafer switch. In nearly all cases, this expensive system is based on a normal potentiometer, whose spindle is fitted with a mechanical construction to simulate the stepping movement. A normal rotary switch is not suitable for adjusting the volume of an amplifier because it briefly



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disconnects the input from the signal source when operated, and so readily gives rise to clicks and contact noise.

Different problems crop up when designing an electronic volume control. Of these, distortion is probably the hardest to master, but reasonable results are still obtainable, as will be shown here.

Basically, there are two methods for making an electronic potentiometer. One is to create a tapped resistor ladder (which is not much different from a normal potentiometer), the other is to change the resistance of the two "track sections" such that the total resistance remains constant. The circuit proposed here is based on the second method, and features 16 steps in its basic form. The number of steps can be increased to, say, 64 by adding four switches and resistors.

The electronic potentiometer is composed of two equal sections, which have a total resistance of 15 kΩ each. The electronic switches in each section are controlled by binary counter IC_5. Since the switches in section ES_1-ES_4 and those in ES_5-ES_8 are controlled in complementary fashion, the total resistance of the potentiometer remains constant. Resistors R_1-R_2 and R_7-R_8 serve to keep the potential at the input and output at 0 V so as to preclude clicks when the step switch, S_2, is operated. Switch S_1 is the up/down selector. Gates N_5-N_6 form a bistable to ensure that the counter is clocked with debounced step pulses.

The number of steps can be increased by adding a counter and the required number of electronic switches, divided over the two "track sections". These switches are then connected in parallel with resistors whose values correspond to binary order 1-2-4-8, etc., as shown in the circuit diagram. Fortunately, precise binary ratios are not required here, since adequate results are obtainable with approximations of the theoretical resistance values, and as long as the actual resistors are kept equal in both sections.