DS1846
NV Tri-Potentiometer, Memory and MicroMonitor

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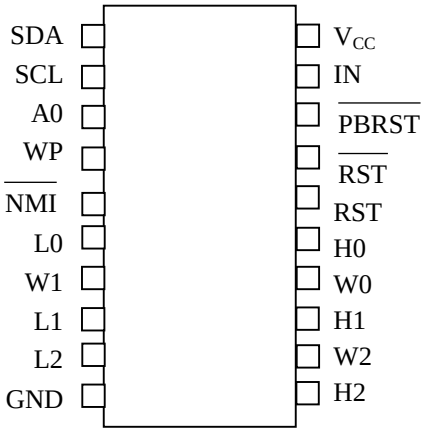
FEATURES

- Three linear taper potentiometers
  - Two 10 kΩ, 100 position
  - One 100 kΩ, 256 position
- 256 bytes of EEPROM memory
- Monitors microprocessor power supply, voltage sense, and external override
- Access to data and potentiometer control via a 2-wire interface
- External Write Protect pin to protect data and potentiometer settings
- Nonvolatile wiper storage
- Operates from 3V or 5V supplies
- Packaging: 20-pin TSSOP
- Industrial operating temperature: -40ºC to +85ºC
- Programming temperature: 0ºC to +70ºC

PIN ASSIGNMENT



20-pin TSSOP

PIN DESCRIPTION

V_{CC}	-	3V or 5V Power Supply Input
GND	-	Ground
SDA	-	2-wire Serial Data Input/Output
SCL	-	2-wire Serial Clock Input
WP	-	Write Protect Input
A0	-	Address Input
H0, H1, H2	-	High-End of Potentiometer
L 0, L1, L2	-	Low-End of Potentiometer
W0, W1, W2	-	Wiper Terminal of Potentiometer
$\overline{\text{PBRST}}$	-	Push Button Reset Button
$\overline{\text{NMI}}$	-	Non-maskable Interrupt
IN	-	Voltage Input
$\overline{\text{RST}}$	-	Active Low Reset Output
RST	-	Active High Reset Output

OVERVIEW

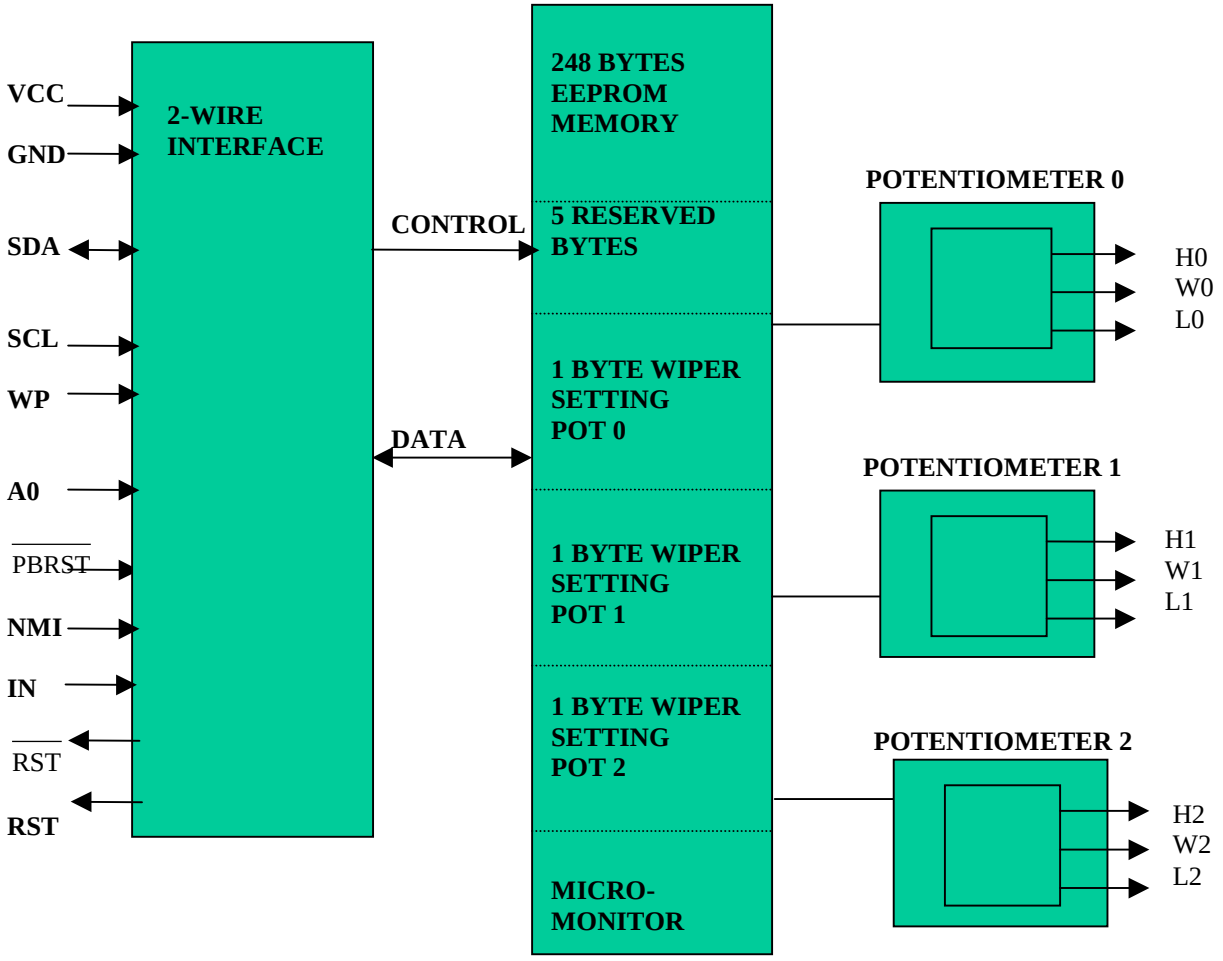
The DS1846 NV Tri-Potentiometer, Memory and MicroMonitor consists of two 10 kΩ, 100-position linear taper potentiometer, one 100 kΩ, 256-position linear taper potentiometer, 256 bytes of EEPROM memory, and a MicroMonitor. The device provides an ideal method for setting bias voltages and currents in control applications using a minimum of circuitry.

The EEPROM memory allows a user to store configuration or calibration data for a specific system or device as well as provide control of the potentiometer wiper settings. Any type of user information may reside in the first 248 bytes of this memory. The next three bytes of memory are for potentiometer settings and the top five addresses of EEPROM memory are reserved. These reserved and potentiometer registers should not be used for data storage. Access to this EEPROM is via an industry standard 2-wire bus. The interface I/O pins consist of SDA and SCL. The wiper positions of the DS1846, as well as EEPROM data, can be hardware write-protected using the Write Protect (WP) input pin.

The MicroMonitor is a precision temperature-compensated reference and comparator that monitors certain vital status conditions for a microprocessor. When a sense input detects an out-of-tolerance Vcc condition, a non-maskable interrupt is generated. As the voltage at the device degrades, an internal power fail signal is generated that can be used to reset the processor. When Vcc returns to an in-tolerance level, the reset signal is kept in the active state for a minimum of 130 ms to allow for the stabilization of the power supply and the microprocessor. The MicroMonitor also functions as a pushbutton reset control. The pushbutton input is debounced internally and is generated with an active pulse width of 130 ms minimum.

Additionally, the DS1846 will operate from 3 volt or 5 volt supplies. One package option is available: 20-pin TSSOP.

DS1846 BLOCK DIAGRAM Figure 1



PIN DESCRIPTIONS

V_{CC} - Power Supply Terminal. The DS1846 will support supply voltages ranging from +2.7 to +5.5 volts.

GND - Ground Terminal.

SDA - 2-wire serial data interface. The serial data pin is for serial data transfer to and from the DS1846. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces.

SCL - 2-wire serial clock interface. The serial clock input is used to clock data into the DS1846 on rising edges and clock data out on falling edges.

WP - Write Protect. Write Protect must be connected to GND before either the data in memory or potentiometer wiper settings may be changed. Write Protect is pulled high internally and must be either left open or connected to Vcc if write protection is desired.

A0 - Address Input. This input pin specifies the address of the device when used in a multi-dropped configuration. Up to two individual DS1846s may be addressed on a single 2-wire bus.

H0, H1, H2 – These are the high-end terminals of the potentiometers. For the three potentiometers, it is not required that these terminals be connected to a potential greater than the low-end terminal of the potentiometer. Voltage applied to the high end of the potentiometers cannot exceed the power supply voltage, V_{CC}, or go below ground.

L0, L1, L2 – These are the low-end terminals of the potentiometers. It is not required that these terminals be connected to a potential less than the high-end terminals of the pot. Voltage applied to the low end of the potentiometers cannot exceed the power-supply voltage, V_{CC}, or go below ground.

W0, W1, W2 - Wiper of the potentiometer. This pin is the wiper terminal of the potentiometer. Three bytes in EEPROM memory locations F8h, F9h and FAh determine each wiper's setting. Voltage applied to either wiper terminal cannot exceed the power-supply voltage, V_{CC}, or go below ground.

$\overline{\text{PBRST}}$ – Push button reset. This input pin is active low. It acts as the push button reset pin for the MicroMonitor.

$\overline{\text{NMI}}$ **–** Non-maskable interrupt. Active low signal that is generated in order to provide for an early power fail warning.

IN – NMI voltage input.

$\overline{\text{RST}}$ **-** Active Low Reset Output. This signal provides an output that can be used to reset a microprocessor.

RST - Active High Reset Output. This signal provides an output that can be used to reset a microprocessor.

MEMORY ORGANIZATION

The DS1846's serial EEPROM is internally organized with 32 pages. Each page contains 8 bytes. Each byte requires an 8-bit address for random byte addressing. The address bytes, starting at F8h, contain the wiper setting for the three potentiometers. The byte at address F8h determines the wiper setting for potentiometer 1, which contains 256 positions. The byte at address F9h determines the wiper setting for potentiometer 0, which contains 100 positions (00h to 63h). The byte at address FAh determines the wiper setting for potentiometer 2, which contains 100 positions (00h to 63h). If a value greater than 63h is written to either address F9h or FAh, the wiper is set according to the value in the seven least significant bits and the MSB is ignored. Address locations FBh though FFh are reserved and should not be written.

DEVICE OPERATION

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL high periods will indicate a start or stop conditions depending on the conditions discussed below. Refer to the timing diagram Fig 2 for further details.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command. Refer to the timing diagram Fig 2 for further details.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the DS1846 into a low-power mode. Refer to the timing diagram Figure 2 for further details.

Acknowledge: All address and data bytes are transmitted via a serial protocol. The DS1846 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode: The DS1846 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

Memory Reset: After any interruption in protocol, power loss, or system reset, the following steps reset the DS1846.

1. Clock up to nine cycles.

2. Look for SDA high in each cycle while SCL is high.

3. Create a start condition while SDA is high.

Device Addressing: The DS1846 must receive an 8-bit device address word following a start condition to enable a specific device for a read or write operation. The address word is clocked into the DS1846 MSB to LSB. The address word consists of 101000 binary followed by A0 then the R/W (READ/WRITE) bit. If the R/W bit is high, a read operation is initiated. The R/W is low, a write operation is initiated. For a device to become active, the value of A0 must be the same as the hard-wired address pins on the DS1846. Upon a match of written and hard-wired addresses, the DS1846 will output a zero for one clock cycle as an acknowledge. If the address does not match the DS1846 returns to a low-power mode.

Write Operations: After receiving a matching device address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the reception of this byte, the DS1846 will transmit a zero for one clock cycle to acknowledge the receipt of the memory address. The master must then transmit an 8-bit data word to be written into this memory address. The DS1846 will again transmit a zero for one clock cycle to acknowledge the receipt of the data byte. At this point the master must terminate the write operation with a stop condition. The DS1846 then enters an internally timed write process T_w to the EEPROM memory. All inputs other than those controlling the MicroMonitor are disabled during this write cycle.

The DS1846 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a stop condition after the first data byte. Instead, after the slave acknowledges receipt of the data byte, the master can send up to seven more data bytes using the same nine-clock sequence. After a write to the last byte in the page, the address returns to the beginning of the page. The master must terminate the write cycle with a stop condition or the data clocked into the DS1846 will not be latched into permanent memory.

Acknowledge Polling: Once the internally-timed write has started and the DS1846 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a start condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1846 responds with a zero.

Read Operations: After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read and sequential address read.

CURRENT ADDRESS READ

The DS1846 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS1846 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a stop condition afterwards.

RANDOM READ

A random read requires a dummy byte write sequence to load in the data word address. Once the device address and data bytes are clocked in by the master, and acknowledged by the DS1846, the master must generate another start condition. The master now initiates a current address read by sending the device address with the read/write bit set high. The DS1846 will acknowledge the device address and serially clocks out the data byte.

SEQUENTIAL ADDRESS READ

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1846 receives this acknowledge after a byte is read, the master may clock out additional data words from the DS1846. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a stop condition. The master does not respond with a zero.

For a more detailed description of 2-wire theory of operation, refer to the following section.

2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1846 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, A0. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 3 . Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9^{th} bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1846 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. Data transfer from a slave transmitter to a master receiver. The master transmits the 1st byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1846 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1846 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

3. Slave Address: command/control byte is the 1st byte received following the START condition from the master device. The command/control byte consists of a 6-bit control code. For the DS1846, this is set as ***101000*** binary for read/write operations. The next bit of the command/ control byte is the device select bit or slave address (A0). It is used by the master device to select which of two devices is to be accessed. When reading or writing the DS1846, the device-select bits must match the device-select pin (A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1 a read operation is selected, and when set to a 0 a write operation is selected.

Following the START condition, the DS1846 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the ***101000*** control code, the appropriate device address bit, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

WRITE PROTECT

An external pin WP (write protect) protects EEPROM data and potentiometer position from alteration in an application. This pin must be open or tied high to protect data from alteration.

READING AND WRITING THE POTENTIOMETER VALUES

Reading from and writing to the potentiometers consists of a standard read or write to EEPROM memory at the addresses F8h, F9h and FAh. The 8-bit value at address F8h controls the wiper setting for potentiometer 1, which has 256 positions. The 8-bit value at addresses F9h and FAh control the wiper setting of potentiometer 0 and 2 respectively, each has 100 positions. Potentiometer 1 may be set to any value between 00h and FFh. 00h sets the wiper of potentiometer 1 to its lowest value and FFh sets the wiper to its highest. Potentiometer 0 or 2 may be set to any value between 00h and 63h. A value of 00h sets the wiper of potentiometer 0 or 2 to its lowest position, and 63h sets the wiper to its highest position. Any hexadecimal value is a valid address. Writing a value greater than 63h will set the potentiometer according to the seven least significant bits and the MSB will be ignored.

Power Monitor

The DS1846 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below the minimum V_{CC} tolerance, a comparator outputs the RST and $\overline{\text{RST}}$ signals. RST and $\overline{\text{RST}}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moment of valid V_{CC}. On power-up, RST and $\overline{\text{RST}}$ are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

Pushbutton Reset

The DS1846 provides an input pin for direct connection to a pushbutton reset (see Figure 4). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{\text{RST}}$ signals of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The pushbutton can be initiated by connecting the $\overline{\text{NMI}}$ output to the $\overline{\text{PBRST}}$ input as shown in Figure 5.

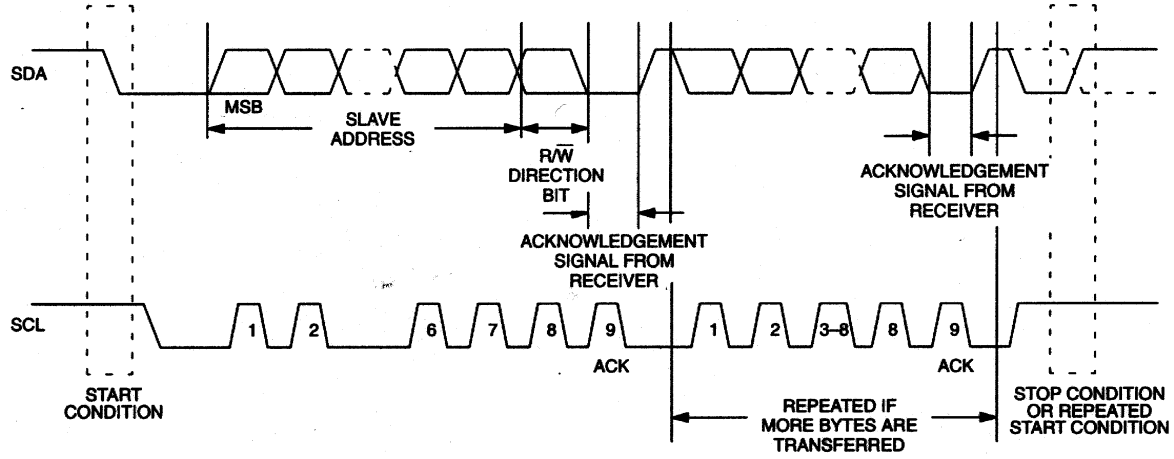
Non-Maskable Interrupt

The DS1846 generates a non-maskable interrupt ($\overline{\text{NMI}}$) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1846 requires that the voltage at the IN pin be limited to V_{CC}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shut-down between $\overline{\text{NMI}}$ and RST/$\overline{\text{RST}}$.

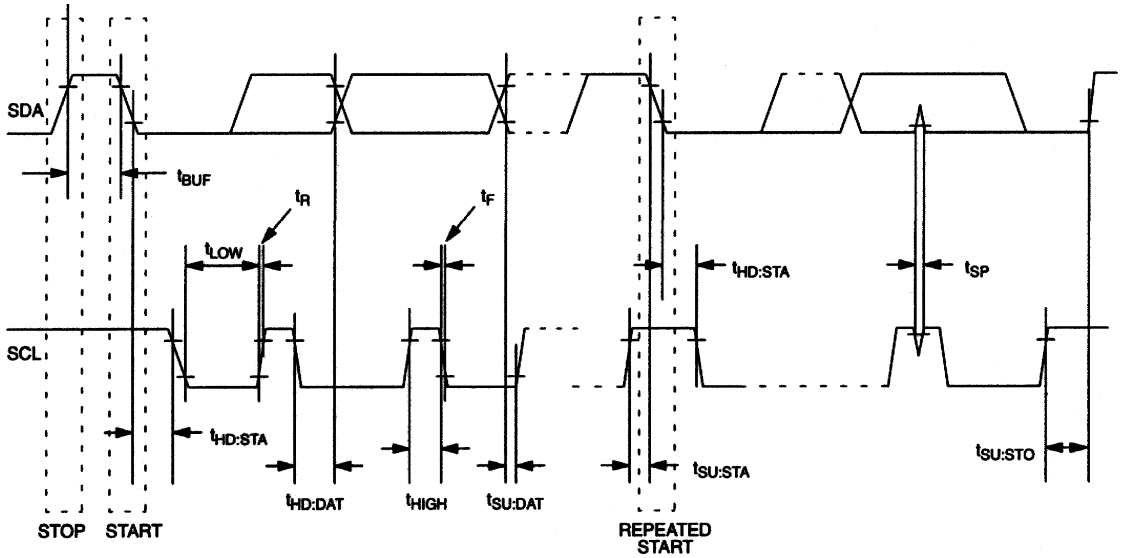
When the supply being monitored decays to the voltage sense point, the DS1846 pulses the $\overline{\text{NMI}}$ output to the active state for a minimum 200 s. The $\overline{\text{NMI}}$ power-fail detection circuitry also has built-in hysteresis of 100 V. The supply must be below the voltage sense point for approximately 5 s before a low $\overline{\text{NMI}}$ will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power-up, any detected IN pin levels below V_{TP} by the comparator are disabled from generating an interrupt until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{\text{NMI}}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Connecting $\overline{\text{NMI}}$ to $\overline{\text{PBRST}}$ would allow the non-maskable interrupt to generate an automatic reset when an out-of-tolerance condition occurred in a monitored supply. An example is shown in Figure 5.

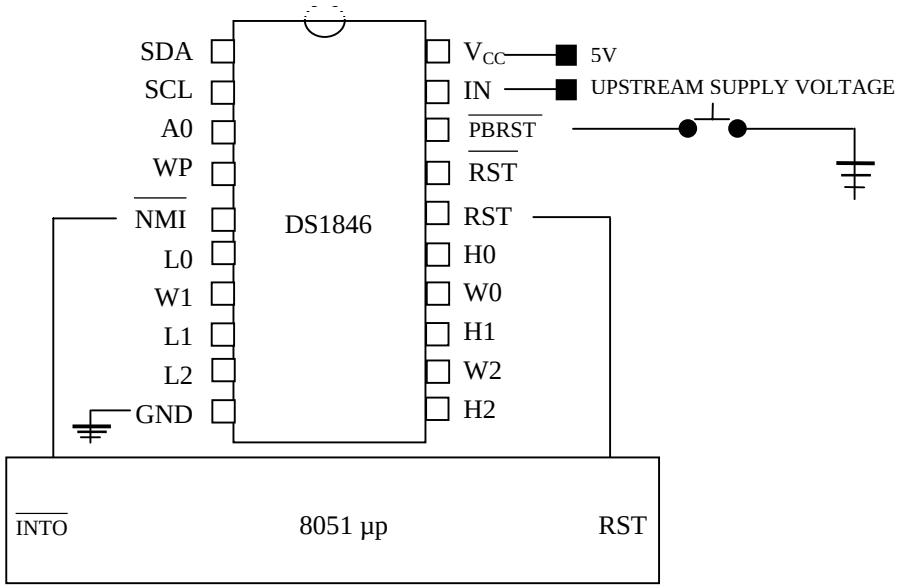
2- Wire Protocol Data Transfer Protocol Figure 2



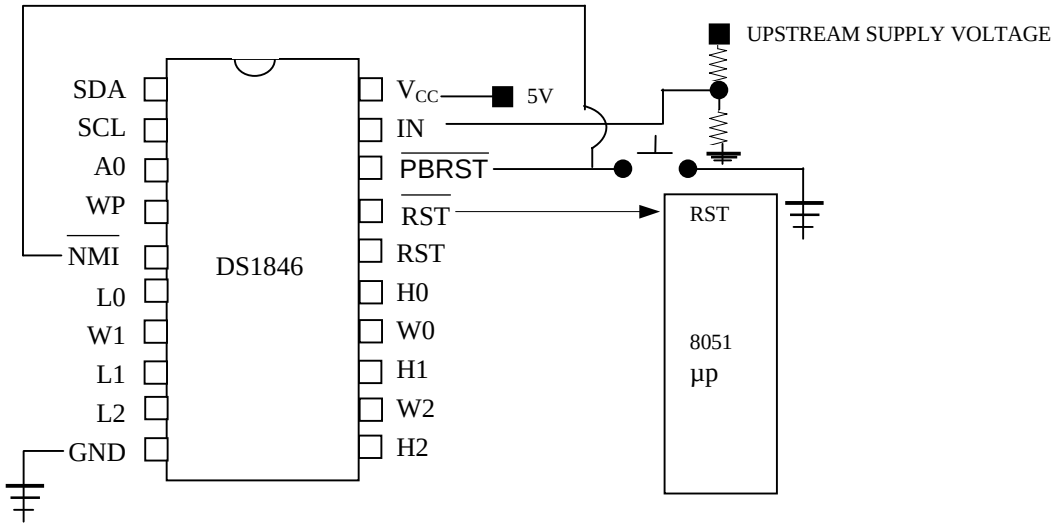
2-Wire AC CHARACTERISTICS Figure 3



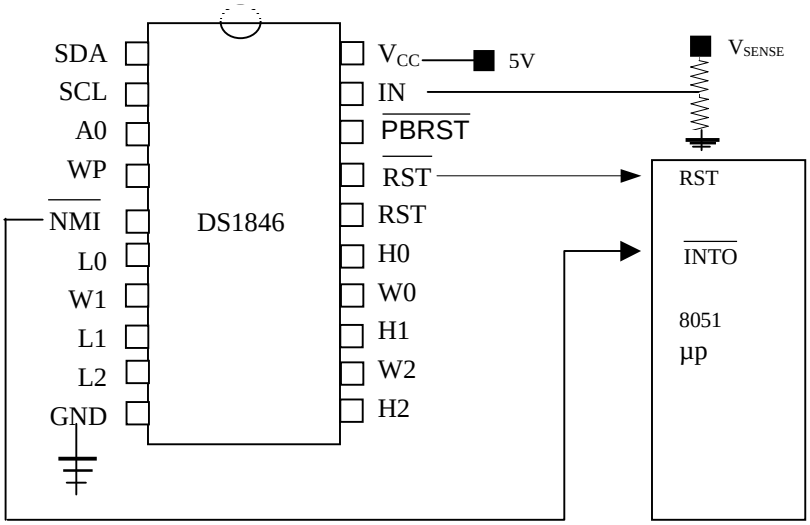
PUSHBUTTON RESET Figure 4



PUSHBUTTON RESET CONTROLLED BY $\overline{\text{NMI}}$ Figure 5



NON-MASKABLE INTERRUPT EXAMPLE Figure 6



$$V_{SENSE} = \frac{R1+R2}{R2} \text{ X } 1.25 \qquad V_{MAX} = \frac{V_{SENSE}}{V_{TP}} \text{ X } V_{CC}$$

Example: V_{SENSE} = 4.70V at the trip point
V_{CC} = 3.3V
10 kΩ = R2

Therefore: $\frac{4.70}{1.25}$ X 3.3 = 12.4V maximum

$$4.70 = \frac{R1+10k}{10k} \text{ X } 1.25 \qquad R1 = 27.6 \text{ k}\Omega$$

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature	-40°C to +85°C; Industrial
Programming Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	.7 V_{CC}		V_{CC}+0.5	V	1,3
Input Logic 0	V_{IL}	GND-0.5		.3 V_{CC}	V	1,3
Resistor Inputs	L,H,W	GND-0.5		V_{CC}+0.5	V	1,20
$\overline{\text{PBRST}}$ Input High Level	V_{IH}	2.0 V_{CC}-0.5		V_{CC}+0.3	V	1,23 1,24
$\overline{\text{PBRST}}$ Input Low Level	V_{IL}	-0.03		+0.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} =2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}				2	mA	17,18
Input Leakage	I_{LI}		-1		+1	µA	
Wiper Resistance	R_W	5V 3V		250 500	500 1000	Ω	
Wiper Current	I_W				1	mA	
Input Logic 1	V_{IH}		0.7 V_{CC}		V_{CC}+0.5	V	1,2
Input Logic 0	V_{IL}		GND-0.5		0.3V_{CC}	V	1,2
Input Logic levels A0, A1, A2		Input Logic 1 Input Logic 0	0.7 V_{CC} GND-0.5		V_{CC}+0.5 0.3V_{CC}	V	4
Input Current each I/O pin		0.4<$V_{I/O}$<0.9V_{DD}	-10		+10	µA	
Standby Current 3V 5V	I_{stby}			 15 25	40	µA	5
Low Level Output Voltage (SDA)	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
D_{OUT} Output @ 2.4V	I_{OH}		-1.0			mA	19
D_{OUT} Output @ 0.4V	I_{OL}				4	mA	19
WP Internal Pull Up Resistance, R_{wp}	R_{wp}		40	65	100	kΩ	
V_{cc} Trip Point	V_{CCTP}		4.25	4.4	4.5	V	1
Output Voltage	V_{OH}			V_{CC}-0.1		V	23
IN Input Trip Point	V_{TP}		1.20	1.25	1.30	V	1

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistance			-20		+20	%	20
Absolute Linearity			-0.5		+0.5	LSB	14
Relative Linearity			-0.25		+0.25	LSB	15
-3 dB Cutoff frequency	f_{cutoff}					kHz	13
Temperature Coefficient				750		PPM/°C	16

AC ELECTRICAL CHARACTERISTICS (-40°C to 85°C, Vcc=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f_{SCL}		0 0		400 100	kHz	*,6 **
Bus free time between STOP and START condition	t_{BUF}		1.3 4.7			µs	*,6 **
Hold time (repeated) START condition	$t_{HD:STA}$		0.6 4.0			µs	*,7,6 **
Low period of SCL clock	t_{LOW}		1.3 4.7			µs	*,6 **
High period of SCL clock	t_{HIGH}		0.6 4.0			µs	*,6 **
Data hold time	$t_{HD:DAT}$		0 0		0.9	µs	*,6,8,9 **
Data set-up time	$t_{SU:DAT}$		100 250			ns	*,6 **
Rise time of both SDA and SCL signals	t_R		20+0.1CB		300 1000	ns	*,10 **
Fall time of both SDA and SCL signals	t_F		20+0.1CB		300 300	ns	*,10 **
Set-up time for STOP condition	$t_{SU:STO}$		0.6 4.0			µs	* **
Capacitive load for each bus line	C_B				400	pF	10
EEPROM write time	T_W				5	ms	11
$\overline{PBRST} = V_{IL}$	t_{PB}		150			ns	
Reset Active Time	t_{RST}		130	205	285	ms	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			5	8	s	21
V_{CC} Slew Rate	t_F		20			s	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}		130	205	285	ms	22
V_{CC} Slew Rate	t_R		0			ns	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}				250	ns	
VIN Detect to $\overline{NMI}$	t_{IPD}			5	8	s	21

* fast mode

** standard mode

NOTES:

1. All voltages are referenced to ground.

2. I_{STBY} specified with for V_{CC} equal 3.0V and 5.0V and control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or V_{CC} for the corresponding inactive state.

3. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.

4. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.

5. I_{STBY} specified with for V_{CC} equal 3.0 V and 5.0V and control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or V_{CC} for the corresponding inactive state.

6. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000+250=1250$ ns before the SCL line is released.

7. After this period, the first clock pulse is generated.

8. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

9. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IN\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

10. C_B - total capacitance of one bus line in picofarads, timing referenced to $(0.9(V_{CC})$ and $(0.1)(V_{CC})$.

11. EEPROM write begins after a stop condition occurs.

12. Resistor inputs can not go beneath GND by more than 0.5V or above V_{CC} by more that 0.5V.

13. The –3 dB cutoff frequency for the DS1846 is 1 MHz.

14. Absolute linearity is used to measure expected wiper voltage as determined by wiper position. The DS1846 is specified to provide an absolute linearity of ± 0.5 LSB.

15. Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions. The DS1846 is specified to have a relative linearity of ± 0.25 dB.

16. When used as a rheostat or variable resister the temperature coefficient applies: 750 PPM/°C. When used as a voltage divider or potentiometer, the effective temperature coefficient approaches 30 PPM/°C.

17. Icc specified with SDA pin open.

18. Maximum I_{CC} is dependent on clock rates. During serial port activity maximum I_{CC} is specified for a clock rate of 5 MHz and worst case input levels.

19. Valid for Vcc = 5V only.

20. Valid at 25°C only.

21. Noise immunity - pulses < 2 µs at V_{CCTP} minimum will not cause a reset.

22. t_R = 5 µs

23. V_{CC} >= 2.4V

24. V_{CC} < 2.4V