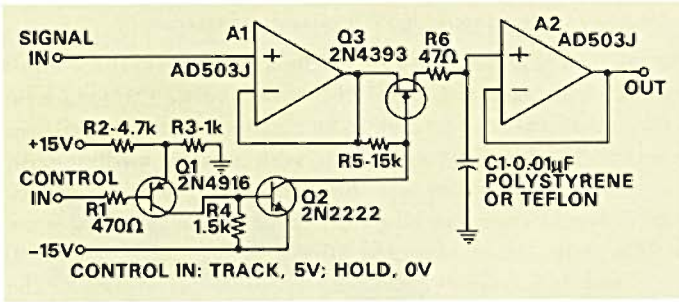
Application Briefs

Two Circuits that Use the AD503* to Advantage

TRACK-HOLD AMPLIFIER



The low input current and high slew rate of the AD503J make it an excellent device for track-hold applications. This circuit will track a ±10V input signal at frequencies up to 4kHz. When the control input changes from Track (+5V) to Hold (0V), the series FET switch, Q3, opens, and the input signal voltage is retained on capacitor C1. The output amplifier, A2, provides a high input impedance to keep C1 from discharging too rapidly.

The drift rate in Hold is determined primarily by the "off" leakage current of Q3, which tends to be greater than that of the amplifier, A2 (25pA max, 5pA typical for AD503J). For example, at 100pA leakage current, the drift rate (for C_1 = 0.01μF) is 10mV/s, and the rate doubles for every 10°C increase of temperature. Lower drift rate and higher accuracy—at the proportional expense of slower acquisition time—can be had by increasing the value of C1. The capacitor should be a type having low dielectric absorption (typically its dielectric would be polystyrene or teflon).

The switching FET, Q3, has low pinchoff voltage, and allows the circuit to handle ±10V signal voltages with standard ±15V supply. In the Track mode, with +5V applied to the control input, Q1 and Q2 are cut off, and the gate of Q3 is at the same voltage as A1's output. Thus, the FET is zero-biased for any value of input and has a resistance less than 100Ω. Resistor R5 adds to the "on" resistance so as to better isolate the capacitive load, C1, from the input follower, A1, to prevent ringing.

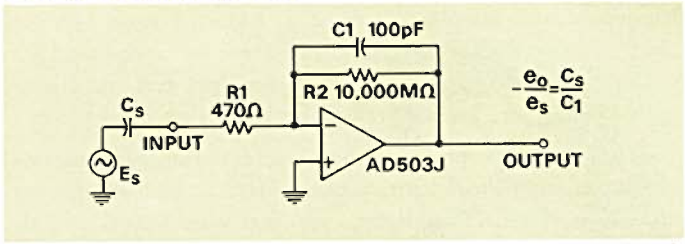
In the Hold mode, both Q1 and Q2 conduct and pull the gate of Q3 toward -5V. When the gate voltage drops to about 3V below the source (about 100ns after a step change to zero control voltage), the capacitor voltage ceases to track the input. Because of capacitance from the gate to the drain of Q3, the gate swing causes the small transferred charge to produce a small step (offset in Hold) in C1's voltage. Typically less than 10mV over the ±10-volt input range, this step is proportional to the gate voltage swing (15V + V_{in}).

There are also settling transients in A1 and A2, which increase the settling time to within 1mV of final value to about 2μs. For a 10-volt step applied during the Track mode, the settling time to within 1mV of final value is less than 15μs (caused by the limited charging rate of C1, and roughly proportional to C1).

The dielectric absorption of C1 may account for an additional 3mV of error if the input signal is changing rapidly at the time the circuit is gated into Hold.

*For technical data on AD503 FET-input I.C. op amp, use reply card. Circle 811

CHARGE AMPLIFIER



This circuit is designed for use with capacitive sources, such as piezoelectric accelerometers, crystal phono pickups and microphones, and capacitance alarms. The amplifier uses capacitance feedback and has a low input impedance, which makes its scale factor essentially independent of input cable capacitance. Because of the very low input current of the AD503J FET-input amplifier, a very high value of feedback resistance can be used to supply the dc bias current, which results in a low noise level of about 5.5μV rms in a 5Hz to 10kHz bandwidth, when connected to a 100pF source.

The voltage gain is determined by the ratio C_1/C_S. Because the capacitance of an input cable appears essentially across the summing junction of an inverting amplifier, it does not affect scale factor. (The amplifier's contribution to scale factor error is determined by loop gain, $(A\beta)^{-1}$. Since $1/\beta = 1 + C_S/C_1 + C_C/C_1$, and A is open-loop gain, the effect of cable capacitance on gain and linearity error is $C_C/(C_1 A)$. If C_C = 1000pF, its contribution to gain error would be 10/A. For those frequencies at which gain is decreasing at 6dB/octave, the error would be in quadrature, and therefore affect scale factor magnitude insignificantly for $A > 100$.)

With the component values shown, the circuit has a gain of unity when used with a 100pF source. Its frequency response extends from 0.16Hz to 800kHz (within 3dB). Resistor R1 isolates the capacitive source from the feedback loop in the megahertz region and helps to reduce overshoot.

For a gain of 10 with a 100pF source, the feedback capacitance, C_1, can be reduced to 10pF. Because of the very small capacitances in the circuit, care is required in the mechanical construction. Small mechanical vibrations can cause the input capacitance to the supply leads to vary, making in effect, a capacitor microphone, which may have substantial output. Also, because $\Delta Q = \Delta(CE) = C\Delta E + E\Delta C$, variations in C1 due to vibration will develop an additive error from the output bias offset voltage.

At low frequencies the response is -3dB at the frequency at which the reactance of C1 is equal to the resistance of R2. The maximum permissible value of R2 is determined by the allowable output offset and the input current of the amplifier at the highest operating temperature $|E_o\,(max) = I_b\,(max)\,R_2\,(max)|$.

Noise in an audio-frequency bandwidth is minimum when R2 has the highest permissible value, because the noise current furnished by R2 is inversely proportional to the square root of its resistance and the gain for amplifier voltage noise is determined (in the operating bandwidth) by 1/β.