# Specifications and Architectures of Sample-and-Hold Amplifiers

National Semiconductor
Application Note 775

## I. INTRODUCTION

Sample-and-Hold (S/H) amplifiers track an analog signal, and when given a "hold" command they hold the value of the input signal at the instant when the "hold" command was issued, thereby serving as an analog storage device. An ideal S/H amplifier would be able to track any kind of input signal, and upon being given a hold command store at its output, without delay, the precise value of the signal, and maintain this value indefinitely. Unfortunately, ideal S/H amps do not yet exist, and to be able to pick a S/H amp to suit a particular application, one must be familiar with how S/H amps are characterized, and how the S/H specifications will affect performance. In addition, it is helpful to be familiar with the common architectures that are used for S/H amps, as the architecture has a profound effect on the performance.

In this application note, we discuss the meaning and significance of the various specifications for S/H amps, and we also discuss several common S/H architectures, and how the performance is influenced by the architectures. In the appendix, we give a table which lists the key specifications for a number of S/H amps. Since the primary use of S/Hs is in data conversion, we will refer to such applications when discussing some of the specifications.

## II. MEANING OF THE SPECIFICATIONS

When discussing S/H specifications, it is helpful to have the circuit diagram of a S/H amp at hand. *Figure 1* shows a schematic of the open loop configuration, which will be discussed later in more detail. Since a S/H amp has two modes (the sample mode and the hold mode), and two transitions between the modes (sample-to-hold and hold-to-sample), it is convenient to discuss the specifications in these four groupings. *Figure 2* shows a S/H timing diagram that displays these two modes and two mode transitions.

### SAMPLE MODE SPECIFICATIONS

**Offset Voltage** is the deviation from zero of the output voltage when the input voltage is zero and the S/H amp is in sample mode. To maintain absolute accuracy in an A/D converter application, the offset voltage must be less than ½ LSB, or

$$V_{OS} < \frac{FS}{2^{n+1}},$$

where FS is full scale and n is the resolution of the analog-to-digital converter (ADC). Many S/H amps have provision for nulling the offset voltage; however, manual nulling can be expensive. Sometimes the offset is specified as an input offset voltage; this is particularly useful if the S/H can be configured for a gain other than unity.

**Gain Error** is the fractional voltage difference between the input voltage and the output voltage (excluding the effects of offset voltage) when the S/H amp is in sample mode; here we assume the ideal gain is unity. If absolute accuracy is required in an A/D application, the gain error should be less than ½ LSB, or

$$\Delta A_V = \frac{V_{OUT} - V_{IN}}{V_{IN}} < \frac{1}{2^{n+1}},$$

where n is the resolution of the converter.

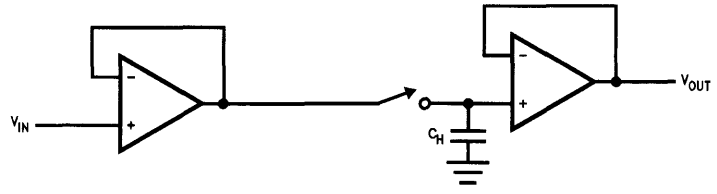


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**FIGURE 1. A Simple S/H Amplifier Consists of a Switch, Hold Capacitor, and Input and Output Buffers**

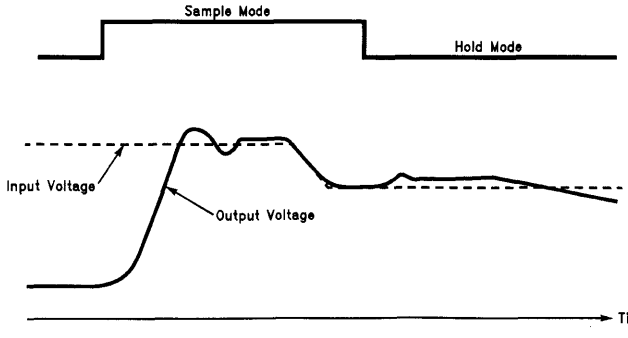


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**FIGURE 2. S/H Timing Diagram Showing the Two Modes and the Two Transitions Between the Modes**

**Gain Linearity Error** is the maximum deviation of the S/H's transfer curve from an ideal straight line connecting the end points of the transfer curve (the effects of offset and gain error are excluded). Spectral distortion is a consequence of gain linearity error in the S/H.

**Full-Power Bandwidth** is commonly defined in two ways. Some manufacturers define it as the frequency at which the voltage gain of the S/H amplifier drops by 3 dB relative to the gain at dc for a full-scale input. Others derive the full power bandwidth from a measurement of the S/H's slew rate. According to this definition, the full power bandwidth is equal to the frequency of the full-scale sine wave which has its maximum rate of change equal to the slew rate. This is given by

$$BW_{fp} = \frac{SR}{2\pi V_p}$$

where $2V_p$ is full scale and SR is the slew rate of the S/H.

**Small Signal Bandwidth** is the frequency at which the voltage gain of the S/H amplifier drops 3 dB relative to the gain at dc for an input that is much smaller than full scale, such as 20 dB or 40 dB below full scale. The small signal bandwidth is generally larger than the full power bandwidth; this would be the case if the full-power bandwidth is slew rate limited, for example. The small signal bandwidth is important for those applications which do not require the conversion of large amplitude, high frequency signals. Relying on the full power bandwidth specification in these cases would constrain one to a smaller bandwidth than can actually be attained in practice.

**Slew Rate** is the maximum rate of change of the output voltage when the S/H amplifier is in sample mode. Because the slew rate depends on the value of the hold capacitor, this capacitance must be specified if the hold capacitor is external. The slew rate is important because it affects the full-power bandwidth and acquisition time of the S/H.

## SAMPLE-TO-HOLD TRANSITION SPECIFICATIONS

**Aperture Time,** also known as aperture delay, is a specification that is defined differently by different manufacturers. The strict definition is that it is the time during which the signal is being disconnected from the hold capacitor after a hold command has been given *(Figure 3).* The broader definition is that it is the time between the application of the hold command and when the signal has been completely disconnected from the hold capacitor. The second definition includes the digital delay which occurs between when the hold command is applied and when the switch connecting the input signal to the hold capacitor *begins* to open.

Unlike aperture jitter, the aperture time is not a limiting factor on the maximum frequency for sinusoidal signals because for a sinusoidal signal, the voltage error caused by the aperture time manifests itself as a phase change, not an amplitude or frequency change.

**Effective Aperture Delay Time** is the time delay between the generation of the hold command and the appearance at the input of the final "held" voltage that exists on the hold capacitor *(Figure 3).* If precise timing is required, the hold command must be given an "effective aperture delay time" before the instant at which the input value is desired.

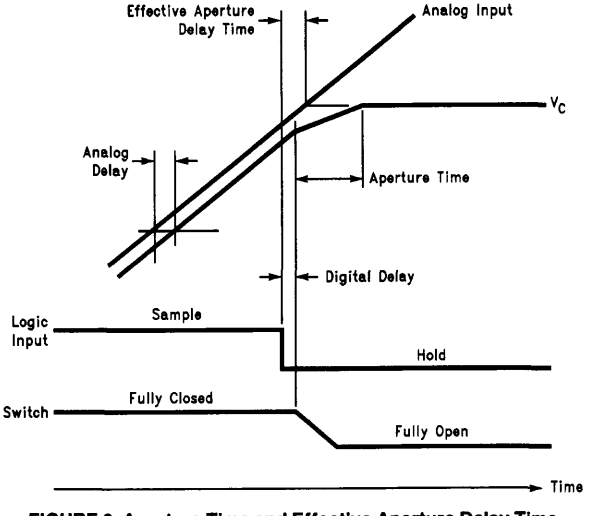


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**FIGURE 3. Aperture Time and Effective Aperture Delay Time**

**Aperture Jitter,** also known as **aperture uncertainty**, is the uncertainty in the aperture time. Aperture jitter results from noise which is superimposed on the hold command, which affects its timing. Aperture jitter is often specified as an rms value, which represents the standard deviation in the aperture time.

The aperture jitter sets an upper limit on the maximum frequency sinusoidal signal that can be accurately sampled by a S/H. In order not to lose accuracy, the rule of thumb is that the signal must not change by more than ±½ LSB during the aperture jitter time. Using a full-scale sinusoidal signal $V = A \sin(2\pi ft)$, we have

$$\frac{dV}{dt} = 2\pi fA \cos(2\pi ft) < \frac{\pm \frac{1}{2}\,LSB}{t_{aj}}$$

where A is half the analog input voltage range and $t_{aj}$ is the aperture jitter. Since ½ LSB = $A/2^n$, where n is the resolution of the converter, we get

$$f < \frac{1}{2\pi \times 2^n \times t_{aj}}$$

As an example of using this criterion, a 12-bit converter whose S/H amplifier has an aperture jitter of 100 ps could convert full-scale signals having frequencies as high as 388 kHz. Of course, this would only be possible if the converter's sampling rate is at least twice as high as this frequency, in order to satisfy the Nyquist criterion.

**Charge Transfer,** or **charge injection**, is the amount of charge transferred to the hold capacitor upon opening the switch after a hold command has been given. It is caused by capacitive coupling between the hold capacitor and the gate of the transistor that serves as the switch. Because of this charge transfer, there is a hold step at the output. For architectures in which the hold capacitor "sees" the input voltage, the charge transfer is a function of the input voltage, and can be a nonlinear function, leading to harmonic distortion.

**Hold Step,** also known as **pedestal** and **sample-to-hold offset,** is the voltage step that appears at the output due to the sample-to-hold transition *(Figure 4)*. It is caused by a transfer of charge to the hold capacitor due to the opening of the switch. The hold step can be determined from the charge transfer by

$$V_{HS} = \frac{Q}{C_H}$$

where Q is the charge transferred to the hold capacitor. Hence, the hold step can be reduced by increasing the value of the hold capacitor. This will, however, result in a larger acquisition time. For A/D applications, it is desirable that the hold step be independent of the input voltage and less than ½ LSB.

**Hold Mode Settling Time** is the time required for the output to settle within a specified error band after a hold command has been given. This error band is commonly specified as 1%, 0.1% or 0.01% of a full-scale step input. For A/D converter applications, one needs the output to settle within ±½ LSB before a conversion is started. The hold mode settling time is also important because the sum of the acquisition time, the hold mode settling time, and the A/D conversion time determines the maximum sampling rate of the S/H-ADC system. (If the conversions are pipelined, the sampling rate can be higher).

$$(f_s)_{max} = \frac{1}{t_{aq} + t_{HS} + t_c}$$

**Sample-to-Hold Transient** is the transient that appears at the output due to a sample-to-hold transition. The maximum amplitude of the transient is usually specified. S/Hs used to deglitch the output of digital-to-analog converter must have a small sample-to-hold transient.

## HOLD MODE SPECIFICATIONS

**Hold Capacitor Leakage Current** is the current which flows in or out of the hold capacitor while the S/H amplifier is in hold mode. The leakage current consists of three parts: leakage through the dielectric of the hold capacitor, leakage through the analog switch, and the input bias current of the output amplifier. (The leakage currents do not all necessarily have the same polarity). This specification is important because the droop rate is proportional to the hold capacitor leakage current.

**Droop Rate** is the rate at which the output voltage is changing due to leakage from the hold capacitor. If the S/H has an internal hold capacitor, the droop rate is specified in the data sheets. However, if the hold capacitor must be added externally, the droop rate depends on the value of the hold capacitor and is calculated from the equation

$$\frac{dV_{CH}}{dt} = \frac{I_L}{C_H}$$

where $I_L$ is the hold capacitor leakage current.

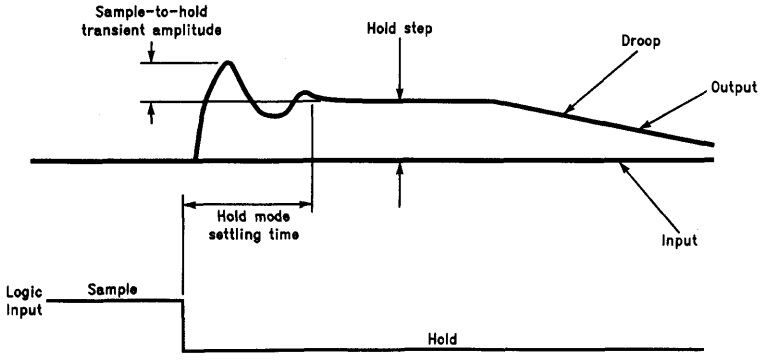


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**FIGURE 4. Sources of Error in Hold Mode and during the Sample-to-Hold Transition**

The droop rate is important for applications where the sampled voltage must be held within a specified error band for long periods of time. In A/D applications, one does not want the output to droop by more than ½ LSB during the conversion time. For these applications, the maximum allowable droop rate of the S/H is given by

$$\frac{dV_{CH}}{dt} < \frac{\frac{1}{2}LSB}{t_c} = \frac{FS}{(2^{n+1})\,t_c}$$

where FS is the full-scale voltage of the ADC, n is its resolution, and $t_c$ is the ADC conversion time. The droop rate can be reduced by increasing the value of the hold capacitor, but this results in a higher acquisition time.

**Feedthrough Attenuation Ratio** is the fraction of the input signal that appears at the output while the S/H amplifier is in hold mode. The feedthrough attenuation ratio is generally specified for a specific frequency of input signal. For A/D applications, the feedthrough must be less than ½ LSB for a full amplitude input. Hence, the feedthrough attenuation ratio must be at least

$$A_F > 20 \log (2^{n+1})\ dB$$

which can be simplified to $A_F > 6(n+1)$ dB, where n is the resolution of the converter.

### HOLD-TO-SAMPLE TRANSITION SPECIFICATIONS

**Acquisition Time** is the maximum time required to acquire a new input voltage once a sample command has been given *(Figure 5)*. A signal is "acquired" when it has settled within a specified error band around its final value of output voltage. The error band is usually either 0.1%, 0.01%, 1 mV, or ½ LSB (in applications that involve an ADC). The maximum value of the acquisition time occurs when the hold capacitor must charge to a full-scale voltage change. The acquisition time depends on the value of the hold capacitor, and this value must be specified if the hold capacitor is supplied externally. The acquisition time can be reduced by choosing a smaller hold capacitance; however, this will increase the hold step and droop rate.

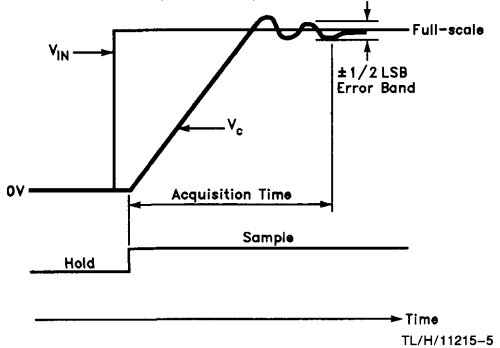


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**FIGURE 5. Acquisition Time**

### III. SAMPLE-AND-HOLD ARCHITECTURES

The symbol that is frequently used for the S/H amplifier in system block diagrams is a switch in series with a capacitor *(Figure 6)*. Although the switch can control the mode of the device, and the capacitor can store a voltage, a S/H using just these components would have very poor performance. By studying the deficiencies of such a configuration, one can better appreciate the components that are added to this basic core to comprise a practical S/H amplifier.

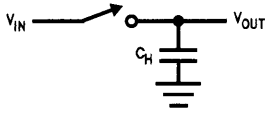


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**FIGURE 6. S/H Symbol**

First, when in sample mode the charging time of the hold capacitor for the S/H in *Figure 6* is dependent on the source impedance of the input. A large source impedance would give a large RC time constant, leading to a high acquisition time. To ameliorate this effect, one buffers the hold capacitor from the input with an operational amplifier (assuming that the op amp is capable of driving a capacitive load). The acquisition time will then be independent of the source impedance, and will in fact be low due to the low output impedance of an operational amplifier.

Second, when in hold mode the hold capacitor will discharge through the load. Hence, the droop rate will be load dependent and could be very high. To ameliorate this problem, one buffers the hold capacitor from the output with an op amp. the droop rate will then be independent of the load, and will actually be rather low, due to the large input impednace of an op amp.

Hence, in addition to a switch and a hold capacitor, a practical S/H amplifier must include input and output buffers. The two main variations of this structure, the open-loop and closed-loop architectures, differ in the manner of their feedback.

In the open-loop architecture *(Figure 7)*, the input and output buffer amps are each configured as voltage followers. The advantage of this architecture is its speed—the acquisition time and settling time are short because there is no feedback between the buffer amps. The disadvantage of this architecture is in its accuracy, which suffers because of the lack of feedback, causing the dc errors of both amplifiers to add.

For applications requiring high accuracy, one can use the closed loop-architecture, with either a follower output *(Figure 8)* or an integrator output *(Figure 9)*. The feedback significantly improves the accuracy of the S/H relative to the open-loop configuration, although the speed is somewhat less.

In both the open-loop architecture and the closed-loop architecture with follower output, the charge transfer, and hence the hold step, is a function of the input voltage. This is because the hold capacitor is connected to the input signal (through the input buffer amp). The closed-loop architecture with integrator output ameliorates this problem by connecting the hold capacitor to virtual ground instead of the nput signal. Hence the charge transfer is constant.

A new architecture which combines the speed of the open-loop configuration and the accuracy of the closed-loop configuration is the current-multiplexed architecture shown in *Figure 10*. The LF6197, National's High Performance VIP™ Sample-and-Hold Amplifier used this architecture. This architecture provides for a cancellation of charge injection, allowing one to use a small hold capacitor to get high speeds without the disadvantage of a large hold step.

In the sample mode, the transconductance input stage $g_{m1}$ is connected to the output buffer, while switches S2 and S3 are closed, thereby shorting the dummy capacitor $C_D$ and grounding one end of the hold capacitor, allowing it to charge. The hold command connects input stage $g_{m2}$ to the output buffer and opens switches S2 and S3. The voltage differential caused by charge injection into the hold capacitor is cancelled by an equal but opposite polarity of charge injection into the dummy capacitor, which is the same value as the hold capacitor. Hence, the common mode rejection of $g_{m2}$ results in a greatly reduced hold step.

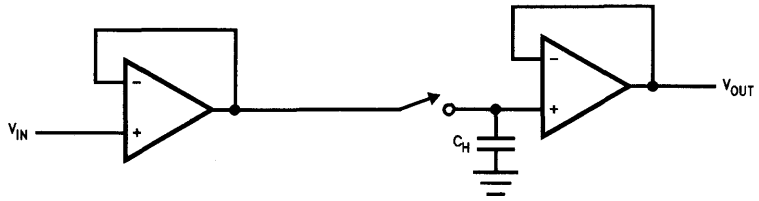


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**FIGURE 7. Open-Loop Architecture**

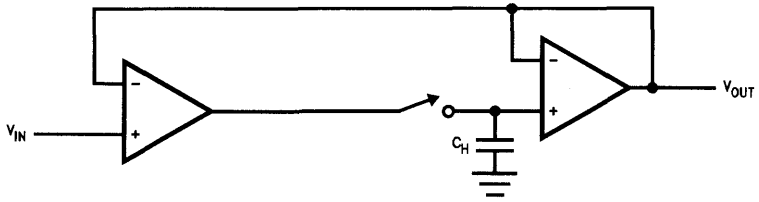


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**FIGURE 8. Closed-Loop Architecture with Follower Output**

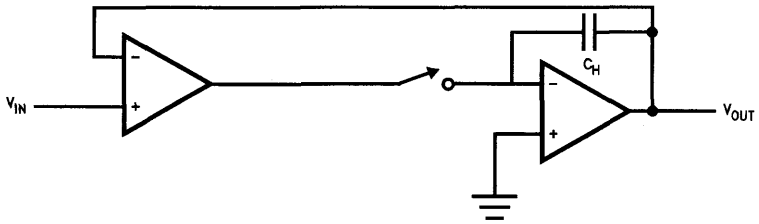


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**FIGURE 9. Closed-Loop Architecture with Integrator Output**

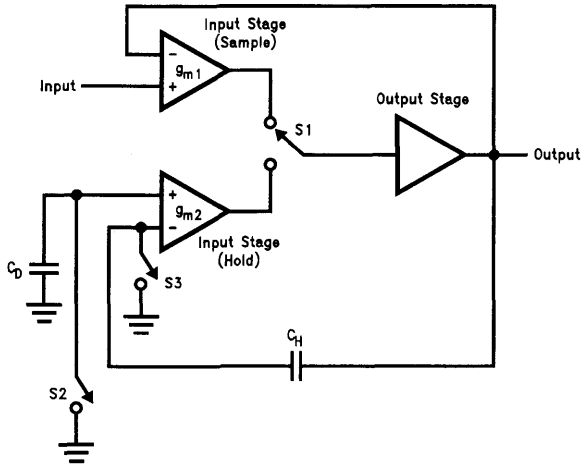


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**FIGURE 10. Current Multiplexed Architecture**

## IV. CONCLUSION

The selection of a S/H amplifier for a particular application requires an understanding of how S/Hs are specified and how a particular specification will affect system performance. When comparing S/H amplifiers one must also be aware that the test conditions and even the definitions of the specifications may vary from manufacturer to manufacturer. A clear understanding of the meanings of the specifications should make it easier to compare S/Hs that are tested using different definitions of the specifications.

## APPENDIX

What follows is a table which presents values of the specifications for a number of National's S/H amplifiers. Additional information, such as the values of the acquisition time and hold mode settling time at other hold capacitor values and to other accuracies, can be found in the data sheets. Additional S/H amplifiers made by National are the LH0023, LH0043, and LH0053.

### SPECIFICATIONS FOR SELECTED S/H AMPLIFIERS

| Spec (Note 1) | LF398 | LH4860 | LF6197 |
|---|---|---|---|
| Architecture | Closed-Loop, Follower Output | Closed-Loop, Integrator Output | Current Multiplexed |
| Input Offset Voltage | ±2 mV | ±0.5 mV | ±3 mV |
| Gain Error | 0.004% | ±0.005% | 0.03% |
| Small Signal BW | | 16 MHz | 25 MHz |
| Slew Rate | | 300 V/μs | 145 V/μs |
| Aperture Time | 200 ns | 6 ns | 4 ns |
| Aperture Jitter | | 35 $ps_{rms}$ | 8 $ps_{rms}$ |
| Hold Step (Note 2) | ±1.0 mV | ±2.5 mV | ±10 mV |
| Hold Mode Settling Time to 0.01% | 1 μs | 60 ns | 50 ns |
| Hold Capacitor Leakage Current | 30 pA | 5 pA | 6 pA |
| Droop Rate | | ±0.5 μV/μs | 0.6 μV/μs |
| Feedthrough Attenuation Ratio at 1 kHz | 90 dB | | 83 dB |
| Acquisition Time to 0.1% (Notes 3, 4) | 4 μs | 100 ns | 130 ns |

**Note 1:** The table lists the typical values of these specifications.

**Note 2:** LF398: $C_H$ = 0.01 μF, $V_{OUT}$ = 0V.

**Note 3:** $\Delta V_{OUT}$ = 10V.

**Note 4:** LF398: $C_H$ = 1000 pF.