Single a-d converter cuts cost of droopless sample-and-hold

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Because leakage currents cause droop, sample-and-hold circuits with capacitors as storage elements cannot retain a sampled voltage indefinitely. This is the major reason designers, to improve sample-and-hold performance, have resorted to converters combining analog-to-digital and digital-to-analog converter functions. But a single a-d device can be made to perform both functions alternately, thus cutting the cost and complexity of the two-converter scheme. Only one operational amplifier and a solid-state switch are needed in addition.

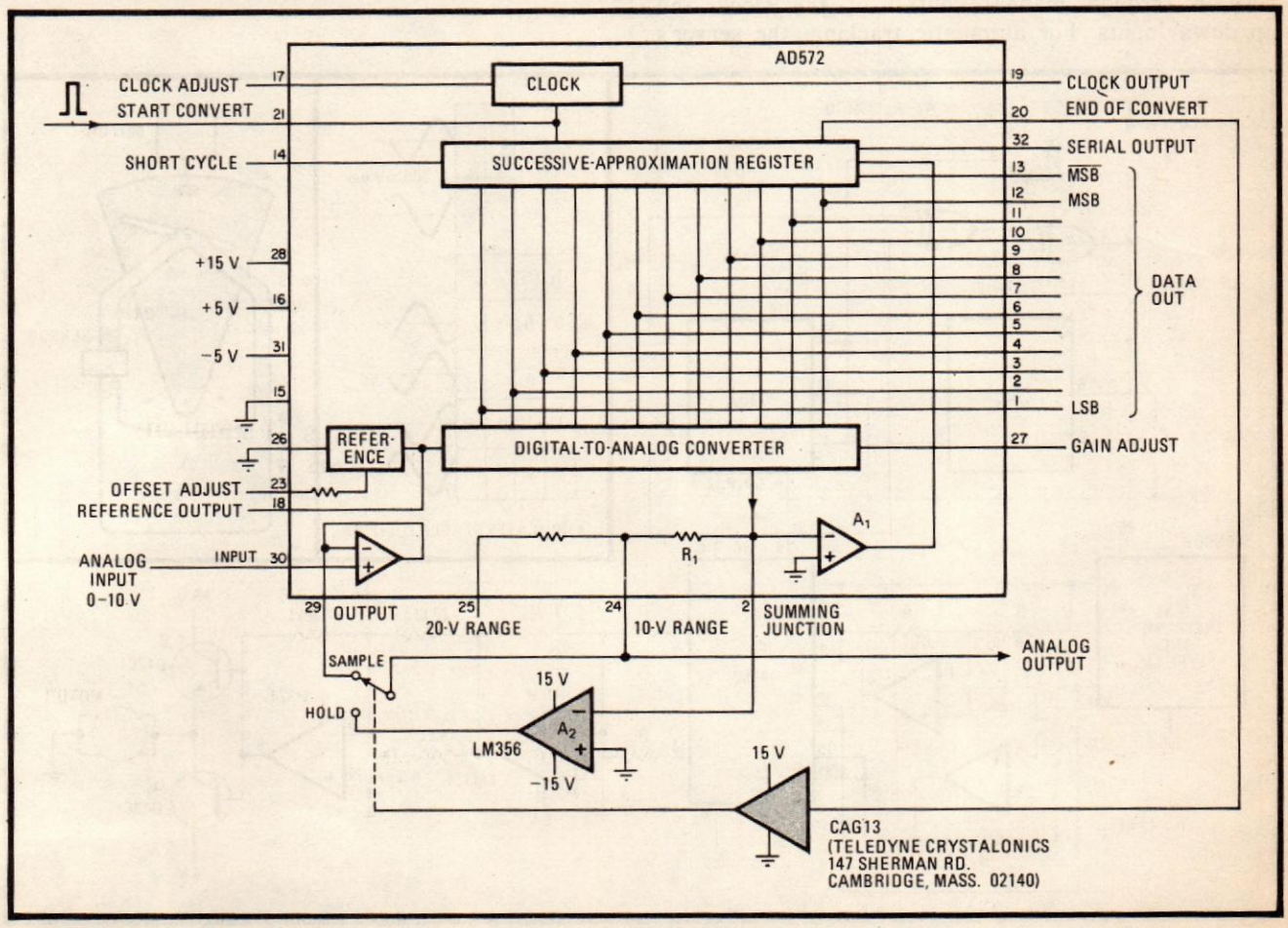
The more popular forms of a-d converter use a successive-approximation register that—with the aid of a self-contained comparator and a d-a converter—generates a digital estimate of the sampled analog voltage. When the comparison has been approximated to the least significant bit, the measurement is ended and an end-of-conversion signal is generated. If the unit is then configured as a latched d-a converter, the sampled analog voltage may be recovered and held indefinitely (assuming that one input of the comparator is accessible).

As shown, in the normal a-d conversion mode of a representative device like the AD582, a start-convert pulse initiates the measurement. An analog voltage, applied across resistor R_1 in the summing junction of comparator A_1, can then be sampled.

The successive-approximation register generates a 12-bit equivalent of the analog voltage and also drives the d-a converter that is connected to A_1's summing junction. The d-a converter then attempts to null A_1's output, whereupon the end-of-conversion signal (EOC) is generated. The sampling period takes a nominal time of 2.5 microseconds.

In this circuit, the EOC signal energizes a solid-state relay (CAG13) so that the converter can be switched to the holding mode. R_1 is then placed at the output of an op amp, A_2.

A_2's output maintains A_1's summing junction at a voltage null so that the output voltage becomes the potential across R_1—that is, the sampled voltage. Note that the switch resistance and A_2's input-bias current are taken into consideration for both modes and therefore they are not, for all practical purposes, sources of error in the measurement. □



Inverting the converting. This analog-to-digital converter, when it is combined with an op amp and switch, can provide d-a function on the hold portion of sample-and-hold cycle, thereby reducing cost and complexity of the usual two-converter (a-d–d-a) scheme. No sampling-peak capacitor is required in the converter sampling technique, so that the sample-voltage droop is eliminated.