Apply sample-and-hold techniques for elegant design solutions

More than just a data-acquisition device, a S/H amplifier can also simplify—indeed, make possible—other circuit designs. The applications presented here provide a sampling of ideas ranging from data-link eavesdropping to oven control.

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Most designers regard sample/hold amplifiers merely as system components utilized in high-speed data-acquisition work. But they should also consider S/H devices' possibilities as circuit-oriented building blocks.

Sampling techniques can implement circuit functions that are sophisticated in performance, low in cost and not easily realized with other approaches. The designs presented here illustrate a few of the many application possibilities for S/H amplifiers as circuit elements.

Stop fiber-optic eavesdropping

Fig 1 depicts a design that detects attempts to tap a fiber-optic data link. Because the circuit works with pulse-encoded data formats, it detects only short-term changes in the fiber-optic cable's loss characteristics. Thus, long-term changes arising from temperature variations or component aging won't trigger the alarm, but any unauthorized data extraction—a short-term phenomenon—will.

Under normal operating conditions, because the input light pulse's amplitude is constant, so is the level detected by photodiode D_1 and amplified by A_6. A_6's constant-amplitude output pulses are sampled by the S/H amplifier, A_3, which is driven by a delayed S/H pulse generated by A_1 and A_2. (Delaying the sampling ensures that A_6's output settles completely.) Unless

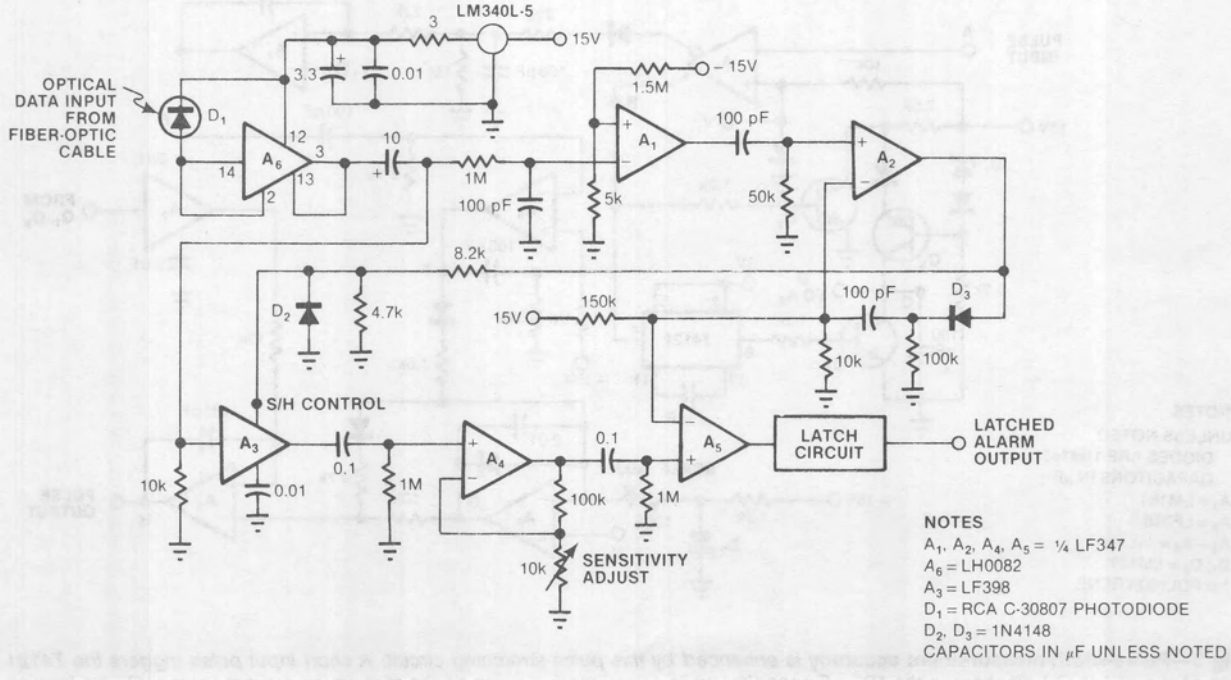


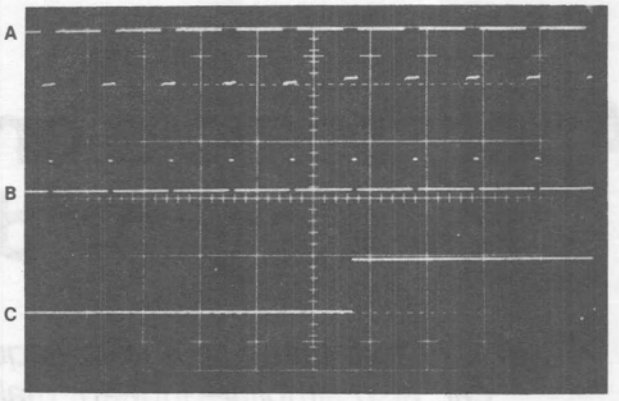
Fig 1—Fiber-optic-link eavesdropping attempts *are immediately detected by this design. Working on a pulse-by-pulse comparison basis, A_3 samples each input pulse and holds its amplitude value as a dc level. Anything that disturbs the next input's amplitude causes a jump in this level; because A_4 is an ac-coupled amplifier, the comparator and latch then activate.*

Sample/hold techniques benefit fiber-optics usage

something changes the input light pulse's amplitude, A_3's output is a dc voltage; because A_4 is ac coupled, its output is 0V.

A link-intrusion attempt disturbs the input pulse's amplitude, causing A_6's output to shift. A_4 ac-amplifies this shift, trips comparator A_5 and activates the alarm latch.

This sequence is represented in **Fig 2**, where trace A is A_6's output, B tracks A_3's S/H control pin and C is the alarm's output. An input disturbance occurs slightly past trace A's midpoint, indicated by A_6's reduced output. The alarm's output latches HIGH just after the Sample command rises—a result of the S/H amplifier's level jumping to A_6's changed output. **Fig 2** shows a large disturbance (10%) for demonstration purposes, but in practice, the design can detect an energy loss of as little as 0.1%.



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV	500 μSEC/DIV
B	10V/DIV	500 μSEC/DIV
C	5V/DIV	500 μSEC/DIV

Fig 2—An intrusion attempt *occurring just past the midpoint of trace A is immediately detected by* **Fig 1***'s circuit. The photodetector's amplifier output (A) shows a slight amplitude drop. The next time the S/H amplifier samples this signal (B), the alarm latch sets (C).*

Stretching pulses proportionally

You can measure short-duration pulses with another S/H circuit, shown in **Fig 3.** The design works for either single-shot or repetitive events.

Assume that you must measure a 1-μsec-wide pulse to an accuracy of 1%. With digital techniques, this task would require use of a 100-MHz clock (1% of 1 μsec). **Fig 3**'s design avoids this requirement by linearly amplifying the pulse's width by a factor of 1000 or more. Thus, a 1-μsec input pulse becomes a 1-msec output pulse—a somewhat easier time duration to measure to 1% accuracy.

Fig 4 shows how this design responds to an even shorter (350 nsec) input pulse (trace A). Comparator A_1's output goes LOW (B), and the 74121-one-shot/Q_1 combination discharges the associated 100-pF capacitor via a 50-nsec pulse (D). Concurrently, Q_2 turns off, allowing current source Q_3 to start linearly recharging

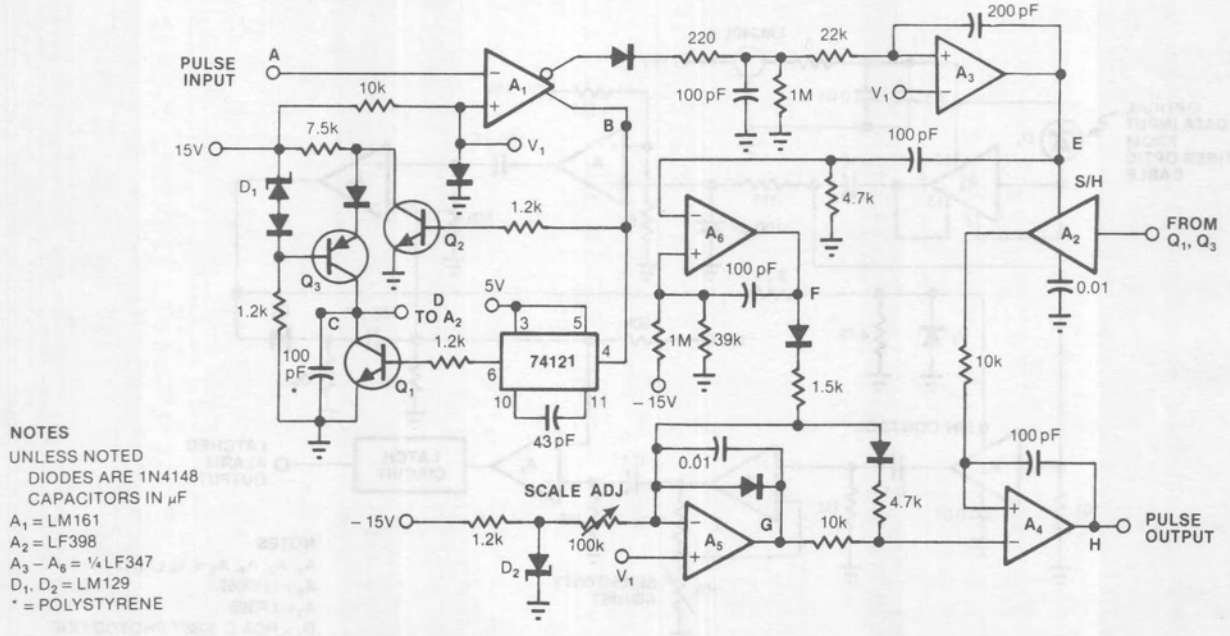
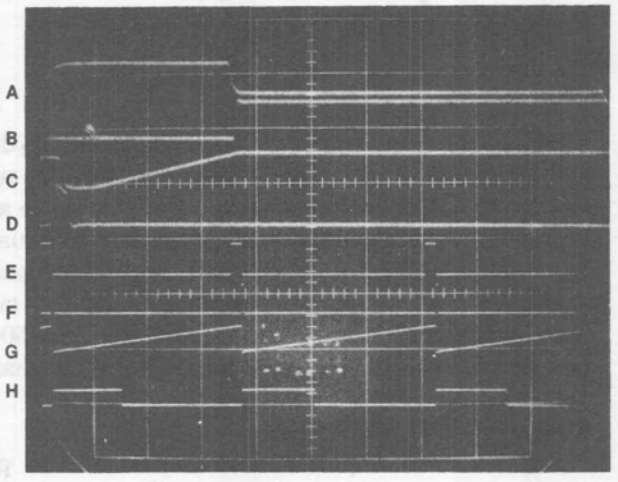


Fig 3—Pulse-width-measurement accuracy *is enhanced by this pulse-stretching circuit. A short input pulse triggers the 74121 one-shot and (via Q_1) discharges the 100-pF capacitor while concurrently turning on the recharging current source, Q_3. So long as the input pulse is present, the capacitor charges; when the pulse ends, the capacitor's voltage is proportional to the pulse's width. S/H amplifier A_2 samples this voltage, and the resultant dc level controls the ON duration of the A_4/A_5 pulse-width modulator. (Letters at key points in the circuit refer to waveforms shown in* **Fig 4.**)

the 100-pF capacitor (C). Charging continues until the input pulse terminates, which causes A_1's output to again go HIGH and cut off the current source. The voltage across the capacitor is then directly proportional to the input pulse width; S/H amplifier A_2 samples this voltage when A_3 generates the command shown by trace E. (Note the horizontal scale's change.) A_3's input derives via a delay network from A_1's inverting output, completing the sampling cycle.

A_2's dc output voltage represents the most recently applied input pulse's width. This voltage feeds to A_4, which works with A_5 as a voltage-controlled pulse-width modulator. A_5's output ramps positive (G) until reset by a pulse from A_6. (A_6 goes HIGH briefly (F) each time A_3's output (E) goes LOW.) To generate the circuit's final output, A_4 compares A_6's output with A_2's and produces a HIGH level (H) for a time linearly dependent upon A_2's output.

With the component values shown in **Fig 3**, the input-to-output time-amplification factor equals approximately 2000. Thus, a 1-μsec input yields a 1.4-msec output. Absolute accuracy is 1% (10 nsec) referred to the input, and the measurement's resolution extends down to 2 nsec. The 74121 one-shot's 50-nsec pulse limits the minimum measurable pulse width.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 μSEC/DIV
E	50V/DIV	500 μSEC/DIV
F	50V/DIV	500 μSEC/DIV
G	20V/DIV	500 μSEC/DIV
H	100V/DIV	500 μSEC/DIV

Fig 4—A sequence of events *in Fig 3's circuit stretches a 350-nsec input pulse (A) by a factor of 2000. When triggered, comparator A_1 goes LOW (B). This action starts the recharging of a capacitor (C) after its previously stored charge has been dumped (D). When the input pulse ends, the capacitor's voltage is sampled under control of a delayed pulse (E) derived from the input amplifier's inverting output (F). The sampled and held voltage then turns off a voltage-controlled pulse-width modulator (G), and a stretched output pulse results (H).*

Control a pulse's amplitude

S/H amplifiers also make possible the amplitude-stabilized pulse generator shown in **Fig 5**; this circuit drives 20Ω loads at levels as high as 10V pk. The pulse's adjustable amplitude remains stable over time, temperature and load changes.

The circuit functions by sampling the output pulse's amplitude and holding this value as a dc voltage. This voltage then connects to a feedback loop that controls the output switching devices' supply voltage.

Specifically, an input TTL-level pulse turns on output drivers Q_2 and Q_3 and simultaneously places S/H amplifier A_1 in Sample mode. When the input pulse ends, A_1 outputs a dc voltage that represents the output pulse's amplitude. A_2 compares this level with the one

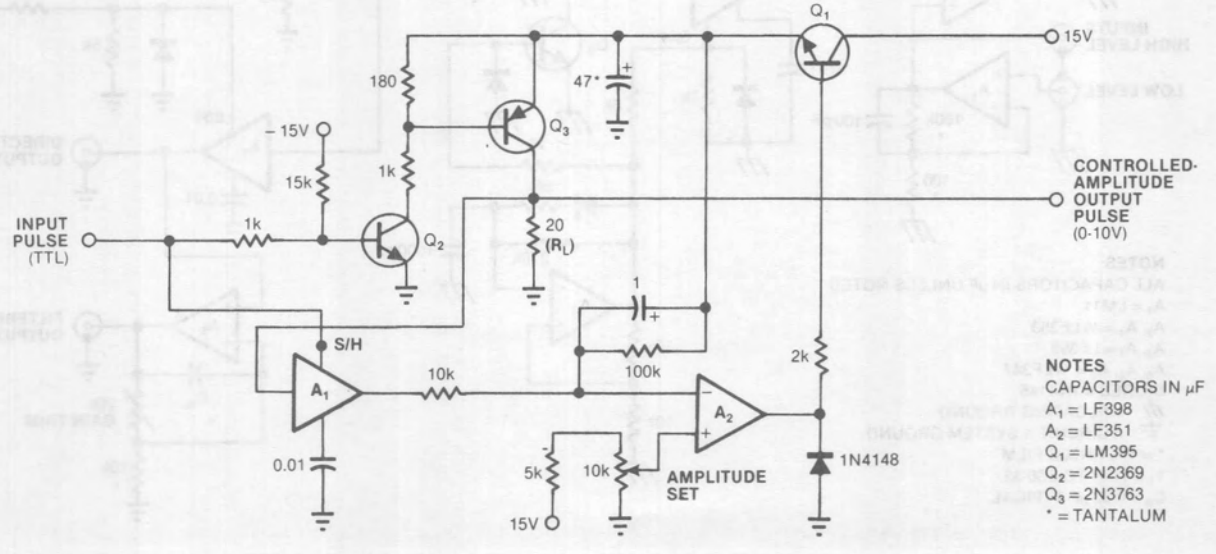
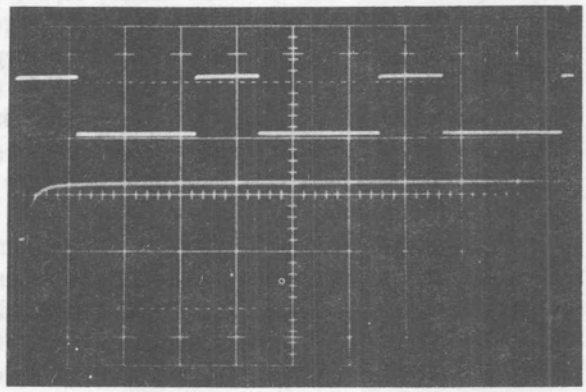


Fig 5—Pulse-amplitude control *results when this circuit samples an output pulse's amplitude and compares it with a preset reference level. When the output exceeds this reference, A_2 readjusts switching transistor Q_3's supply voltage to the correct level.*

Pulse-amplitude control results from S/H designs

established by the Amplitude Set adjustment; A_2 drives emitter follower Q_1, which provides the dc supply voltage to output switches Q_2 and Q_3. This servo action forces the output pulses' peak amplitude to equal the "set" value, regardless of Q_3's losses or output loading.

Fig 6's trace A shows the pulser's overall output wave shape, and traces B and C detail the clean 50-nsec rise and fall times. (Note the horizontal scale change.)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	10V/DIV	100 nSEC/DIV

Fig 6—A 10V, 0.5A pulse (A) *is amplitude-stabilized by the S/H technique depicted in* **Fig 5.** *Note the clean 50-nsec rise (B) and fall (C) times.*

Input isolation made easy

Fig 7 shows a powerful extension of the pulse-amplitude-control scheme that permits you to measure low-level signals (eg, thermocouple outputs) in the presence of common-mode noise or voltages as high as 500V. Despite the input terminals' complete galvanic isolation from the output, you can expect a 0.1% transfer accuracy. And by using the optional low-level preamp (A_1), you can measure inputs as low as 10 mV FS.

The circuit works by generating a pulse train whose amplitude is linearly related to the input signal's amplitude. This pulse train drives the input-to-output isolating transformer, T_1. T_1's output, demodulated to a dc level, provides the circuit's system-ground-referenced output. The pulse train's amplitude is controlled by a loop similar to the one employed in the pulse-amplitude-servo design. Here, however, the Amplitude Set doesn't appear, and the servo amplifier's + input becomes the signal input.

Set up as an oscillator, A_2 generates both the sample pulse for S/H amplifier A_3 and the drive for switches Q_2 and Q_3 (**Fig 8**, trace A). The feedback to the pulse-amplitude stabilizing loop comes from T_1's isolated secondary—a trick that ensures highly accurate amplitude-information transfer despite T_1's or Q_2's losses.

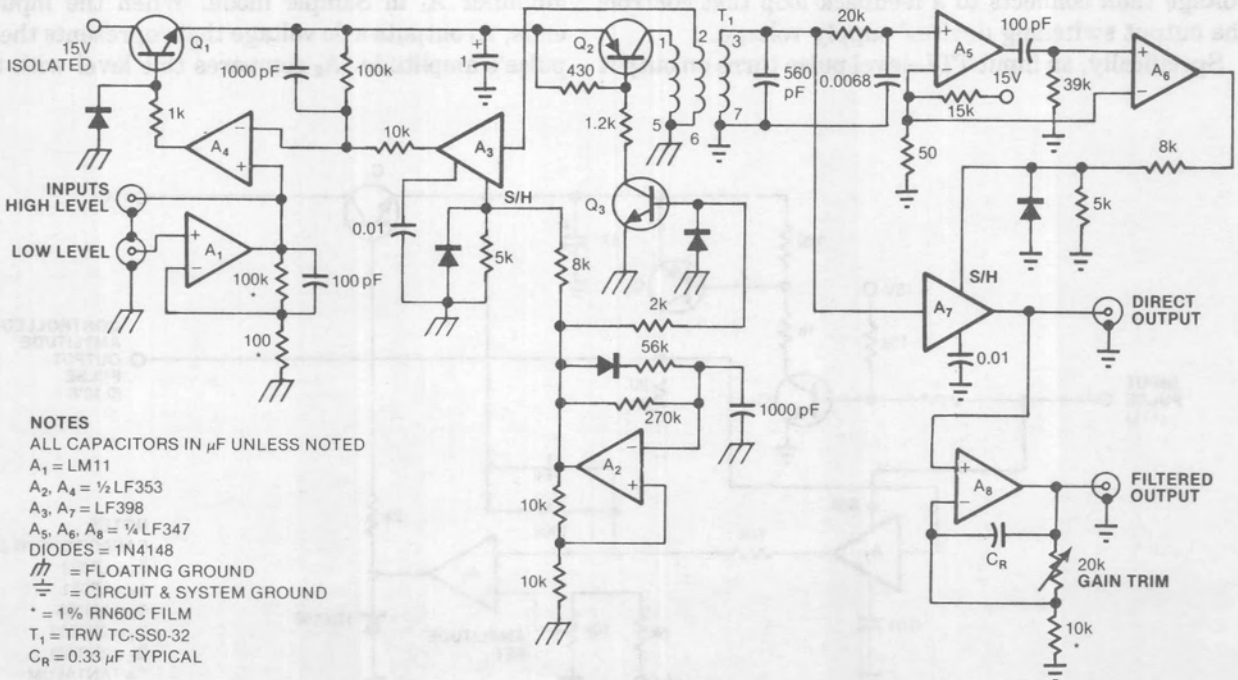
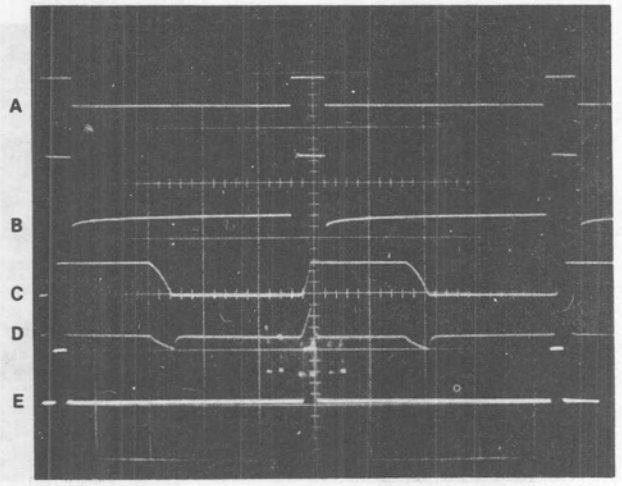
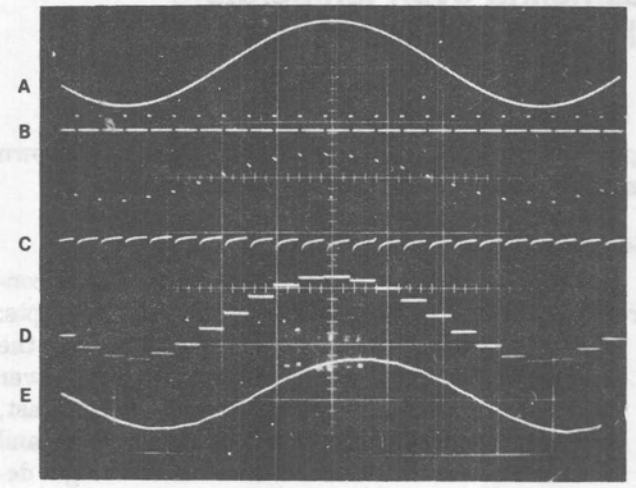


Fig 7—Obtain input-signal isolation *using this circuit's dual-S/H scheme. Analog input signals amplitude-modulate a pulse train using a technique similar to that employed in* **Fig 5***'s design. This modulated data is transformer coupled—and thereby isolated—to a dc filter stage, where it's resampled and reconstructed.*



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	100 μSEC/DIV
B	1V/DIV	100 μSEC/DIV
C	50V/DIV	100 μSEC/DIV
D	10V/DIV	100 μSEC/DIV
E	5V/DIV	100 μSEC/DIV

Fig 8—Fig 7's in-circuit oscillator (A_2) *generates both the sampling pulse (A) and the switching transistors' drive. Modulated by the analog input signal, Q_2's (and therefore T_1's) output (B) is demodulated by S/H amplifier A_7. A_5's output (C) and A_6's input (D) and output (E) provide a delayed Sample command.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	100V/DIV	
C	5V/DIV	
D	5V/DIV	
E	5V/DIV	

Fig 9—Completely input-to-output isolated, ***Fig 7's*** *circuit's analog input signal (A) is sampled by a clock pulse (B) and converted to a pulse-amplitude-modulated format (C). After filtering and resampling, the reconstructed signal (D) is available smoothed (E).*

S/H amplifier A_7 demodulates the amplitude-encoded signal at T_1's output (B) back to a dc level. A_5's output (C) and A_6's + input (D) and output (E) provide A_7's delayed Sample command. A_8 furnishes an optional gain-trimmed and filtered output.

Fig 9 illustrates the design at work. Here, the input signal (trace A) is a dc-biased sine wave. Trace B shows A_2's output clock pulse, and A_7's Sample command

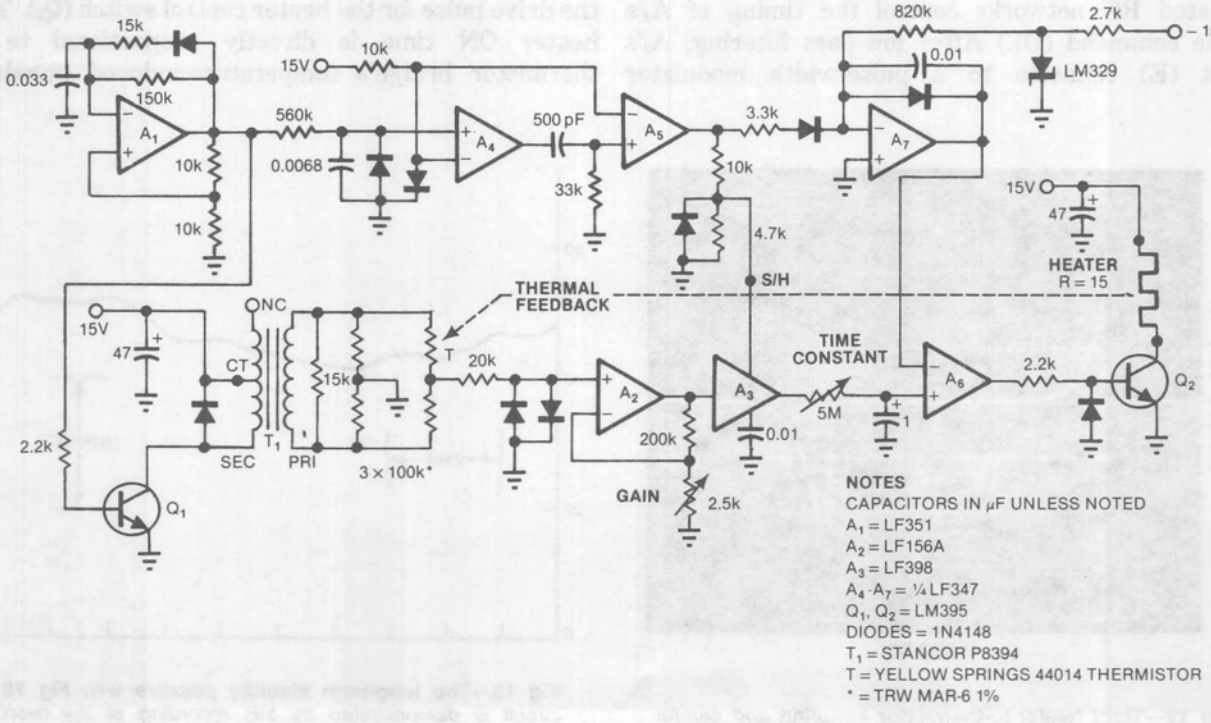


Fig 10—Tight temperature control *results when high-voltage pulses synchronously drive a thermistor bridge—a trick that increases signal level—and are then sampled and used to control a pulse-width-modulated heater driver.*

Sampling oven temperature tightens stability

appears as trace C. A_7's reconstructed output is shown as trace D and A_8's filtered output as trace E.

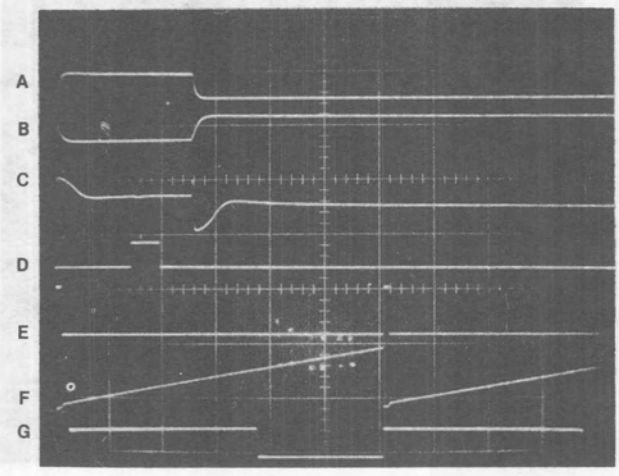
Sampling holds the temperature

The S/H-based high-stability oven-temperature controller shown in **Fig 10** embodies two unusual concepts:

- High-voltage, low-duty-cycle pulses drive the circuit's bridge and thus provide low power dissipation and high output levels. (In contrast, the power-dissipation limits of the resistors and thermistors in standard thermistor-bridge designs define the maximum dc bias level and therefore the maximum recoverable signal.)
- A S/H amplifier performs as a synchronous detector in the circuit's servo feedback loop. And because the sampling pulse establishes the design's reference level as well as the sampling interval, even the usual drift problems don't arise.

The circuit generates pulses via the oscillator-A_1/amplifier-Q_1 combination, driving a standard 24V transformer (T_1) "backwards." The transformer applies a floating 100V pulse across the thermistor bridge. Because one side of the bridge's output is grounded, this signal becomes the pair of complementary 50V pulses shown in **Fig 11** (traces A and B).

Amplified by A_2 (**Fig 11**, trace C), the bridge's output feeds to S/H amplifier A_3, whose dc output level equals A_2's peak output. (The A_4 and A_5 stages and their associated RC networks control the timing of A_3's Sample command (D).) After low-pass filtering, A_3's output (E) connects to a pulse-width modulator consisting of A_6 and A_7. A_5's output periodically resets A_7's output ramp (F). A_6's output pulse (G) results from the comparison of A_5's and A_3's outputs and serves as the drive pulse for the heater control switch (Q_2). Thus, heater ON time is directly proportional to the thermistor bridge's temperature-induced unbalance.



TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	200 μSEC/DIV
B	100V/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	10V/DIV	200 μSEC/DIV
E	5V/DIV	1 mSEC/DIV
F	10V/DIV	1 mSEC/DIV
G	50V/DIV	1 mSEC/DIV

Fig 11—Driving a thermistor bridge *with complementary high-voltage pulses (A and B) permits high-gain amplification without drift problems (C). Driven by a delayed Sample command (D), a S/H amplifier converts the bridge's error signal to a dc level (E) that controls a pulse-width-modulated heater driver (F and G).*

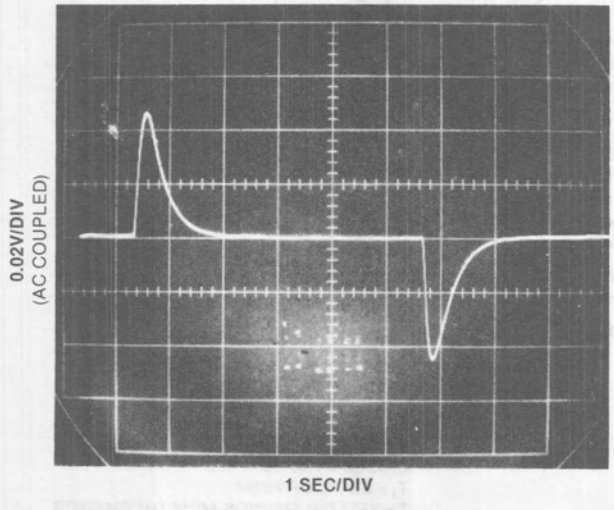


Fig 12—Tight heater-to-thermistor coupling *and careful calibration can provide rapid temperature restabilization. Here the controlled oven recovers within 2 sec after ±0.002°C steps.*

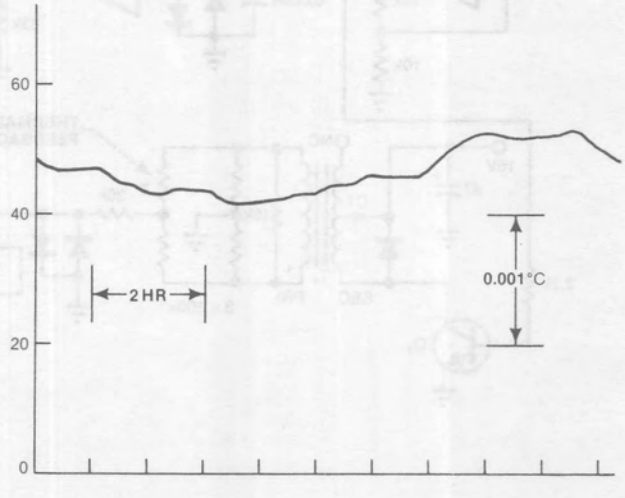


Fig 13—The long-term stability *possible with* ***Fig 10****'s circuit is demonstrated by this recording of the oven's temperature. Set at 50°C, the internal temperature stays within 0.001°C even though the exterior temperature varies by 6°C.*

Oven temperature stabilizes within 2 sec

Heater-to-thermistor thermal feedback completes the servo loop.

To adjust the loop's performance characteristics, apply small step changes in the temperature setpoint by switching a 100Ω resistor in series with one of the bridge's resistors. (For the thermistor shown in **Fig 10,** this modification produces a 0.02°C change.) While monitoring the loop's response at A_3's output, adjust the Gain and Time Constant potentiometers for minimum settling time.

Fig 12 shows how the system stabilizes within 2 sec for both positive and negative steps. And **Fig 13** demonstrates the design's very tight temperature-control capability. Set at 50°C, the oven's interior temperature varies by less than 0.001°C even when the ambient temperature changes by 6°C. Although **Fig 13** shows only a a few hours of operation, the circuit continued this performance over a 48-hr test period. **EDN**

Author's biography

Jim Williams, design engineer with National Semiconductor Corp's Linear Applications Group, Santa Clara, CA, has made a specialty of analog-circuit design and instrumentation development. Before joining National, he was a consultant with Arthur D Little Inc in analog systems and circuits. From 1968 to 1977, Jim directed the Instrumentation Development Lab at the Massachusetts Institute of Technology, where in addition to designing experimental biomedical instruments, he was active in course development and teaching. A former student of psychology at Wayne State University, he lists tennis, art and collecting antique scientific instruments as his leisure interests.