Wideband peak detector operates over wide input-frequency range

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This Design Idea builds on a previous one (**Reference 1**) to realize a precision peak detector with a bandwidth of 15 to 30 MHz or more, depending on the maximum input-signal level of your application. The crucial feature of this Design Idea is an ultrafast comparator that provides the high slew rate and low propagation delay that this application requires. The comparator in this design is the Analog Devices (www.analog.com) AD8561, a 7-nsec device (**Reference 2**). This peak detector provides accuracy from 100 Hz to more than 14 MHz at input-signal levels of 100 mV p-p to 6V p-p. At higher frequencies, the maximum usable input-signal level decreases. The circuit exhibits an accuracy of ±3% over much of the input-level range. Also, its high input impedance of about 100 kΩ in parallel with 3 pF does not significantly load the circuit under test in many applications; 3 pF results in an impedance of 3.5 kΩ at 15 MHz.

Referring to **Figure 1**, the high-input-impedance buffer comprising IC_1 and its associated components provides the ac signal to the ultrafast comparator, IC_3. The output of IC_1 centers on 0V dc by the action of op amp IC_{2A} and its associated components, which sample the dc level at Pin 6 of IC_1 and then provide a dc-correction voltage to Pin 3 of IC_1. This action virtually eliminates the effects of IC_1's input-offset voltage and input-bias currents. R_1, R_4, and C_1 provide a small amount of gain boost as the frequency increases to 25 MHz, and C_5 then begins to roll off the gain.

The input signal capacitively couples to the input buffer, so, for proper operation, the input-ac signal must have a symmetrical waveform, such as a sine wave. An unsymmetrical waveform has a shift in its peak value after passing through C_2, and, as a result, the output of the peak detector will be inaccurate.

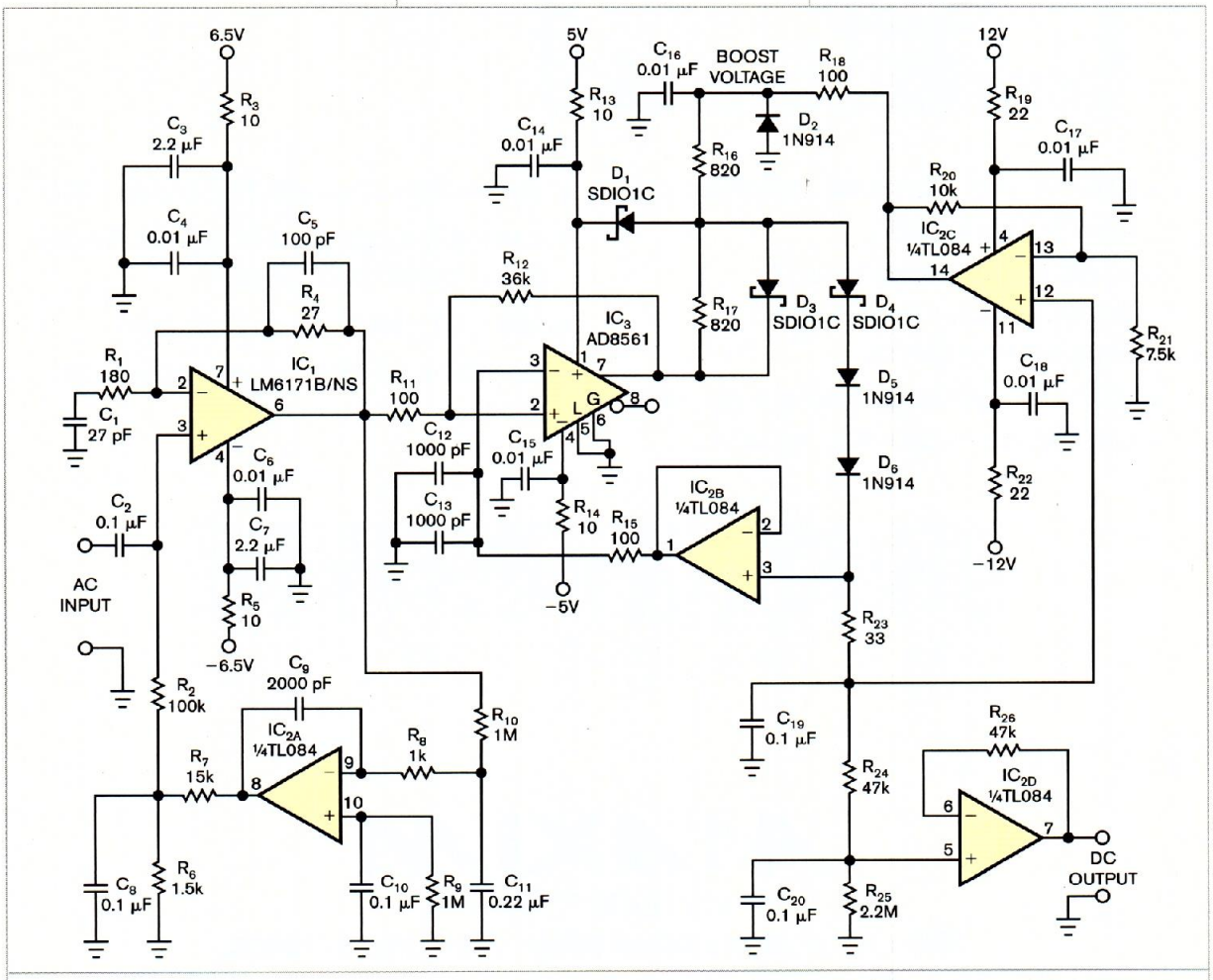

Figure 1 This precision peak detector uses an ultrafast comparator to achieve high accuracy over a wide input-frequency range.

The output of comparator IC_3 swings high when the input at Pin 2 is higher than the dc level at Pin 3. This action, in turn, charges holding capacitor C_{19} through R_{17}, D_4, D_5, D_6, and R_{23}. When the voltage on C_{19} is higher than the peak signal level at Pin 2 of IC_3, the comparator stops providing charging pulses at its output. At equilibrium, the comparator provides output pulses with the correct amplitude and width to maintain the voltage on C_{19} at approximately the peak level of the input signal. The high-input-impedance dc buffer, IC_{2B}, minimizes the discharging of C_{19} between charging pulses.

The network comprising R_{24}, R_{25}, and C_{20} filters and attenuates the dc output by 2.1%. This attenuation is necessary because the output tends to be slightly higher than the actual peak level of the input signal at Pin 3 of IC_1. The circuitry comprising IC_{2C} and its associated components provides a novel feature: a voltage boost at Pin 14 of IC_{2C} as the voltage on holding capacitor C_{19} increases. The circuitry then applies this voltage boost to R_{16}, which in turn causes the voltage swing at the junction of R_{16} and R_{17} to increase as the charge on C_{19} increases. This action causes the amplitude of the pulses driving D_4 to increase. This action maintains a relatively constant drive to C_{19} as its charge increases.

Diode D_1 keeps the voltage at the output of IC_3 from exceeding its supply voltage. Diode D_2 keeps the boost voltage from going to a large negative level at start-up, which could cause the circuit to latch up. The switching action of the comparator and diode D_3 prevents latch-up due to a large positive-boost transient. This circuit exhibits no indication or tendency for instability. The maximum input signal is 6V p-p because of the input common-mode-voltage specification of the AD8561 comparator. The supply voltages for the input buffer are ±6.5V to avoid the possibility of severely overdriving the comparator.

You can improve the precision of the circuit by substituting a 100-kΩ potentiometer for R_4 to provide an output-level adjustment, and a dc-offset adjustment would improve accuracy at low signal levels.

This circuit used a 300-MHz-bandwidth oscilloscope to make the performance measurements. As a result, the data in **Table 1**, which is available in the online version of this Design Idea at www.edn.com/071122di1, may include some measurement errors. Therefore, take the results in the **table** as representing the circuit's performance rather than as precise data. The data is simply the result of the best equipment on hand when the measurements were made. **EDN**

REFERENCES

1. McLucas, Jim, "Precision peak detector uses no precision components," *EDN*, June 10, 2004, pg 102, www.edn.com/article/CA421510.
2. "AD8561 ultrafast 7 ns single supply comparator," Analog Devices, www.analog.com/UploadedFiles/Data_Sheets/AD8561.pdf.