Ultra-responsive peak detector

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The peak detector presented here will respond to amplitude changes of the input signal within one-half of a cycle. Because no 'bleed' resistor is required on the output capacitor, droop is only limited by the 'off' resistance of a CMOS switch. Note that circuit is more accurately described as an *amplitude detector*, as the output level is equal to the average of the absolute values of the positive and negative amplitudes. For a sinusoidal input waveform, this corresponds to the peak detect function.

Positive and negative peaks are measured separately. Whilst the positive peak is being acquired, the negative peak is output, or vice versa. At the time a positive-going zero-crossing is detected, the positive peak detector is reset, and similarly for negative signals.

There are two key subcircuits. One is a peak detector, the other is a zero-crossing detector (ZCD). There are two instances of each type, corresponding to the two possible signs of the input signal. Note that all detectors (of both types) give a positive output.

When +ZCD goes high, this causes a brief pulse to reset the positive-peak detector. The reset has no effect on V_{OUT}, since the high level of the +ZCD means that the negative peak detector is connected to V_{OUT} at this time.

During this (positive) half of the input cycle, the +peak detector continuously registers the most positive input signal to date until such a time as it is reset.

Now consider what happens over the negative-going excursion of the input signal. Firstly, +ZCD goes Low, then –ZCD goes High. In the short interval that both are Low, the output capacitor is isolated. When +ZCD goes Low, V_{OUT} is removed from the negative peak detector output, and because –ZCD is high, V_{OUT} is instead connected to the positive peak detector output.

The negative peak detector operates in the same way as described above for the positive one, but because it sees an inverted copy of V_{IN}, it gives a positive (absolute value) output, as required.

The circuit shown is suitable for low frequencies up to a few kHz. The AD8534 is specified as unity-gain stable for capacitive loads of up to 10 nF. Empirically, it was found that even an ordinary opamp such as the LMC6484 gave no problems with ringing at V_{OUT}; possibly the 'on' resistance of the switch in the 74HC4066 helped to isolate the output capacitor.

One speed restriction is the width of the reset pulse. It would be possible to use a monostable instead of the RC network. In order to allow short reset times, the MOS switches used here to short the peak detect capacitors could be supplemented with discrete, low $R_{DS(ON)}$ NMOS transistors, such as TN0200K. If necessary, dedicated comparators may be used for the ZCD sections.

Current consumption could also be reduced. Firstly, by swapping the comparator inputs around — the 'working' comparator inputs are high-impedance. If this is done, be sure to invert the BAT54 diodes as well. Of course, now we have an inverted output to the peak detector, i.e.

$V_{OUT} = -V_{PEAK}$

Lastly, if desired the inverting opamp stage may be amended to use 100 kΩ resistors.

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