Digital peak detector finds 4-bit highs and lows

by N. Bhaskara Rao
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This circuit finds the maximum and minimum value of a 4-bit data signal over any given time interval. Here, a latch-comparator feedback scheme using standard TTL operates as a real-time memory bank to determine the peaks and valleys of the input signal.

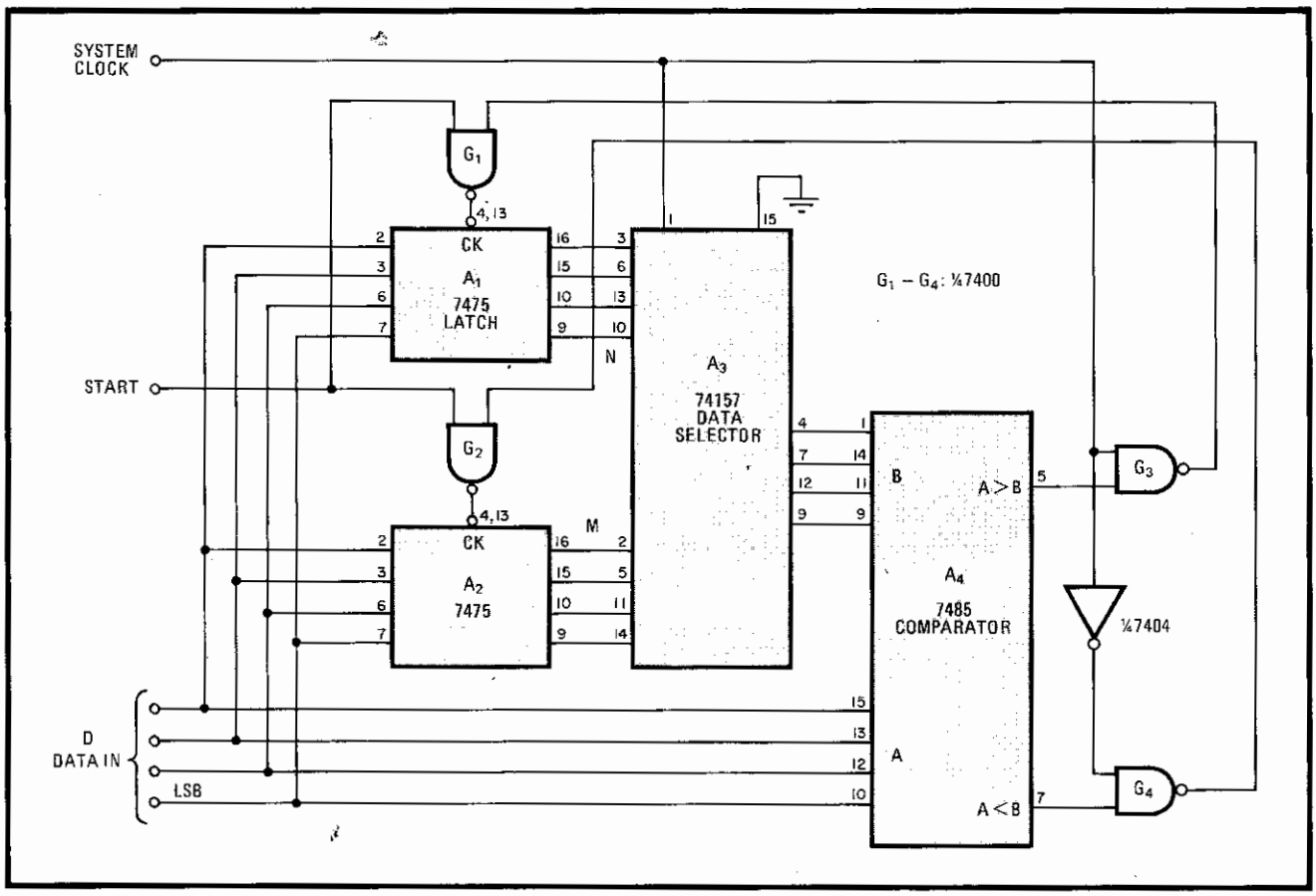
A negative-going start pulse latches the incoming data, D, in A_1 and A_2 at the beginning of the sample period. Thus initially, $D_o = N_o = M_o$, where N and M are the stored maximum and minimum data values, respectively.

When the system clock first moves high, gate G_3 is enabled and N_o appears at the output of the data selector, A_3. N_o is then compared to the present value of the input data at A_4. If D should exceed N_o, pin 5 of A_4 will go high and A_1 will therefore latch the input data.

Similarly, when the system clock first moves low, gate G_4 is enabled and A_4 compares M_o to the present data value. If D is less than M_o, A_2 will latch the input data. This process is repeated during each system clock until the end of the sample period, which may be terminated by the user in any of several ways, depending on the application. The maximum and minimum values of D appear at the output of A_1 and A_2, respectively.

No difficulties have been encountered with the generation of signal spikes or transients from pins 5 and 7 of A_4 during A_3's switching periods, and no problems will occur as long as the data-input lines are settled during those times. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Peaks and valleys. Maximum/minimum detector for 4-bit digital data uses standard TTL elements in latch-comparator feedback arrangement. Circuit performs continual comparison of previously stored maximum and minimum data versus present value of input data, and relatches latter when necessary. Updated high and low values appear at output of A_1 and A_2, respectively.

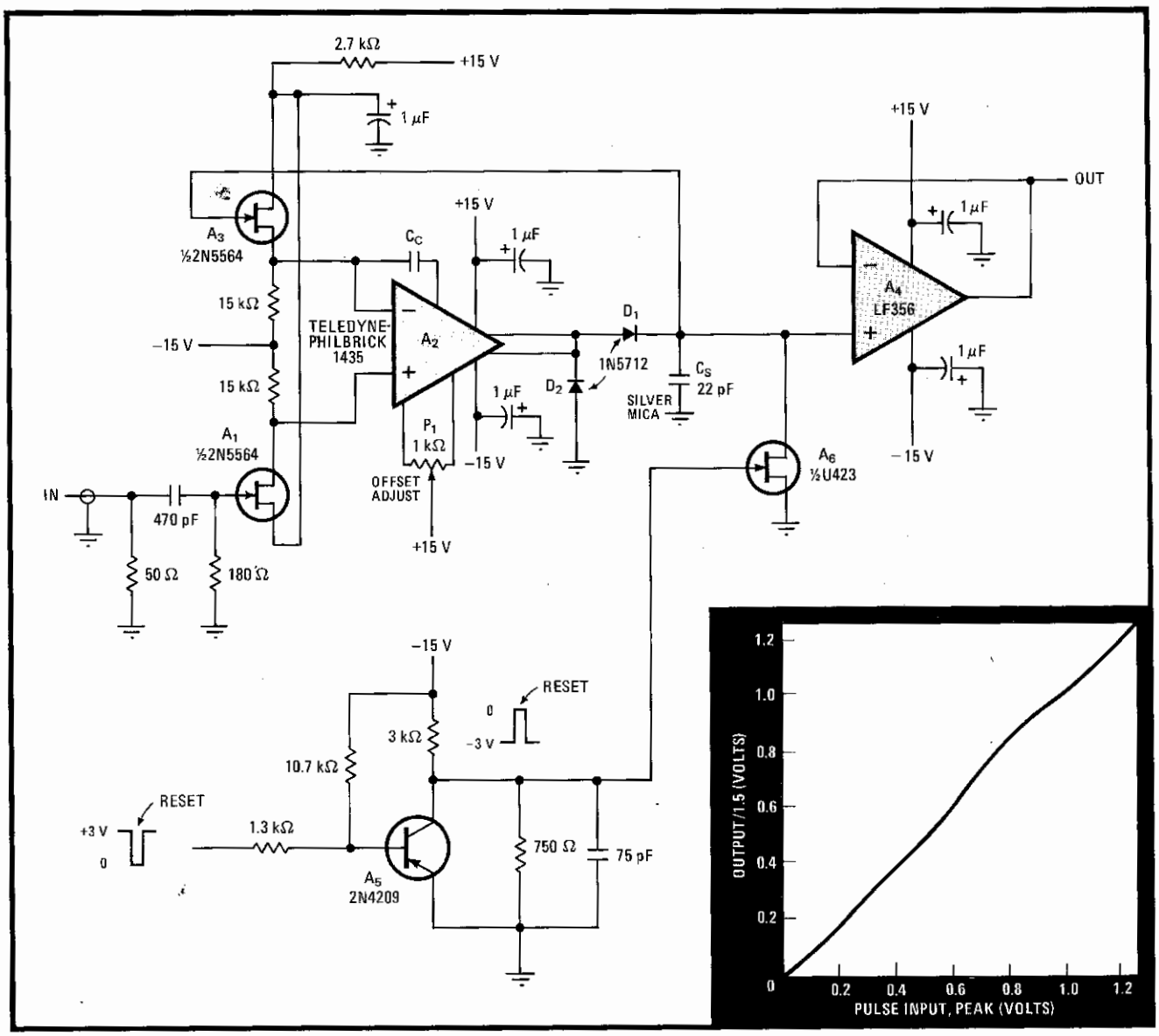
Wideband peak detector recovers short pulses

by Saul Malkiel
Advanced Technology Systems, Roselle, N. J.

Using a Schottky-barrier diode for detection and a wideband operational amplifier, this peak detector recovers data pulses as narrow as 10 nanoseconds in the range of 0.1 to 1.3 volts. The circuit's linearity as a percentage of the full scale output is 4%.

The input signal, whose rise time is assumed to be a minimum of 10 ns, is applied to one side of the differential source follower, A_1-A_3, via a 50-ohm coaxial cable. A blocking capacitor removes any baseline shifts. The output of this JFET follower is then applied to the wideband amplifier, A_2. The amplifier has a gain-bandwidth product of 1 gigahertz.

The output of the amplifier switches on diode detector D_1 so that a charging current can be delivered to storage capacitor C_s. When there is overshoot, source follower A_3 is turned on more heavily than A_1 so that A_2 may be driven negative. D_2 then comes into play, acting to limit the amplifier's negative excursion. The excursion, coupled through D_1's shunt capacitance, reduces the



Narrow capture. Wideband amplifier and fast diode detect pulses having widths as small as 10 ns. Output-to-input voltage linearity of circuit is 4%, and linearity is virtually independent of pulse width. Response is illustrated in curve at bottom right.

output voltage by 30 millivolts. This pullback effect is one cause of error in small-signal detection.

The storage capacitor is a silver-mica type, chosen for its low loss and its high stability. Its value is 22 picofarads, a tradeoff between A_2's hold-drift (100 microvolts per microsecond) and pullback characteristics.

The detected voltage is now applied to A_4, which serves as a buffer and provides a low-output impedance for driving the external circuitry. The LF356 operational amplifier used has wideband characteristics, notably a settling time of approximately 200 ns, after which its output becomes valid.

A pulsed command can then be applied to the 2N4209 transistor, A_5, to reset the circuit. The reset command is then transferred to A_6, the U423, and the stored voltage on C_s discharges exponentially toward zero. In order to minimize the discharge time, the output of A_2 is biased at 10 mV dc under no-signal conditions. Potentiometer P_1 is used to adjust the required offset. A total time of about 2 microseconds is required to reset the circuit. □

Peak and trough detector

In data-logging systems it is often necessary to measure the peak and trough of a waveform superimposed on a d.c. level. This circuit uses two i.cs and offers acceptable performance down to about 10Hz. Measurements are made with a conventional d.c. voltmeter.

Input signals are fed to a precision peak detector, which outputs the peak voltage "max". The input signal is also passed through an active low pass filter and inversion amplifier, whose output at TP2 is the mean value. A differential amplifier subtracts the maximum value from the mean, to give the minimum value of the input. A compromise is necessary between response time and lowest operating frequency but the 100μF capacitor can be reduced for higher speed operation. The circuit is set up by shorting the input and adjusting R_1 until 0V ± 1mV appears at TP1. Resistor R_2 is then adjusted so that 0V also appears at TP2. With +5V ±1mV applied to the input, R_3 is adjusted until TP1 measures +5V ±1mV, and R_4 is adjusted until TP2 measures −5V ±1mV. Finally, R_5 is adjusted until +5V ±1mV appears at the "max" output.

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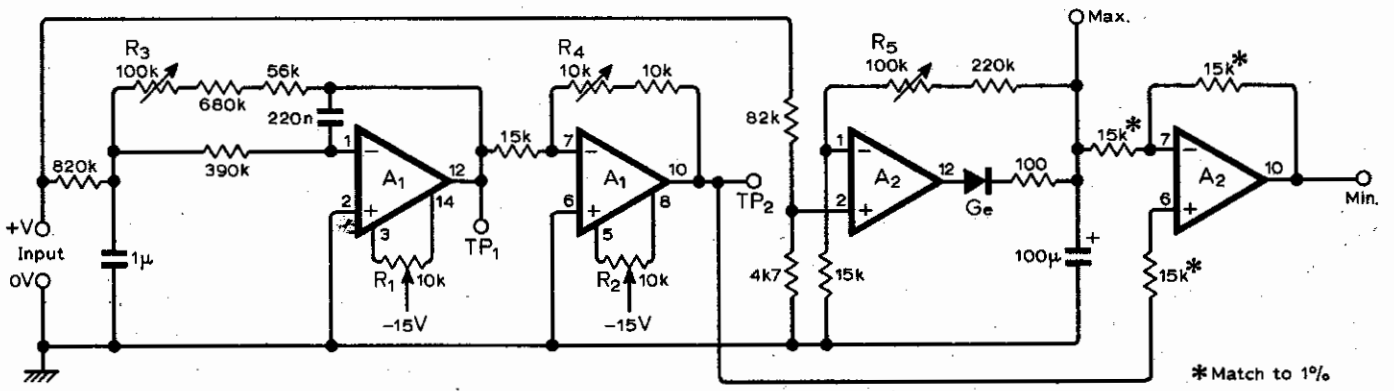

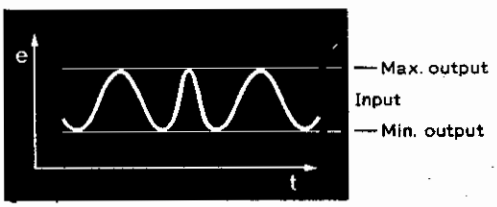

A_1 and A_2 I.c. type LM747CN (dual 741)

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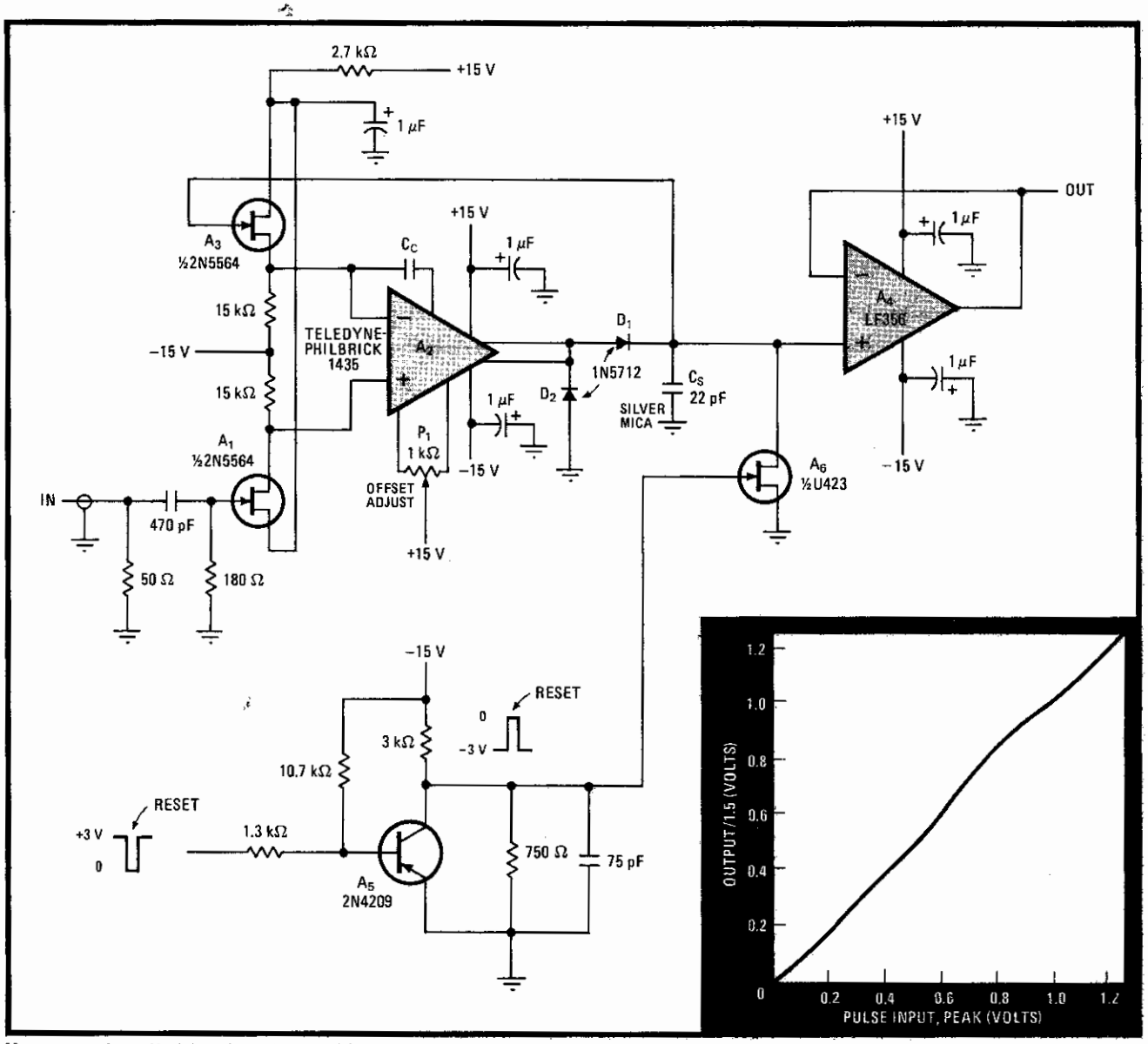

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Peak detector recovers narrow pulses accurately

by Jerome Leiner
Loral Electronic Systems, Yonkers, N. Y.

This peak detector can accurately process input data pulses as narrow as 50 nanoseconds and as high as 3 volts. The recovered voltage is always within 1% of the input signal's true value.

In the circuit shown, emitter-coupled logic generates a −0.2- to −3-volt signal for input into amplifier A_1. Assuming a pulse with a 50-nanosecond width and a rise and fall time of 5 ns, that leaves storage capacitor C_4 only 45 ns in which to charge. The LH0024 op amp used for A_1 has wide bandwidth and a high slew rate to accommodate the fast charging required.

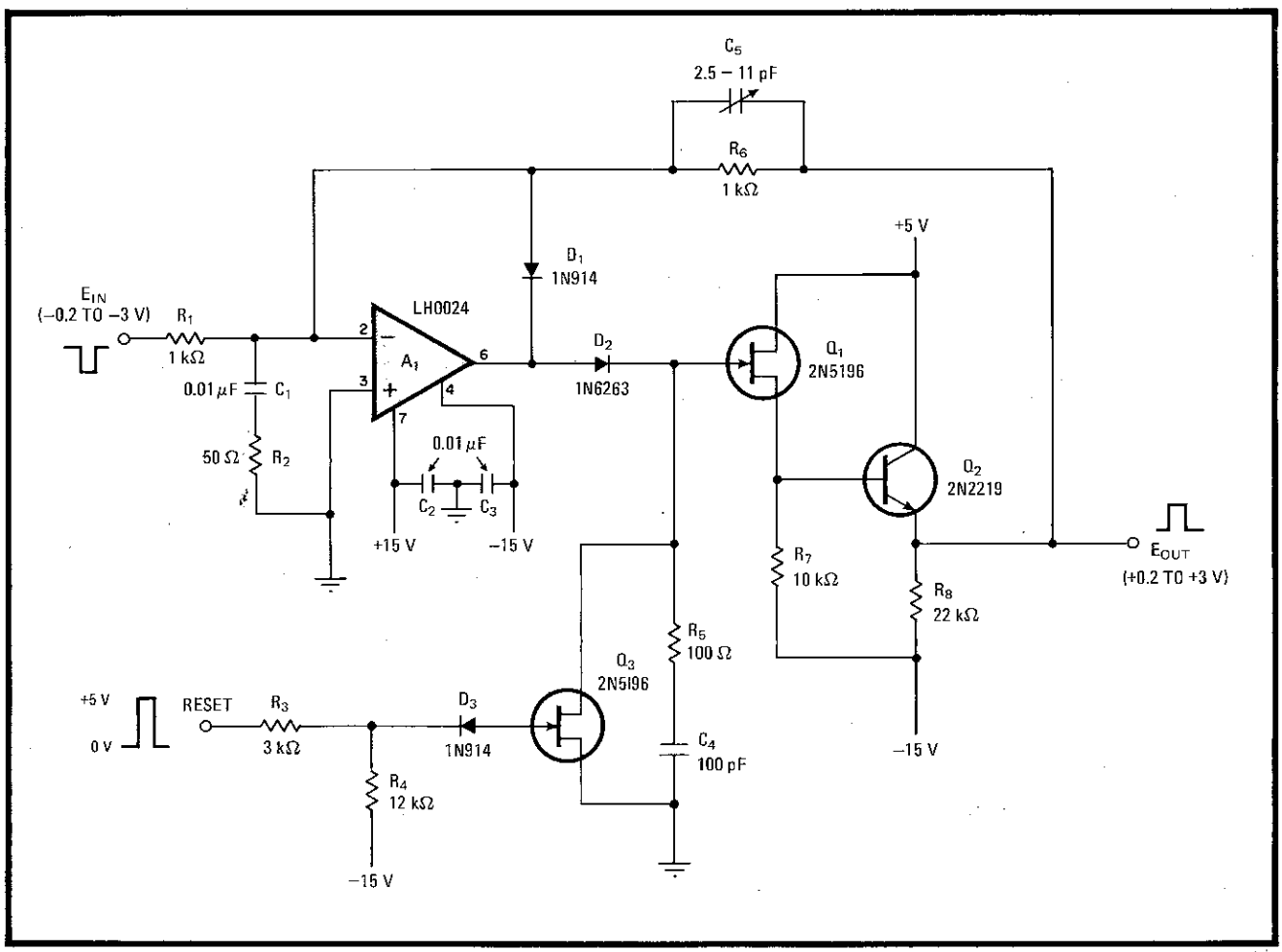
Q_1 acts as a buffer to prevent C_4 from discharging through R_7 between system reset pulses. The voltage at Q_1 appears at Q_2 and is fed back to A_1, to be compared with E_{in}. When E_{out} reaches E_{in}, D_2 becomes back-biased and the stored charge is held until C_4 is intentionally discharged by the reset signal. D_2 remains back-biased during discharge.

A_1 is normally used as an amplifer, and so it will be driven into negative saturation whenever the input signal drops below the output level. D_1 prevents this by clamping the amplifier output.

C_1 and R_2 provide A_1 with input- and feedback-signal stabilization. C_5 compensates for A_1's input capacitance. Note that if C_1R_2 were placed at the output of A_1, a larger charging current would be required for a given input signal. Because this current is usually limited, A_1's effective slew rate would be reduced.

The peak detector is optimized by shorting D_2 and then adjusting C_1, R_2, and C_5 for minimum overshoot and ringing on a series of fast data pulses. □

Fast and precise. Using one op amp, one transistor, and two field-effect transistors, peak detector recovers data pulses having amplitudes of up to 3 volts and widths as narrow as 50 nanoseconds. Output voltage is within 1% of the input data's true value under all signal conditions.



Video detector stores peak for minutes

by Stephen Hayes
Altadena, Calif.

In slow-scan image processing, a video signal often must hold its peak value for longer than the few seconds provided by diode peak rectifiers. But a rectifier that can retain a peak value of a video signal for up to four minutes can be built from two operational amplifiers and two transistors, avoiding the cost and complexity of digital storage for a sample-and-hold circuit.

In the circuit shown in Fig. 1, the CA3100 op amp compares the input signal (between 0 and 6 volts) to the voltage on a 0.47-microfarad plastic capacitor. The output of the CA3100 is an amplified error signal used to adjust the charge on the storage capacitor.

The storage and output sections are conventional. A MOSFET operational amplifier, the CA3130, with the twin assets of low cost and low input bias current, acts as a unity-gain buffer between the capacitor and the output terminal. The 2.2-kilohm resistor lowers the output impedance from the very high level of the 3130.

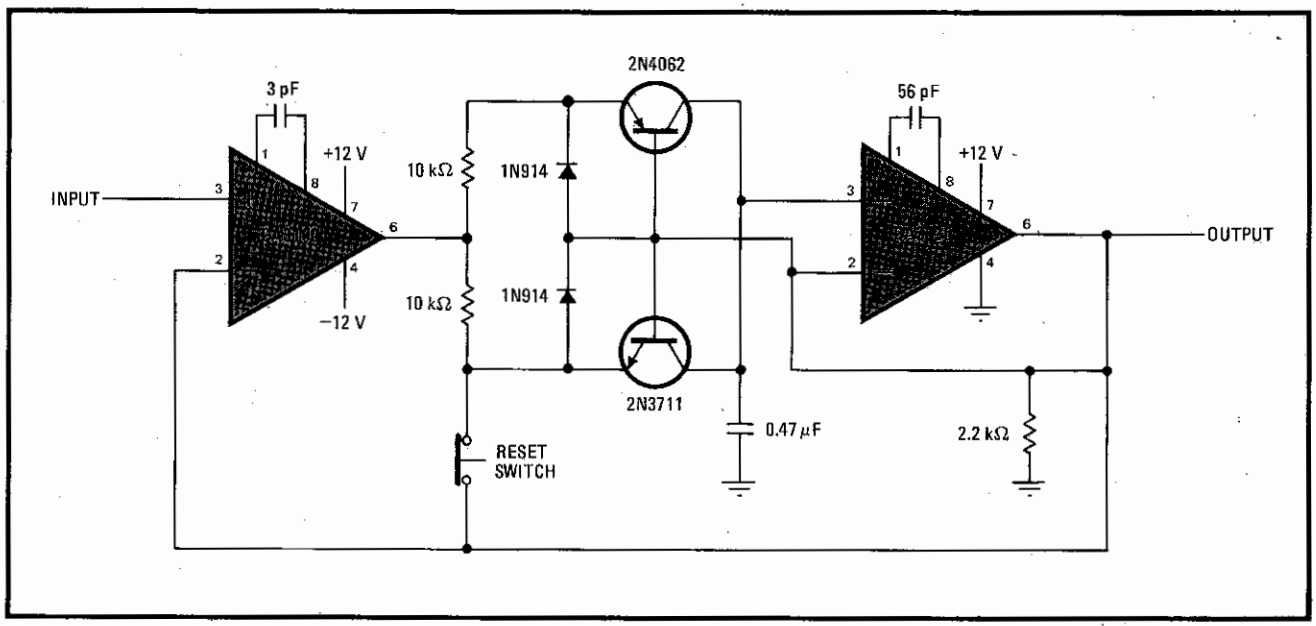
The key feature of the circuit is the unusual method of transferring charge into and out of the capacitor. Normally, a peak rectifier uses a series diode for this purpose. However, the diode has a reverse leakage current that is unpredictable, temperature-dependent, and often on the order of several nanoamperes. To avoid this leakage, the circuit shown uses the base-collector junction of a pnp transistor to transfer charge. The current is injected into the emitter, with the base connected to the output of the buffer amplifier. As a result, the base-collector voltage is close to zero, and collector leakage current is small.

An npn transistor is added to allow the capacitor to be discharged. Normally, this transistor does not conduct because its base-emitter junction is shorted by the switch. Thus, when the switch is closed, the output voltage (which is equal to the voltage across the capacitor) is determined by the most positive level applied to the input terminal. When the switch is open, the output voltage tracks the input signal (Fig. 2).

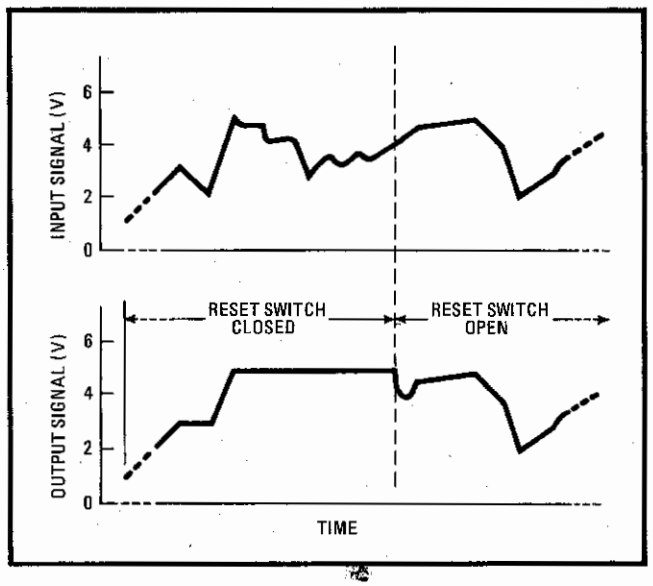
Holding performance of the circuit is quite good. If a 3-V signal is applied and removed, the output decays less than 10 millivolts in 10 minutes. This implies that the total leakage current into the capacitor is less than 10 picoamperes.

A drawback is the low slew rate. The minimum slew rate is set by the 10-kilohm resistors, the 0.47-μF capacitor, and the difference between the maximum output voltage of the CA3100 and the maximum signal voltage. With a 6-V input signal, the slew rate is about 850 V/s.

Several variations on the circuit are possible. The switch could be replaced by an electronically controlled device, such as a relay or a CD4016 complementary-metal-oxide-semiconductor transfer gate. This change



1. Stores maximum level. Peak detector circuit accepts analog input signals of 0 to 6 V in amplitude, provides output level that is maximum value of input. Use of pnp transistor for rectification minimizes charge leakage from capacitor, so peak level can be held for several minutes. Switch and npn transistor allow circuit to be reset. While reset switch is open, output signal follows input signal. If the reset switch is relocated to short the emitter to the base on the pnp transistor, the circuit is a minimum level detector, storing the lowest level of the input signal.



2. Holding the peak. Output from circuit of Fig. 1 is the highest level that has been applied to the input since switch was closed. If switch is opened, output slews down to input level, and then follows input. Circuit was developed for determining dynamic range of low-bandwidth scanning signal from an electron microscope, but is useful for any peak rectifier that requires low decay rate.

would allow electronic control of the reset function.

If the switch is moved to the emitter of the npn transistor, the circuit stores the lowest level of the input signal. If switches are placed in both locations, the circuit can function in four modes: tracking (both switches open), positive peak detector, minimum level detector, and holding (both switches closed).

By using both a positive peak detector and a minimum level detector in a circuit, maximum and minimum voltage levels can be stored for such purposes as setting the gains of variable-gain amplifiers, or storing the levels of transient peaks in a signal. □