LINEAR TECHNOLOGY

DESIGN NOTES

Peak Detectors Gain in Speed and Performance – Design Note 61

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Introduction

Fast peak detectors place unusual demands on amplifiers. High slew rate is needed to keep the amplifier internal nodes from overracing the output stage. This condition causes either a long overload, or DC accuracy errors. To support the high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Compounding these problems are issues of amplifier instability with a large capacitive load, as well as the accuracy of the output voltage.

Detecting Sinewaves

The LT1190 is the ideal candidate for this application, with a high 400V/µs slew rate, large 50mA output current, and a wide 70 degree phase margin. The closed-loop peak detector circuit of Figure 1 uses a Schottky diode inside the feedback loop to obtain good accuracy. The 20Ω resistor R_O isolates the 0.01µF load and prevents oscillation. The DC error with a sinewave input is plotted in Figure 2 for various input amplitudes. The DC value is read with a DVM. At low frequency, the error is small and dominated by decay of the detector capacitor between cycles. As frequency rises the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sinewave cycle. Finally at approximately 4MHz the error rises rapidly due to the slew rate limitation of the op amp. For comparison purposes the error of an LM118 is also plotted for $V_{IN} = 2V_{P-P}$.

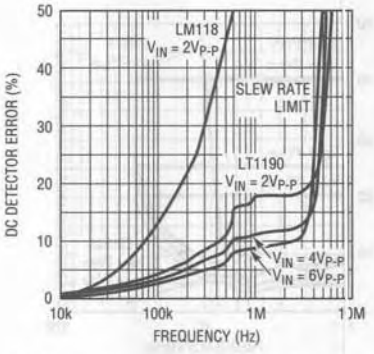

Figure 2. Closed-Loop Peak Detector Error vs Frequency

A fast Schottky diode peak detector can be built with a 1000pF capacitor, and 10k pull down. Although this simple circuit is very fast, it has limited usefulness due to the error of the diode threshold, and its low input impedance. The accuracy of this simple circuit can be improved with the LT1190 circuit of Figure 3. In this open-loop design, the detector diode is D1, and a level shifting or compensating diode is D2. A load resistor R_L is connected to –5V, and an identical bias resistor R_B is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1k to 10k) provide fast response, but at the expense of poor low frequency accu-

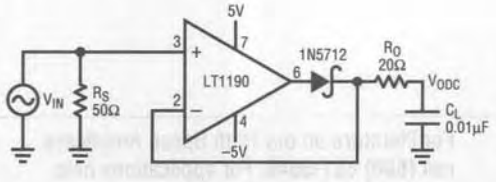

Figure 1. Closed-Loop Peak Detector

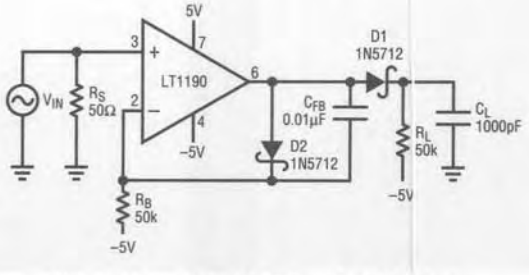

Figure 3. Open-Loop High Speed Peak Detector

be made by adding a feedback capacitor C_{FB} which enhances the negative slew rate on the (–) input. The DC error with a sinewave input is plotted in Figure 4 and is read with a DVM. For comparison purposes the LM118 error is plotted as well as the error of the simple Schottky detector.

Detecting Pulses

A fast pulse detector can be made with the circuit of Figure 5. A very fast input pulse will exceed the amplifier slew rate and cause a long overload recovery time.

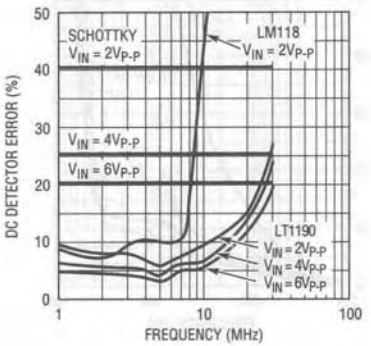

Figure 4. Open-Loop Peak Detector Error vs Frequency

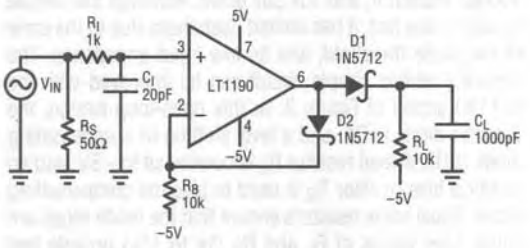

Figure 5. Fast Pulse Detector

Figure 6 shows the detector error vs pulse width. Figure 7 is the response to a 4V_{P-P} input that is 80ns wide. The maximum output slew rate in the photo is 70V/µs. This rate is set by the 70mA current limit driving 1000pF. As a performance benchmark, the LM118 takes 1.2µs to peak detect and settle the same amplitude input. This slower response is due in part to the much lower slew rate and lower phase margin of the LM118.

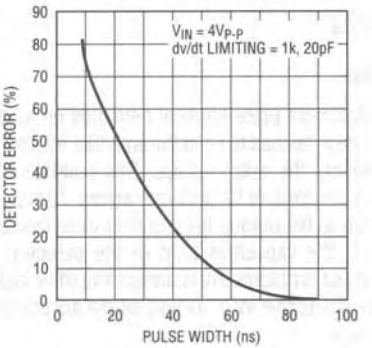

Figure 6. Detector Error vs Pulse Width

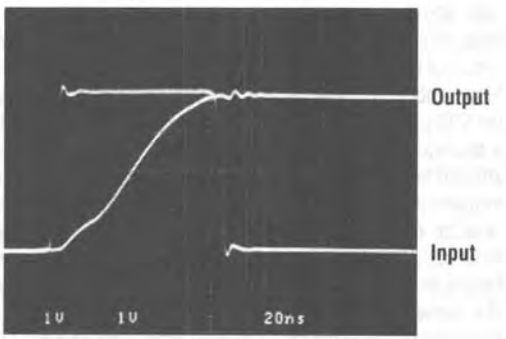

Figure 7. Open-Loop Peak Detector Response

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