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What does “rail to rail” input operation really mean?

A hot discussion topic with single-supply operational amplifiers is whether they are capable of rail-to-rail input or output operation. Vendors of single-supply op amps claim their amplifiers have rail-to-rail input capability, but the chip designer has to make some compromises to achieve this type of performance.

A common single-supply amplifier input topology has parallel PMOS and NMOS differential input stages, combining the advantages of those stages to achieve actual rail-to-rail input operation (Figure 1). When you bring V_{IN+} toward the negative rail, the PMOS transistors are completely on, and the NMOS transistors are completely off. When you bring the input terminals to the positive rail, the NMOS transistors are in use, and the PMOS transistors are off.

Although the precision, low-power OPA344 input stage in Figure 1 has rail-to-rail input operation, there are

performance compromises that the circuit designer must address. The design topology in Figure 1 can have wide variations in offset voltage across the amplifier's common-mode input range. In the region near ground, the PMOS offset-error portion of the input stage is dominant. In the region near the positive power supply, the NMOS offset error dominates.

The best way to view the input stage's behavior is to look at the offset voltage versus the common-mode input voltage (Figure 2). The 4.6-MHz, rail-to-rail input/output LMP7701 CMOS amplifier in Figure 2 exhibits the offset-

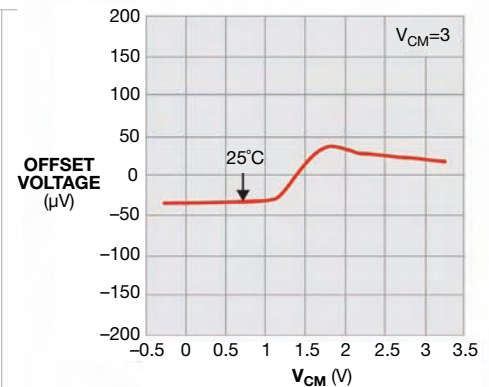


Figure 2 As the amplifier's common-mode voltage changes from ground to the positive supply, the input stage of the CMOS amplifier completely changes from its PMOS input pair to its NMOS input pair at $-2V$ below the $3V$ positive supply rail.

voltage-error crossover behavior around $1.4V$. At lower common-mode input voltages, the PMOS transistors are in operation, with the NMOS transistors turned off. At approximately $1.1V$, the NMOS transistors start to turn on. As the common-mode input voltage increases, the NMOS section of the circuit finally takes over, with the PMOS transistors completely off. From approximately 1.1 to $2V$, both the PMOS and NMOS transistors are operating.

There are circuit-design tricks at your disposal for minimizing this input-stage crossover effect; you can read about them in “Rail-to-rail input amplifier application solutions” (www.edn.com/4400221).

Single-supply amplifier manufacturers also claim they have devices that will swing rail-to-rail on the output. With those types of amplifiers, the output cannot go all the way to the rails, but it can get close.

Next time, I'll talk about the rail-to-rail amp's output stage and its ability to achieve rail-to-rail performance. **EDN**

REFERENCES

- 1 OPA344 data sheet, Texas Instruments, www.ti.com/opa344-ca.
- 2 LMP7701 data sheet, Texas Instruments, www.ti.com/lmp7701-ca.

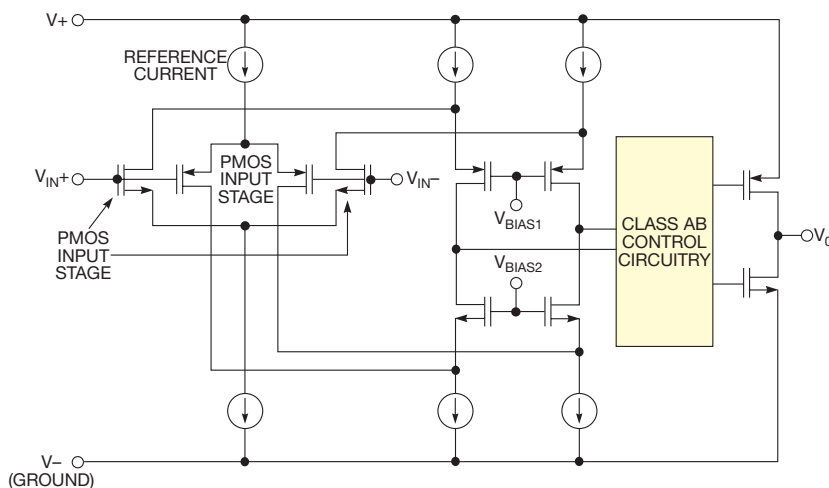


Figure 1 This composite input stage of the op amp uses PMOS and NMOS differential pairs so the input-voltage range can extend from above the positive rail to below the negative rail.