SECTION 7-4

Op Amp Protection

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Frequently, op amps and other analog ICs require protection against destructive potentials at their input and output terminals. One basic reason behind this is that these ICs are by nature relatively fragile components. Although designed to be as robust as possible *for normal signals*, there are nevertheless certain application and/or handling conditions where they can see voltage transients beyond their ratings. This situation can occur for either of two instances. The first of these is *in-circuit,* that is, operating within an application circuit. The second instance is *out-of-circuit,* which might be at anytime after receipt from a supplier, but prior to final assembly and mounting of the IC. In either case, under over-voltage conditions, it is a basic fact of life that unless the designer limits the fault currents at the input (or possibly output) of the IC, it can be damaged or destroyed.

So, obviously, the designer should fully understand all of the fault mechanisms internal to those ICs that may require protection. This then allows design of networks that can protect the in-circuit IC throughout its lifetime, without undue compromise of speed, precision, and so forth. Or, for the out-of-circuit IC, it can help define proper protective handling procedures until it reaches its final destination. This section of the chapter examines a variety of protection schemes to ensure adequate protection for op amps and other analog ICs for in-circuit applications, as well as for out-of-circuit environments.

In-Circuit Overvoltage Protection

There are many common cases that stress op amps and other analog ICs at the input, while operating within an application, i.e., in-circuit. Since these ICs must often interface with the outside world, this may entail handling voltages exceeding their absolute maximum ratings. For example, sensors are often placed in environments where a fault condition can expose the circuit to a dangerously high voltage. With the sensor connected to a signal processing amplifier, the input then sees excessive voltages during a fault.

General Input Common-Mode Limitations

Whenever an op amp input common-mode (CM) voltage goes outside its supply range, the op amp can be damaged, even if the supplies are turned off. Accordingly, the absolute maximum input ratings of almost all op amps limits the greatest applied voltage to a level equal to the positive and negative supply voltage, plus about 0.3 V beyond these voltages (i.e., $+V_S$ + 0.3 V, or $-V_S$ – 0.3 V). While some exceptions to this general rule might exist it is important to note this: *Most IC op amps require input protection when over-voltage of more than 0.3 V beyond the rails occurs.*

A safe operating rule is to always keep the applied op amp CM voltage between the rail limits. Here, "safe" implies prevention of outright IC destruction. As will be seen later, there are also intermediate "danger-zone" CM conditions between the rails with certain op amps, which can invoke dangerous (but not necessarily destructive) behavior.

Speaking generally, it is important to note that almost *any* op amp input will break down, given sufficient overvoltage to the positive or negative rail. Under breakdown conditions high and uncontrolled current can flow, so the danger is obvious. The exact breakdown voltage is entirely dependent on the individual op amp input stage. It may be a 0.6 V diode drop, or a process-related breakdown of 50 V or more. In many cases, overvoltage stress can result in currents over 100 mA, which destroys a part almost instantly.

Therefore, unless otherwise stated on the data sheet, op amp input fault current should be limited to ≤5 mA to avoid damage. This is a conservative rule of thumb, based on metal trace widths in a typical op amp input. Higher levels of current can cause *metal migration*, a cumulative effect, which, if sustained, eventually leads to an open trace. Should a migration situation be present, failure may only appear after a long time due to multiple overvoltages, a very difficult failure to identify. So, even though an amplifier may appear to withstand overvoltage currents well above 5 mA for a short time period, it is important to limit the current to 5 mA (or preferably less) for long term reliability.

Figure 7-65 illustrates an external, general-purpose op amp CM protection circuit. The basis of this scheme is the use of Schottky diodes D1 and D2, plus an external current limiting resistor, R_{LIMIT}. With appropriate selection of these parts, input protection for a great many op amps can be ensured. Note that an op amp may also have *internal* protection diodes to the supplies (as shown) which conduct at about 0.6 V forward drop above or below the respective rails. In this case however, the external Schottky diodes effectively parallel any internal diodes, so the internal units never reach their threshold. Diverting fault currents externally eliminates potential stress, protecting the op amp.

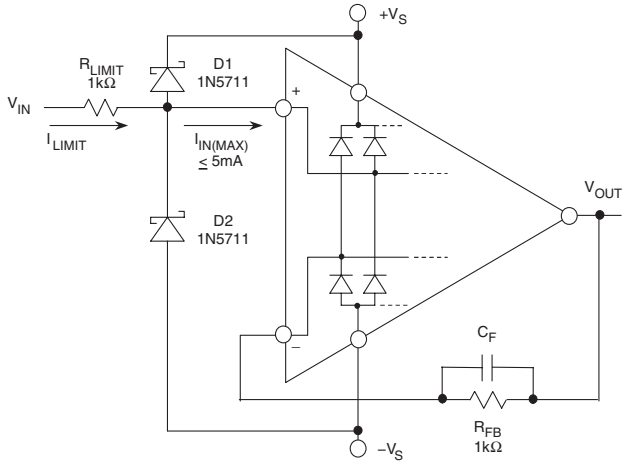


Figure 7-65: A general-purpose op amp CM overvoltage protection network using Schottky clamp diodes with current limit resistance

The external diodes also allow other degrees of freedom, some not so obvious. For example, if fault current is allowed to flow in the op amp, R_{LIMIT} must then be chosen so that the maximum current is no more than 5 mA for the worst case V_{IN}. This criterion can result in rather large R_{LIMIT} values, and the associated increase in noise and offset voltage may not be acceptable. For instance, to protect against a V_{IN} of 100 V with the 5 mA criterion, R_{LIMIT} must be ≥20 kΩ. However with external Schottky clamping diodes, this allows R_{LIMIT} to be governed by the maximum allowable D1-D2 current, which can be larger than 5 mA. However, care must be used here, for at very high currents the Schottky diode drop may exceed 0.6 V, possibly activating internal op amp diodes.

It is very useful to keep the R_{LIMIT} value as low as possible, to minimize offset and noise errors. R_{LIMIT}, in series with the op amp input, produces a bias-current-proportional voltage drop. Left uncorrected, this voltage appears as an increase in the circuit's offset voltage. Thus for op amps where the bias currents are moderate and approximately equal (most bipolar types), compensation resistor R_{FB} balances the dc effect, and minimizes this error. For low bias current op amps (Ib ≤10 nA, or FET types) it is likely R_{FB} won't be necessary. To minimize noise associated with R_{FB}, bypass it with a capacitor, C_F.

Clamping Diode Leakage

For obvious reasons, it is critical that diodes used for protective clamping at an op amp input have a leakage sufficiently low to not interfere with the bias level of the application.

Figure 7-66 illustrates how some well-known diodes differ in terms of leakage current, as a function of the reverse bias voltage, Vbias.

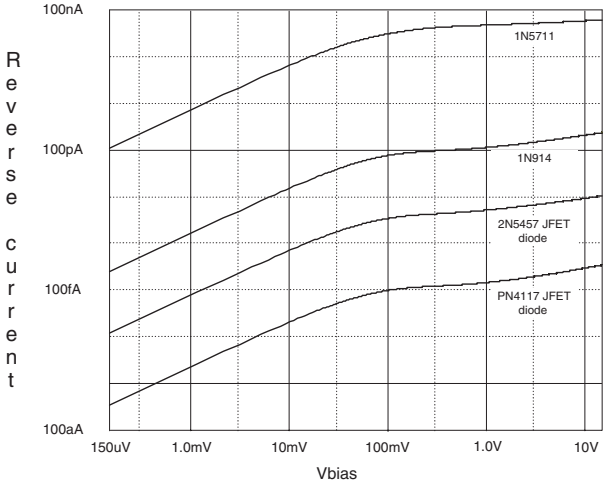


Figure 7-66: Reverse bias current characteristics for diodes useful in protective clamping networks (PSpice simulation)

In this chart, a 25°C simulation using PSpice diode models, it is easy to see that not only is the diode type critical, so is the reverse bias. The 1N5711 Schottky type for example, has a leakage of nearly 100 nA at a reverse bias of 15 V, as it would typically be used with a ±15 V powered op amp. With this level of leakage, such diodes will only be useful with op amps with bias currents of several μA. For protection of appreciably lower bias current op amps (particularly most FET input devices) much lower leakage is necessary.

As the data of Figure 7-66 shows, not only does selecting a better diode help control leakage current, but operating it at a low bias voltage condition reduces leakage substantially. For example, while an ordinary 1N914 or 1N4148 diode may have 200 pA of leakage at 15 V, this is reduced to slightly more than a pA with bias controlled to 1 mV. But there is a caveat here. When used in a high impedance clamp circuit, glass diodes such as the 1N914/1N4148 families should either be shielded from incident light, or use opaque packages. This is necessary to minimize parasitic photocurrent from the surrounding light, which effectively appears as diode leakage current.

Specialty diodes with much lower leakage are also available, such as diode-connected FET devices characterized as protection diodes (see DPAD series of Reference 2). Within the data of Figure 7-66, the 2N5457 is a general purpose JFET, and the 2N4117/PN4117 family consists of parts designed for low current levels. Other low leakage and specialty diodes are described in References 3 and 4.

A Flexible Voltage Follower Protection Circuit

Of course, it isn't a simple matter to effectively apply protective clamping to op amp inputs, while reducing diode bias level to a sub-mV level.

The circuit of Figure 7-67 shows low leakage input clamping and other means used with a follower connected FET op amp, with protection at input and output, for both power on or off conditions.

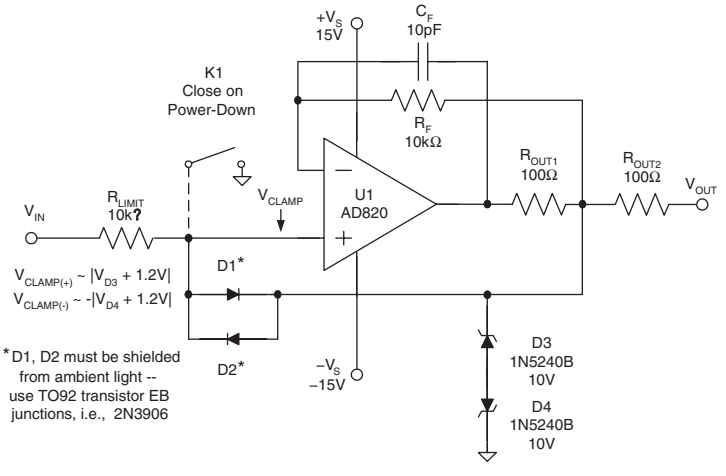


Figure 7-67: Bootstrapping the D1-D2 protection network reduces diode leakage to negligible levels, and is voltage-programmable for clamp level.

Disregarding the various diodes momentarily, this circuit is an output-current-limited voltage follower. With the addition of diodes D1-D2 and D3-D4, it has both a voltage-limited output, and an overvoltage protected input. Operating below the voltage threshold of output series-connected zener diodes D3-D4, the circuit behaves as a precision voltage follower. Under normal follower operation, that is at input/output voltages $< | V_Z + 0.6 |$ volts (where V_Z is the breakdown voltage of D3 or D4), diodes D1-D2 see only the combined offset and CM voltage errors of U1 as bias voltage. This reduces the D1-D2 leakage to very low levels, consistent with the pA level bias current of a FET input op amp. Note that D1-D2 *must* be prevented from photoconduction, and one direct means of this is to use opaque package diodes, such as the 2N3906 EB junctions discussed by Pease (see References 3 and 4). If 1N914s are used they must be light shielded. In either case, bootstrapping greatly reduces the effective D1-D2 leakage.

For input/output voltage levels greater than $V_Z + 0.6$ V, zener diodes D3-D4 break down. This action clamps both the V_{OUT} output node and the V_{CLAMP} node via D1-D2. The input of the op amp is clamped to either polarity of the two input levels of V_{CLAMP}, as indicated within the figure. Under clamp conditions, input voltage V_{IN} can rise to levels beyond the supply rails of U1 without harm, with excess current limited by R_{LIMIT}. If sustained high-level (~100 V) inputs will be applied, R_{LIMIT} should be rated as a 1–2W (or fusible) type.

This circuit has very good dc characteristics, due to the fact that the clamping network is bootstrapped. This produces very low input/output errors below the V_{CLAMP} threshold (consistent with the op amp specifications, of course). Note that this bootstrapping has ac benefits as well, as it reduces the D1-D2 capacitance seen by the source. While the ~100 pF capacitance of D3-D4 might cause a loading problem with some op amps, this is mitigated by the isolating effect of R_{OUT1}, plus the feedback compensation of C_F. Both R_{OUT1} and R_{OUT2} protect the op amp output.

The input voltage clamping level is also programmable, and is set by the choice of zener voltage V_Z. This voltage plus 1.2 V should be greater than the maximum input, but below the rail voltage, as summarized in the figure. The example uses 10 V ±5% zener diodes, so input clamping typically will occur at ±11.2 V, allowing ±10 V swings.

An important caveat to the above is that it applies for *power-on* conditions. With *power-off*, D1–D4 still clamp to the noted levels, but this now produces a condition whereby the U1 input and output voltage can exceed the rails.

Note that this could be dangerous, for a given U1 device. If so, an optional and simple means towards providing a lower, safe clamping level for power off conditions is to use a relay at the V_{CLAMP} node. The contacts are open with power applied, and closed with power absent. With attention paid to an overall PCB layout, this can preserve a pA level bias current of FET op amps used for U1.

CM Over-Voltage Protection Using CMOS Channel Protectors

A much simpler alternative for overvoltage protection is the CMOS *channel protector*. A channel protector is a device in series with the signal path; for example, preceding an op amp input. It provides overvoltage protection by dynamically altering its resistance under fault conditions. Functionally, it has the distinct advantage of affording protection for sensitive components from voltage transients, whether the power supplies are present or not. Representative devices are the ADG465/ADG466/ADG467, which are channel protectors with single, triple, and octal channel options. Because this form of protection works whether supplies are present or not, the devices are ideal for use in applications where input overvoltages are common, or where correct power sequencing can't always be guaranteed. One such example is within hot-insertion rack systems.

An application of a channel protector for overvoltage protection of a precision buffer circuit is shown in Figure 7-68. A single channel device, the ADG465 at U2, is used here at the input of the U1 precision op amp buffer, an OP777.

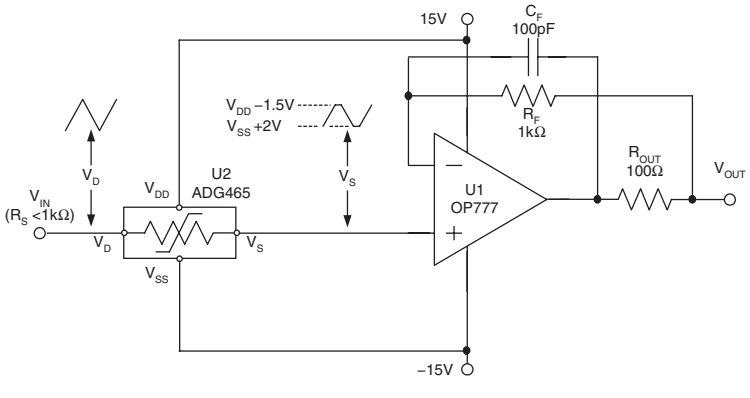


Figure 7-68: Using an ADG465 channel protector IC with a precision buffer offers great simplicity of protection and fail-safe operation during power off.

In operation, a channel protector behaves just like a series resistor of 60 Ω to 80 Ω in normal operation (i.e., nonfault conditions). Consisting of a series connection of multiple P and N MOSFETs, the protector dynamically adjusts channel resistance according to the voltage seen at the V_D terminal. Normal conduction occurs with V_D more than a threshold level above or below the rails, i.e., $(V_{SS} + 2\ V) < V_D < (V_{DD} - 1.5\ V)$. For fault conditions the analog input voltage exceeds this range, causing one of the series MOSFETs to switch off, thus raising the channel resistance to a high level. This clamps the V_S output at one extreme range, either $V_{SS} + 2$ V or $V_{DD} - 1.5$ V, as shown in Figure 7-68.

A major channel protector advantage is the fact that both circuit and signal source protection are provided, in the event of overvoltage or power loss. Although shown here operating from op amp ±15 V supplies, these channel protectors can handle total supplies of up to 40 V. They also can withstand overvoltage inputs from $V_{SS} - 20$ V to $V_{DD} + 20$ V with power on (or ±35 V in the circuit shown). With power off ($V_{DD} = V_{SS} = 0$ V), maximum input voltage is ±35 V. Maximum room temperature channel leakage is 1 nA, making them suitable for op amps and in-amps with bias currents of several nA and up.

Related to the ADG46x series of channel protectors are several *fault-protected multiplexers*, for example the ADG508F/ADG509F, and the ADG438F/ADG439F families. Both the channel protectors and the fault-protected multiplexers are low power devices, and even under fault conditions, their supply current is limited to sub microampere levels. A further advantage of the fault-protected multiplexer devices is that they retain proper channel isolation, even for input conditions of one channel seeing an overvoltage; that is, the remaining channels still function.

CM Overvoltage Protection Using High CM Voltage In Amp

The ultimate simplicity for analog channel overvoltage protection is achieved with resistive input attenuation ahead of a precision op amp. This combination equates to a high voltage capable in amp, such as the AD629, which is able to linearly process differential signals riding upon CM voltages of up to ±270 V. Further, and most important to overvoltage protection considerations, the on-chip resistors afford protection for either common mode or differential voltages of up to ±500 V. All of this is achieved by virtue of a precision laser-trimmed thin-film resistor array and op amp, as shown in Figure 7-69.

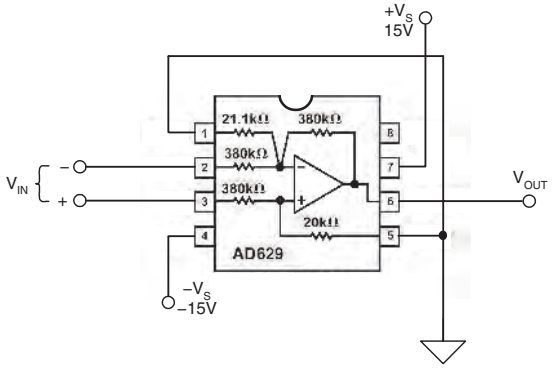


Figure 7-69: The AD629 high voltage in amp IC offers ± 500 V input overvoltage protection, one-component simplicity, and fail-safe power-off operation

Examination of this topology shows that the resistive network around the AD629's precision op amp acts to divide down the applied CM voltage at V_{IN} by a factor of 20/1. The AD629 simultaneously processes the input differential mode signal V_{IN} to a single-ended output referred to a local ground, at a gain factor of unity. Gain errors are no more than ±0.03% or 0.05%, while offset voltage is no more than 0.5 mV or 1 mV (grade dependent). The AD629 operates over a supply range of ±2.5 V to ±18 V.

These factors combine to make the AD629 a simple, one-component choice for the protection of off-card analog inputs that can potentially see dangerous transient voltages. Due to the relatively high resistor values used, protection of the device is also inherent with no power applied, since the input resistors safely limit fault currents. In addition, it offers those operating advantages inherent to an in amp: high CMR (86 dB minimum at 500 Hz), excellent overall dc precision, and the flexibility of simple polarity changes. On the flip side of performance issues, several factors make the AD629's output noise and drift relatively high, if compared to a lower gain in amp configuration such as the AMP03. These are the Johnson noise of the high value resistors, and the high noise gain of the topology (21×). These factors raise the op amp noise and drift along with the resistor noise by a factor higher than typical. Of course, whether or not this is an issue relevant to an individual application will require evaluation on a case-by-case basis.

Inverting Mode Op Amp Protection Schemes

There are some special cases of overvoltage protection requirements that don't fit into the more general CM protection schemes above. Figure 7-70 is one such example, a low bias current FET input op amp I/V converter.

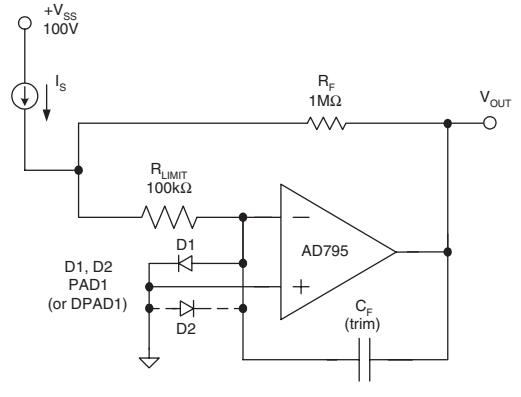


Figure 7-70: A low bias current FET input op amp I/V converter with overvoltage protection network RLIMIT and D1

In this circuit the AD795 1 pA bias current op amp is used as a precision inverter. Some current-source nature signals can originate from a high voltage potential, such as the 100 V V_{SS} level shown. As such, they have the potential of developing fault voltage levels beyond the op amp rails, producing fault current into the op amp well above safe levels. To prevent this, protection resistor R_{LIMIT} is used inside the feedback loop as shown, along with voltage clamp D1 (D2).

For normal signal condition (i.e., $I_S \leq 10$ uA) the op amp's inverting node is very close to ground, with just a tiny voltage drop across R_{LIMIT}. Normal I/V conversion takes place, with gain set by R_F. For protection, D1 is a special low leakage diode, clamping any excess voltage at the (–) node to ~0.6 V, thus protecting the op amp. The value of R_{LIMIT} is chosen to allow a 1 mA max current under fault conditions. Bootstrapping the

D1 (and/or D2) clamp diodes as shown minimizes the normal operating voltage across the inverting node, keeping the diode leakage low (see Figure 7-66). Note that for a positive source voltage as shown, only positive clamping is needed, so just one diode suffices.

Only the lowest leakage diodes (≤1 pA) such as the PAD1 (or the DPAD1 dual) should be used in this circuit. As previously noted, any clamping diode used here should either be shielded from light (or use opaque packaging), to minimize photocurrent from ambient light. Even so, the diode(s) will increase the net input current and shunt capacitance, and feedback compensation C_F will likely be necessary to control response peaking. C_F should be a very low leakage type. Also, with the use of very low input bias current devices such as the AD795, it isn't possible to use the same level of internal protection circuitry as with other ADI op amps. This factor makes the AD795 more sensitive to handling, so ESD precautions should be taken.

Amplifier Output Voltage Phase-Reversal

As alluded to above, there are "gray-area" op amp groups that have anomalous CM voltage zones, falling between the supply rails. As such, protection for these devices cannot be guaranteed by simply ensuring that the inputs stay between the rails—they must additionally stay *entirely* within their rated CM range, for consistent behavior.

Peculiar to some op amps, this misbehavior phenomenon is called *output voltage phase-reversal.* It is seen when one or both of the op amp inputs exceed their allowable input CM voltage range. Note that the inputs may still be well within the extremes of rail voltage, but simply below one specified CM limit. Typically, this is towards the negative range. Phase-reversal is most often associated with JFET and/or BiFET amplifiers, but some bipolar single-supply amplifiers are also susceptible to it.

The Figure 7-71 waveforms illustrate this general phenomenon, with an overdriven voltage follower input on the left, and the resulting output phase-reversal at the right.

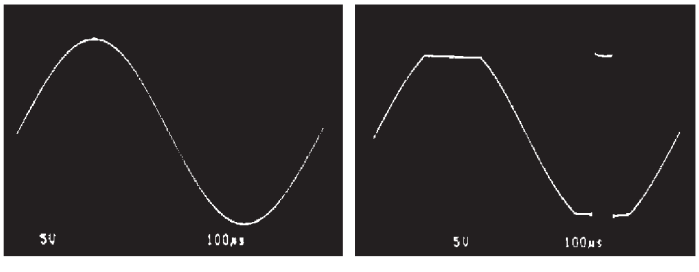


Figure 7-71: An illustration of input overdriving waveform (left) and the resulting output phase-reversal (right), using a JFET input op amp

While the specific details of the internal mechanism may vary with individual op amps, it suffices to say that the output phase-reversal occurs when a critical section of the amplifier front end saturates, causing the input-output sign relationship to temporarily reverse. Under this condition, when the CM range is exceeded, the negative-going input waveform in Figure 7-71 (left) does not continue going more negative in the output waveform, Figure 7-71 (right). Instead, the input-output relationship *phase-reverses*, with the output suddenly going positive, i.e., the spike. It is important to note that this is *not* a latching form of phase-reversal, as the output will once again continue to properly track the input, when the input returns to the CM range. In Figure 7-71, this can be seen in the continuance of the output sine wave, after the positive-going phase-reversal spike settles.

In most applications, this output voltage phase-reversal does no harm to the op amp, nor to the circuit where it is used. Indeed, since it is triggered when the CM limit is exceeded, noninverting stages with appreciable signal gain never see it, since their applied CM voltage is too small.

Note that with inverting applications the output phase-reversal problem is nonexistent, as the CM range isn't exercised. So, although a number of (mostly older) op amps suffer from phase-reversal, it still is rarely a serious problem in system design.

Nevertheless, when and if a phase-reversal susceptible amplifier used in a servo loop application sees excess CM voltage, the effect can be disastrous—it goes **Bang!** So, the best advice is to be forewarned.

An Output Phase-Reversal Do-it-Yourself Test

Since output phase-reversal may not always be fully described on a data sheet, it is quite useful to test for it. This is easily done in the lab, by driving a questionable op amp as a unity-gain follower, from a source impedance (R_{LIMIT}) of ~1kΩ. It is helpful to make this a variable, 1 kΩ –100 kΩ range resistance.

With a low resistance setting (1 kΩ), while bringing the driving signal level slowly up towards the rail limits, observe the amplifier output. If a phase-reversal mechanism is present when the CM limit of the op amp is exceeded, the output will suddenly reverse (see Figure 7-71, right). If there is no phase-reversal present in an amplifier, the output waveform will simply clip at the limits of its swing. It may prove helpful to have a well-behaved op amp available for this test, to serve as a performance reference. One such device is the AD8610.

Note that, in general, some care should be used with this test. Without a series current-limit resistor, if the generator impedance is too low (or level too high), it could possibly damage an internal junction of the op amp under test. So, obviously, caution is best for such cases.

Once a suitable R_{LIMIT} resistance value is found, well-behaved op amps will simply show a smooth, bipolar range, clipped output waveform when overdriven. This clipping will appear more like the *upper (positive swing)* portion of the waveform within Figure 7-71, right.

Fixes For Output Phase–Reversal

An op amp manufacturer might not always give the R_{LIMIT} resistance value appropriate to prevent output phase-reversal. But, the value can be determined empirically with the driving method mentioned above. Most often, the R_{LIMIT} resistor value providing protection against phase-reversal will also safely limit fault current through any input CM clamping diodes. If in doubt, a nominal value of 1 kΩ is a good starting point for testing.

Typically, FET input op amps will need only the current limiting series resistor for protection, but bipolar input devices are best protected with this same limiting resistor, *along with a Schottky diode* (i.e., R_{LIMIT} and D2, of Figure 7-65).

For a more detailed description of the output voltage phase-reversal effect, see References 7 and 8. Figure 7-72 summarizes a number of the key points relating to output voltage phase-reversal.

- Nonlatching Inversion of Transfer Function, Triggered by Exceeding Common-Mode Limit
- Sometimes Occurs in FET and Bipolar (Single-Supply) Op Amps
- Doesn't Harm Amplifier… but *Disastrous* for Servo Systems
- Not Usually Specified on Data Sheet, so Amplifier Must be Checked
- Easily Prevented:
  - All op amps: Limit applied CM voltage by clamping or other means
  - BiFETs: Add series input resistance, R_{LIMIT}
  - Bipolars: R_{LIMIT} and Schottky clamp diode to rail

Figure 7-72: A summary of key points regarding output phase-reversal in FET and bipolar input op amps

Alternately, any of the several previously mentioned CM clamping schemes can be used to prevent output phase-reversal, by setting the clamp voltage to be less than the amplifier CM range limit where phase-reversal occurs. For example, Figure 7-67 would operate to prevent phase-reversal in FET amplifiers susceptible to it, if the negative clamp limit is set so that $V_{CLAMP(-)}$ never exceeds the typical negative CM range of –11 V on a –15 V rail.

For validation of this or any of the previous overvoltage protection schemes, the circuit should be verified on a number of op amps, over a range of conditions as suitable to the final application environment.

Input Differential Protection

The discussions thus far have been on overvoltage common-mode conditions, which is typically associated with forward biasing of PN junctions inherent in the structure of the input stage. There is another equally important aspect of protection against overvoltage, which is that due to excess *differential* voltages. Excessive differential voltage, when applied to certain op amps, can lead to degradation of their operating characteristics.

This degradation is brought about by *reverse junction breakdown,* a second case of undesirable input stage conduction, occurring under conditions of *differential* over-voltage. However, in the case of reverse breakdown of a PN junction, the problem can be more subtle in nature. It is illustrated by the partial op amp input stage in Figure 7-73.

This circuit, applicable to a low noise op amp such as the OP27, is also typical of many others using low noise bipolar transistors for differential pair Q1-Q2. In the absence of any protection, it can be shown that voltages above about 7 V between the two inputs will cause a reverse junction breakdown of either Q2 or Q1 (dependent upon relative polarity). Note that in cases of E-B breakdown, even small reverse currents can cause degradation in both transistor gain and noise (see Reference 6). After E-B breakdown occurs, op amp parameters such as the bias currents and noise may well be out of specification. This is usually permanent, and it can occur gradually and quite subtly, particularly if triggered by transients. For these reasons,

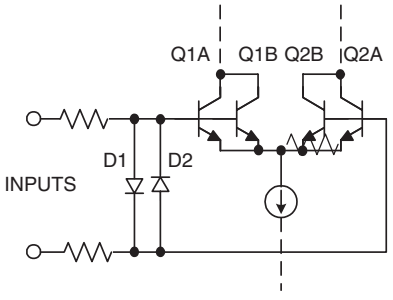


Figure 7-73: An op amp input stage with D1-D2 input differential overvoltage protection network

virtually all low noise op amps, whether NPN or PNP based, utilize protection diodes such as D1-D2 across the inputs. These diodes conduct for applied voltages greater than ±0.6 V, protecting the transistors.

The dotted series resistors function as current limiters (protection for the protection diodes) but aren't used in all cases. For example, the AD797 doesn't have the resistors, simply because they would degrade the part's specified noise of $1\ \text{nV}/\sqrt{\text{Hz}}$. Note: when the resistors are absent internally, some means of external current limiting must be provided, when and if differential overvoltage conditions do occur. Obviously, this is a trade-off situation, so the confidence of full protection must be weighed against the noise degradation. Note that an application circuit itself may provide sufficient resistance in the op amp inputs, such that additional resistance isn't needed.

In applying a low noise bipolar input stage op amp, first check the chosen part's data sheet for internal protection. When necessary, protection diodes D1-D2, if not internal to the op amp, should be added to guarantee prevention of Q1-Q2 E-B breakdown. If differential transients of more than 5 V can be seen by the op amp in the application, the diodes are in order. Ordinary low capacitance diodes will suffice, such as the 1N4148 family. Add current limiting resistors as necessary, to limit diode current to safe levels.

Other IC device junctions, such as base-collector and JFET gate-source junctions don't exhibit the same degradation in performance upon breakdown, and for these the input current should be limited to 5mA, unless the data sheet specifies a different value.

Protecting In Amps Against Overvoltage

From a protection standpoint, instrumentation amplifiers (in amps) are similar in many ways to op amps. Like op amps, their absolute maximum ratings must be observed for both common and differential mode input voltages.

A much simplified schematic of the AD620 in amp is shown in Figure 7-74, showing the input differential transistors and their associated protection parts.

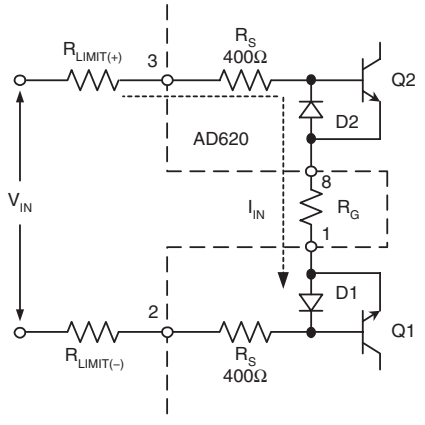


Figure 7-74: The AD620 in amp input internally uses D1-D2 and series resistors R_S for protection (additional protection can be added externally)

An important point, unique to the AD620 device, is the fact that the 400 Ω internal R_S protection resistors are *thin-film types*. Therefore these resistors don't show symptoms of diode-like conduction to the IC substrate (as would be the case were they diffused resistors). Practically, this means that the input ends of these resistors (Pins 3 and 2) can go above or below the supplies. Differential fault currents will be limited by the combination of twice the internal R_S plus the external gain resistance, R_G. Excess applied CM voltages will show current limited by R_S.

In more detail, it can be noted that input transistors Q1 and Q2 have protection diodes D1 and D2 across their base-emitter junctions, to prevent reverse breakdown. For differential voltages, analysis of shows that a fault current, I_{IN}, flows through the external R_{LIMIT} resistors (if present), the internal R_S resistors, the gain-setting resistor R_G, and two diode drops (Q2, D1). For the AD620 topology, R_G varies inversely with gain, and a worst-case (lowest resistance) occurs with the maximum gain of 1000, when R_G is 49.9 Ω. Therefore the lowest total internal path series resistance is about 850 Ω.

For the AD620, any combination of CM and differential input voltages should be limited to levels that limit the input fault current to 20 mA, maximum. A purely differential voltage of 17 V would result in this current level, for the lowest resistance case. For CM voltages that may go beyond either rail, an internal diode not shown in Figure 7-74 conducts, effectively clamping the driven input to either $+V_S$ or $-V_S$ at the R_S inner end. For this overvoltage CM condition, the 400 Ω value of R_S and the excess voltage beyond the rail determines the current level. If, for example, V_{IN} is 23 V with $+V_S$ at 15 V, 8 V appears across R_S, and the 20 mA current rating is reached. Higher fault voltages can be dealt with by adding R_{LIMIT} resistance, to maintain fault current at 20 mA or less.

A more generalized external voltage protection circuit for an in amp like the AD620 is shown in Figure 7-75.

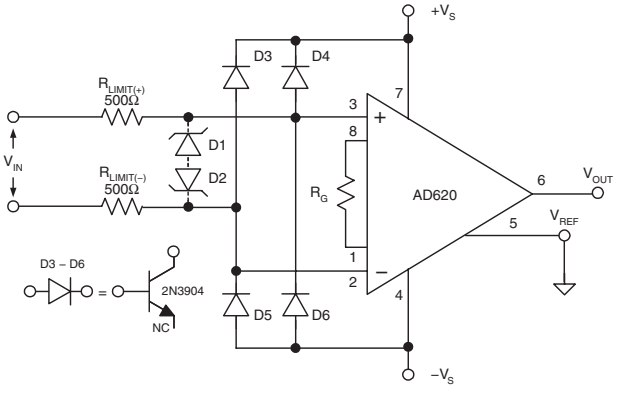


Figure 7-75: A generalized diode protection circuit for the AD620 and other in amps uses D3–D6 for CM clamping and series resistors R_{LIMIT} for protection

In this circuit, low-leakage diodes D3–D6 are used as CM clamps. Since the in amp bias current may be only 1 nA or so (for the AD620), a low leakage diode type is mandatory. As can be noted from the topology, diode bootstrapping isn't possible with this configuration.

It should be noted that not only must the diodes have basically low leakage, they must also maintain low leakage at the highest expected temperature. This suggests either FET type diodes (see Figure 7-66), or the transistor C-B types shown. The R_{LIMIT} resistors are chosen to limit the maximum diode current under fault conditions. If additional *differential* protection is used, either back-back zener or Transzorb clamps can be used, shown as D1-D2. If this is done, leakage of these diodes should be carefully considered.

The protection scheme of Figure 7-75, while effective using appropriate parts, has the downside of being busy for components. A much more simple in amp protection using fault protected devices is shown in Figure 7-76. Although shown with an AD620, this circuit is useful with many other dual-supply in amps with bias currents of 1 nA or more. It uses two-thirds of a triple ADG466 channel-protector for the in amp differential inputs.

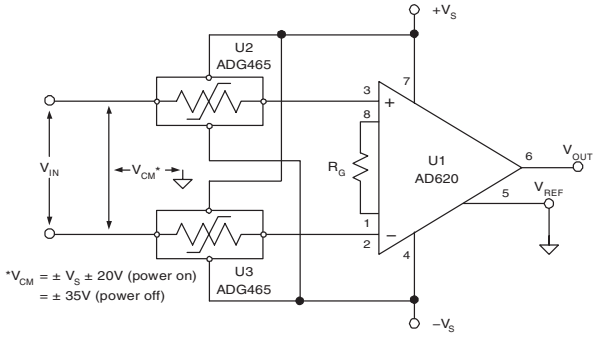


Figure 7-76: A channel protector device (or fault-protected multiplexer) provides protection for dual-supply in amps with a minimum of extra parts

Because the nature of a channel protection device is to turn off as V_{IN} approaches either rail, the scheme of Figure 7-76 doesn't function with rail sensing single-supply in amps. If near-rail operation and protection is required in an in amp application, an alternative method is necessary. Many single-supply in-amps are topologically similar to the two-amplifier in amp circuit which is shown within the dotted box of Figure 7-77.

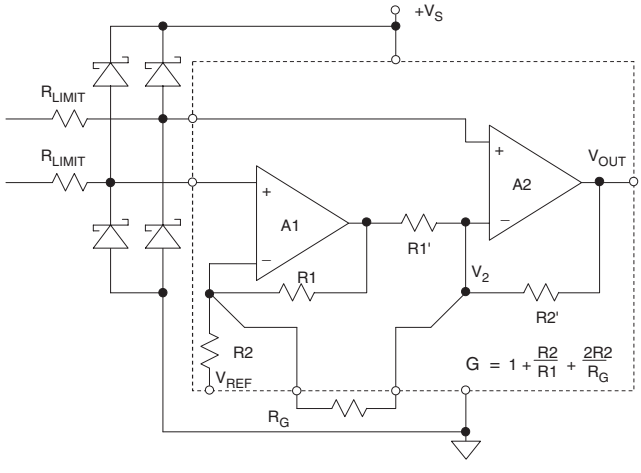


Figure 7-77: Single-supply in amps may or may not require external protection in the form of resistors and clamp diodes—if so, they can be added as shown

In terms of the necessity for externally added protection components, a given in amp may or may not require them. Each case needs to be considered individually. For example, some in amps have clamp diodes as shown, but *internal to the device*. The AD623 is such a part, but it lacks the series resistors, which can be added externally when and if necessary. Note that this approach allows the R_{LIMIT} value to be optimized for protection, with negligible impact on noise for those applications not needing the protection.

Also, some in amp devices have both internal protection resistors *and* clamping diodes, an example here is the AD627. In this device, the internal protection is adequate for transients up to 40 V beyond the supplies (a 20 mA fault current in the internal resistors). For overvoltage levels higher than this, external R_{LIMIT} resistors can be added.

The use of the Schottky diodes as shown at the two inputs is an option for in amp protection. If no clamping is specifically provided internally, then they are applicable. Their use is generally similar to the op amp protection case of Figure 7-65, with comparable caveats as far as leakage. Note that in many cases, due to internal protection networks of modern in amps, these diodes just won't be necessary. But again, there aren't hard rules on this, so always check the data sheet before finalizing an application.

To summarize, Figure 7-78 reviews the major points of the in-circuit overvoltage issues discussed in this section.

If these varied overvoltage precautions for op amps and in amps seem complex, they are. Whenever op amp (or in amp) inputs (and outputs) go outside equipment boundaries, dangerous or destructive things can happen to them. Obviously, for highest reliability these potentially hazardous situations should be anticipated.

Fortunately, most applications are contained entirely within the equipment, and usually see inputs and outputs to/from other ICs on the same power system. Therefore clamping and protection schemes typically aren't necessary for these cases.

- INPUT VOLTAGES MUST NOT EXCEED ABSOLUTE MAXIMUM RATINGS
  (Usually Specified with Respect to Supply Voltages)
- Requires $V_{IN(CM)}$ Stay Within a Range Extending to ≤0.3V Beyond Rails
  ($-V_S-0.3V \geq V_{IN} \leq +V_S+0.3V$)
- IC Input Stage Fault Currents *Must* Be Limited
  (≤ 5mA Unless Otherwise Specified)
- Avoid Reverse-Bias Breakdown in Input Stage Junctions!
- Differential and Common-Mode Ratings Often Differ
- No Two Amplifiers are Exactly the Same
- Watch Out for Output Phase-Reversal in JFET and SS Bipolar Op Amps
- Some ICs Contain *Internal* Input Protection
  - Diode Voltage Clamps, Current Limiting Resistors (or both)
  - Absolute Maximum Ratings Must Still Be Observed

Figure 7-78: A summary of in-circuit overvoltage points

Out-of-Circuit Overvoltage Protection

Linear ICs such as op amps and in amps must also be protected prior to the time they are mounted to a printed circuit board, that is an *out-of-circuit* state. In such a condition, ICs are completely at the mercy of their environment as to what stressful voltage surges they may see. Most often the harmful voltage surges come from *electrostatic discharge,* or, as more commonly referenced, ESD. This is a single, fast, high current transfer of electrostatic charge resulting from one of two conditions. These conditions are:

1) *Direct contact transfer between two objects at different potentials (sometimes called contact discharge)*
2) *A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)*

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, and so forth. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Some common examples of ordinary acts producing significant ESD voltages are shown in Figure 7-79.

- Walking across a Carpet
  1000V – 1500V
- Walking across a Vinyl Floor
  150V – 250V
- Handling Material Protected by Clear Plastic Covers
  400V – 600V
- Handling Polyethylene Bags
  1000V – 2000V
- Pouring Polyurethane Foam into a Box
  1200V – 1500V
- Note: Above Assumes 60% RH. For Low RH (30%) Voltages Can Be > 10 Times

Figure 7-79: ESD voltages generated by various ordinary circumstances

ICs can be damaged by the high voltages and high peak currents generated by ESD. Precision analog circuits, often featuring very low bias currents, are more susceptible to damage than common digital circuits, because traditional input-protection structures that protect against ESD damage increase input leakage—and thus can't be used.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered. Figure 7-80 outlines some relevant points on ESD induced failures.

- ESD Failure Mechanisms:
  - Dielectric or junction damage
  - Surface charge accumulation
  - Conductor fusing
- ESD Damage Can Cause:
  - Increased leakage
  - Degradation in performance
  - Functional failures of ICs
- ESD Damage is often Cumulative:
  - For example, each ESD "zap" may increase junction damage until, finally, the device fails.

Figure 7-80: Understanding ESD damage

All ESD-sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic shipping tubes, and the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as in Figure 7-81, which outlines the appropriate handling procedures.

The presence of outside package notices such as those shown in Figure 7-81 is notice to the user that device handling procedures appropriate for ESD protection are necessary.

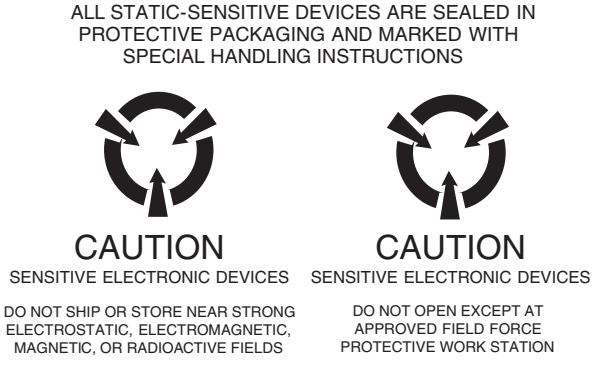
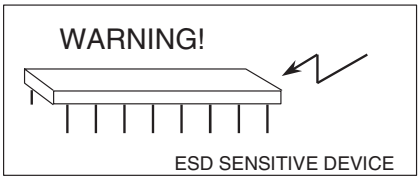


Figure 7-81: Recognizing ESD-sensitive devices by package and labeling

In addition, data sheets for ESD-sensitive ICs generally have a bold statement to that effect, as shown in Figure 7-82.

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packages as long as possible is a first step. A second step is discharging potentially damaging ESD sources before IC damage occurs. Discharging such voltages can be done quickly and safely, through a high impedance.



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADxxx features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 7-82: ESD data sheet statement for linear ICs

A key component required for ESD-safe IC handling is a workbench with a static-dissipative surface, shown in the workstation of Figure 7-83. The surface is connected to ground through a 1 MΩ resistor, which dissipates any static charge, while protecting the user from electrical ground fault shock hazards. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with the discharge resistor.

Note that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the high impedance surface of Figure 7-83, however, the peak current isn't high enough to damage the device.

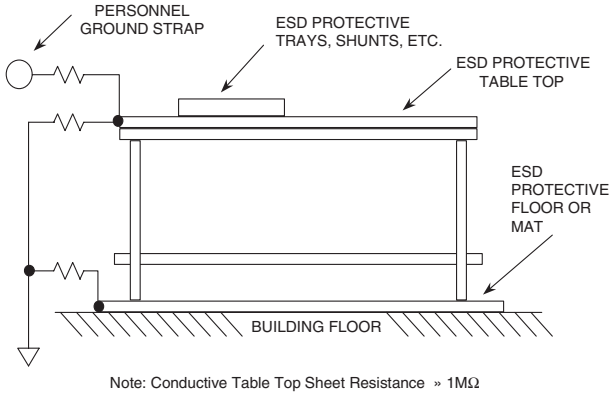


Figure 7-83: A workstation environment suitable for handling ESD-sensitive ICs

Several personnel-handling techniques are keys to minimizing ESD-related damage. At the workstation, a conductive wrist strap is recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape from packages, won't cause IC damage. Again, a 1 MΩ resistor, from the wrist strap to ground, is required for safety. When building prototype breadboards or assembling PC boards that contain ESD-sensitive ICs, all passive components should be inserted and soldered before the ICs. This minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building ESD protection into ICs. The users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures, so that protection can be built in at all key points along the way, as outlined in Figure 7-84.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

ANALOG DEVICES:

- Circuit Design and Fabrication

↓ Design and manufacture products with the highest level of ESD
↓ protection consistent with required analog and digital performance.

- Pack and Ship

↓ Pack in static dissipative material. Mark packages with ESD warning.

CUSTOMERS:

- Incoming Inspection

↓ Inspect at grounded workstation. Minimize handling.

- Inventory Control

↓ Store in original ESD-safe packaging. Minimize handling.

- Manufacturing

↓ Deliver to work area in original ESD-safe packaging. Open packages only at
↓ grounded workstation. Package subassemblies in static dissipative packaging.

- Pack and Ship

Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 7-84: ESD protection requires a partner relationship between ADI and the end customer with control at key points

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher sensitivity to ESD than others. ICs located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits that must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 interface port ICs on a computer, which can easily be exposed to excess voltages. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. Note that this does not apply to individual ICs, *but to the end equipment.* These standards are defined along with test methods in the various IEC1000 specifications, and are listed in Figure 7-85.

- IEC1000-4 Electromagnetic Compatibility EMC
- IEC1000-4-1 Overview of Immunity Tests
- IEC1000-4-2 Electrostatic Discharge Immunity (ESD)
- IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity
- IEC1000-4-4 Electrical Fast Transients (EFT)
- IEC1000-4-5 Lightening Surges
- IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz
- Compliance Marking: CE

Figure 7-85: A listing of the IEC standards applicable to ESD specifications and testing procedures

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*.

Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers).

Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test, noted as follows:

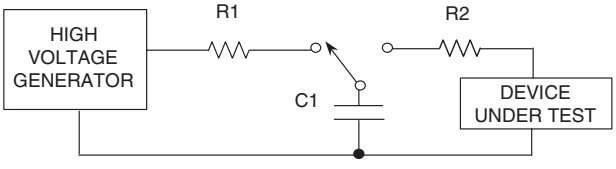
1) *The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.*

2) The current rise time is significantly faster in the IEC test.

3) The IEC test is carried out while power is applied to the device.

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 7-86.

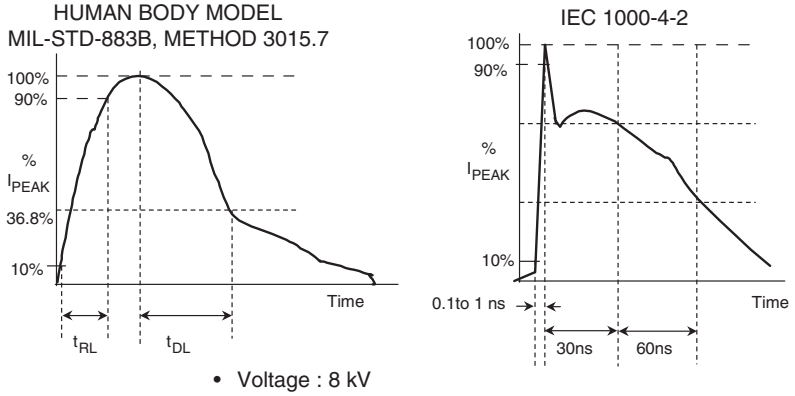


ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARG E VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 7-86: ESD test circuits and values

The ESD waveforms for the MIL-STD-883B, METHOD 3015.7 and IEC 1000-4-2 tests are compared in Figure 7-87, left and right, respectively.



- Voltage : 8 kV
- Peak Current :
  - MIL-883B, Method 3015.7 HBM: 5 A
  - IEC 1000-4-2: 25 A

Figure 7-87: ESD test waveforms

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the overvoltage protection methods already discussed in this section will help.

Additional protection can also be obtained. For RS-232 and RS-485 drivers and receivers, the ADMxxx-E series is supplied with guaranteed 15 kV (HBM) ESD specifications.

For more general uses, the addition of TransZorbs at appropriate places in a system can provide protection against ESD (see References).

Figure 7-88 summarizes the major points about ESD prevention, from both an out-of-circuit as well as an in-circuit perspective.

- Observe all Absolute Maximum Ratings on Data Sheet
- Read ADI AN-397 (See Reference 16)
- Purchase ESD-Specified Digital Interface Devices
  - ADMxxx-E Series of RS-232/RS-485 Drivers/Receivers (See Reference 18)
- Follow General Overvoltage Protection Recommendations
  - Add Series Resistance to Limit Currents
  - Add Zeners or Transient Voltage Suppressors (TVS) for Extra Protection (See Reference 19)

Figure 7-88: A summary of ESD points

References: Op Amp Protection

1. Walt Kester, Wes Freeman, Joe Buxton, "Overvoltage Protection," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.
2. Siliconix PAD/JPAD/SSTPAD series Low leakage Pico-Amp Diodes, Vishay/Siliconix, www.vishay.com/brands/siliconix/SSFsglld.html.
3. Bob Pease, "Bounding, Clamping Techniques Improve Circuit Performance," **EDN**, November 10, 1983, p. 277.
4. Bob Pease, "Understanding Diodes and Their Problems," Chapter 6 within **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991, ISBN 0-7506-9184-0.
5. Dov Kurz, Avner Cohen, "Bootstrapping Reduces Amplifier Input Capacitance," **EDN**, March 20, 1978.
6. C.D. Motchenbacher, J.A. Connelly, Chapter 5, within **Low Noise Electronic System Design**, John Wiley, 1993.
7. Adolfo Garcia**,** "Operational Amplifier Output Voltage Phase Reversal**,**" Section 11, pp. 1–10 within Walt Kester, Editor, **1992 Amplifier Applications Guide**, Analog Devices, Inc., Norwood, MA, 1992, ISBN 0-916550-10-9.
8. Adolfo Garcia**,** Wes Freeman*,* "Overvoltage Effects On Analog Integrated Circuits," Section 7 within Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, Inc., Norwood, MA, 1995, ISBN 0-916550-16-8.
9. Charles Kitchen, Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, Inc., 2000.
10. Walt Kester, Wes Freeman, James Bryant, "Electrostatic Discharge," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.
11. MIL-STD-883 Method 3015, "Electrostatic Discharge Sensitivity Classification." Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA, 19111-5094.
12. EIAJ ED-4701 Test Method C-111, "Electrostatic Discharges." Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.
13. ESD Association Standard S5.2 for "Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)-Component Level." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
14. ESD Association Draft Standard DS5.3 for "Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) Component Testing." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
15. **ESD Prevention Manual**, Analog Devices, Inc.
16. Niall Lyne, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," **Analog Devices AN397**.
17. Mike Byrne, "How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging," **Analog Devices AN311**.
18. Data sheet for **ADM3311E RS-232 Port Transceiver**, Analog Devices, Inc., www.analog.com.
19. TransZorbs are available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, 631-847-3000, www.vishay.com.