7. I need high input impedance! Input impedance vs. input bias current

In helping to select operational amplifiers (op amps) and instrumentation amplifiers, I frequently hear, "I need really high input impedance." Oh, really? Are you sure?

It is rare that input impedance (or more specifically input resistance) is an important issue. (Input capacitance, the reactive part of input impedance, is another matter). What is most often needed is low input bias current, I_B. Yes, they are related, but different. Let us sort it out.

A simple model of a single input is a parallel combination of a current source (the input bias current) and an input resistor (**Figure 15**). The resistor causes the input current to vary with input voltage. The input bias current is the input current at a specific input voltage, usually at midsupply.

The input resistance is a measure of the change in input current with a change in input voltage. It is possible to have an ampere of input bias current and still have extremely high input resistance.

TI often provides a typical graph showing input bias current vs. common-mode voltage. A couple of examples are shown in **Figure 16**; you can see that it's not a perfectly straight line. Note that the OPA211 is a bipolar junction transistor (BJT)-input op amp with input bias current cancellation that greatly reduces input bias current – but it is still pretty high. The OPA211's input bias current and high noise current make it an unlikely choice with a source resistance greater than 10 kΩ, so its input resistance of 1.3 GΩ is seldom an issue.

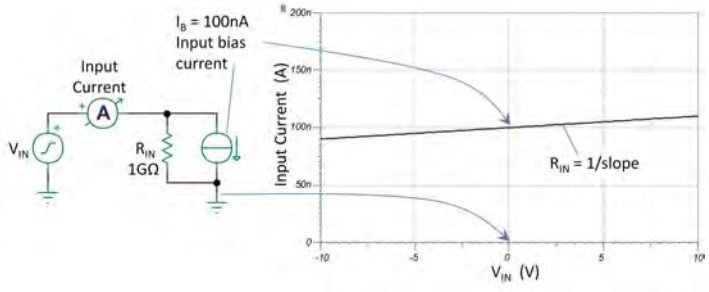

Figure 15: Model of one input terminal is a current source and an input resistor in parallel.

The OPA320 complementary metal-oxide semiconductor (CMOS) op amp has a tiny input bias current, primarily coming from the leakage of its input electrostatic discharge (ESD) protection circuitry. These leakage currents reach a maximum near the rail voltages. CMOS and junction .(JFET)-input amplifiers are generally the best choices when you require a very low input bias current. Yes, the input resistance is high, but it is not generally an important factor in amplifier selection.

There are several ways that input bias current can be detrimental in precision-analog circuitry. Flowing through a source resistance or feedback network resistance, it can contribute $I_B R_S$ to the offset voltage. Flowing in certain sensors and chemical cells such as pH probes, it can polarize the electrodes, creating errors and even causing permanent damage. Input bias current will charge the capacitor of an integrator circuit, creating a ramping output with zero input.

Depending on the sensitivity of your circuit to input bias current, it can be a deciding factor in amplifier selection. Check out typical performance graphs showing variations of I_B with input voltage, with an eye to the particular voltage range of interest. Overtemperature behavior may be particularly important with CMOS and JFET amplifiers, as their I_B generally rises dramatically with increasing temperature.

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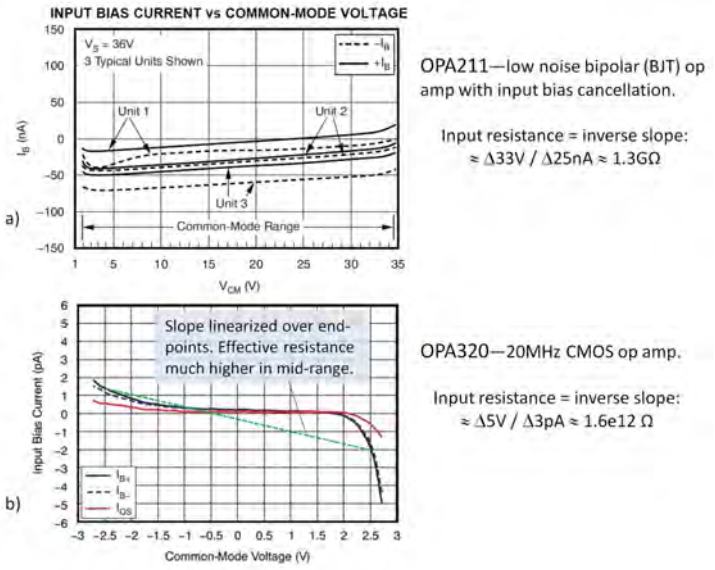

Figure 16: Input bias current vs. common-mode voltage.

8. Input bias current of CMOS and JFET amplifiers

Complementary metal-oxide semiconductor (CMOS) and junction FET (JFET)-input operational amplifiers (op amps) are often selected for their low input bias current (I_B). But there is more to the story than a single line in a specifications table – subtleties that you should be aware of.

The gate of a CMOS transistor (the working input of a CMOS op amp) has extremely low input current. But these fragile gates must be protected from electrostatic discharge (ESD) and electrical overstress (EOS) with additional circuitry that is the primary source of their input bias current. This protection generally includes internal clamp diodes to the supply rails. The OPA320 is an example, shown in **Figure 17a**. These diodes have a small leakage current in the few picoampere range. At an input voltage near midsupply rails, their leakages are pretty well-matched, leaving only a small residual difference current of less than 1 pA that appears as amplifier input bias current.

The relationship of the two diode leakages changes as the input voltage nears the supply rails. Near the bottom rail, for example, D2's reverse voltage nears zero and its leakage drops. D1's leakage will dominate, causing a higher input bias current flowing out of the input terminal. Of course, the opposite occurs as the input approaches the positive supply rail. The input bias current is specified and tested at the midpoint, where leakage is nearly matched and quite low.

The result is an input bias current versus an input voltage that varies, as shown in **Figure 17b**. For any given unit, there is an input voltage where the input bias current is zero (assuming no significant package or circuit layout leakage). In fact, with a rail-to-rail op amp you can often self-bias the input (**Figure 18**); the output will drift to a voltage equal to the zero input-bias-current point. It is an interesting experiment but not a particularly useful circuit.

The story can be different with JFET-input amplifiers such as the OPA140 (**Figure 19**). Here, the gate of the input transistor is a diode junction and its leakage current is often the dominant source of input bias current. The input gate junction is generally larger and therefore leakier than the protection diodes. Thus, the input bias current is more often unidirectional. It can vary and depends on the amplifier.

So, what to conclude? If very low input bias current is important in your circuit, be aware. Look carefully at typical performance graphs to glean all available information. If you operate with input voltages that are near the positive or negative rails, you may have higher input bias current. This leads to another important point – input bias current will increase significantly with temperature.

This discussion applies to most common general-purpose CMOS and JFET amplifiers, but there are special-purpose amplifiers designed for ultra-low input bias current. They use creative protection circuitry with unique pinouts to achieve I_B in the range of 3 fA – three orders of magnitude lower than general-purpose devices.

Examples:

- The LMP7721 3-fA input bias current CMOS op amp.
- The INA116 ultra-low input bias current instrumentation amplifier.

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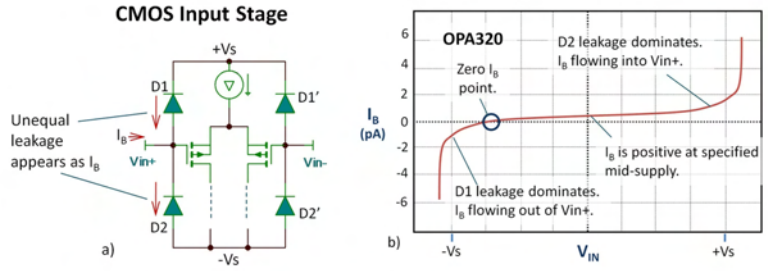


Figure 17: Protecting op amps from ESD and EOS using internal clamp diodes to the supply rail (a); input bias current versus input voltage (b).

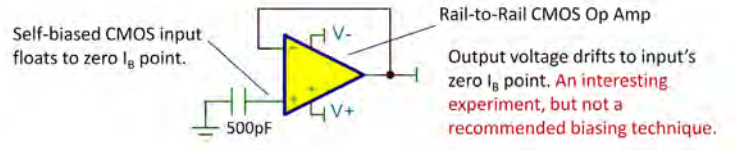


Figure 18: A rail-to-rail CMOS op amp with a self-biased input—not recommended!

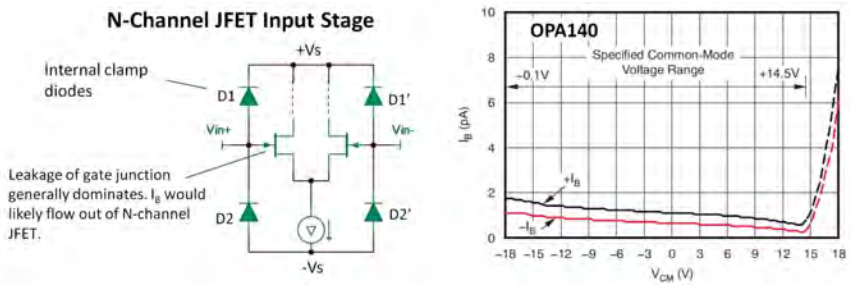


Figure 19: Input bias current is often unidirectional depending on the input amplifier, such as with the JFET-input amplifier shown here.

9. Temperature effects on input bias current

In section 8, I looked at the source of input bias current in complementary metal-oxide semiconductor (CMOS) and junction FET (JFET) amplifiers, finding that it comes from the leakage of one or more reverse-biased P-N junctions. I ended with a caution that these leakages increase significantly with temperature.

The reverse-biased leakage of a P-N junction has a strong positive temperature coefficient, approximately doubling for each 10°C increment in temperature. This exponential increase racks up quickly, as shown in the normalized graph of **Figure 20**. At 125°C, leakage climbs to approximately 1,000 times the room-temperature value.

The rate of increase can vary with diode characteristics, and the doubling of current may occur over a range of 8°C to 11°C. This increased bias current at high temperatures can be a significant problem in some circuits and may be a good reason to select a FET or CMOS operational amplifier (op amp) with a very low room temperature input bias current. In some cases, you may achieve lower I_B at high temperatures with a bipolar-input (BJT) op amp that does not have such a dramatic increase at high temperature.

The leakage generally continues to fall at lower temperatures, but other possible sources of leakage may alter the behavior. These stray leakages may have different temperature dependencies. To be honest, less is known about the behavior below room temperature because the higher leakage at room temperature and above is the greater concern. It is best not to place high confidence in behavior much below room temperature. The important issue at low temperatures is more likely to be possible water condensation, which can cause leakage to rocket upward.

As discussed in section 8, the input bias current of most CMOS op amps comes from the difference in leakage of two input-clamp diodes connected to the power rails. In a perfectly balanced world, the residual difference between two nearly equal leakages still has the same exponential temperature variation; it just starts at a lower initial value. The polarity of I_B is uncertain; and, with small differences in diode behavior, the net current may dip through zero at some temperature (the logarithmic graph shows the absolute value without a sign).

So, what to conclude? If very low input bias current is critical in your FET op amp circuit, carefully consider its increase with temperature. Study all of the specifications and typical performance graphs. Avoid placing sensitive circuitry near heat sources. Make your own measurements, if necessary. For really critical applications, there are special-purpose amplifiers with ultra-low input bias current. They use creative protection circuitry with unique pinouts to achieve I_B in the range of 3 fA at room temperature – three orders of magnitude lower than general-purpose devices.

Examples:

- The LMP7721 3-fA input-bias-current CMOS op amp.
- The INA116 ultra-low-input-bias-current instrumentation amplifier.

To see this original post with comments, click here.

A random quiz: On the film capacitors in **Figure 21**, what is the meaning and purpose of the black bands?

See Page 36 for the answer to this quiz.

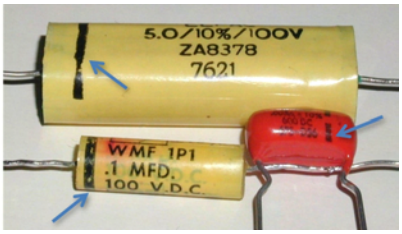


Figure 21: Film capacitors—what is the purpose of the marking stripe?

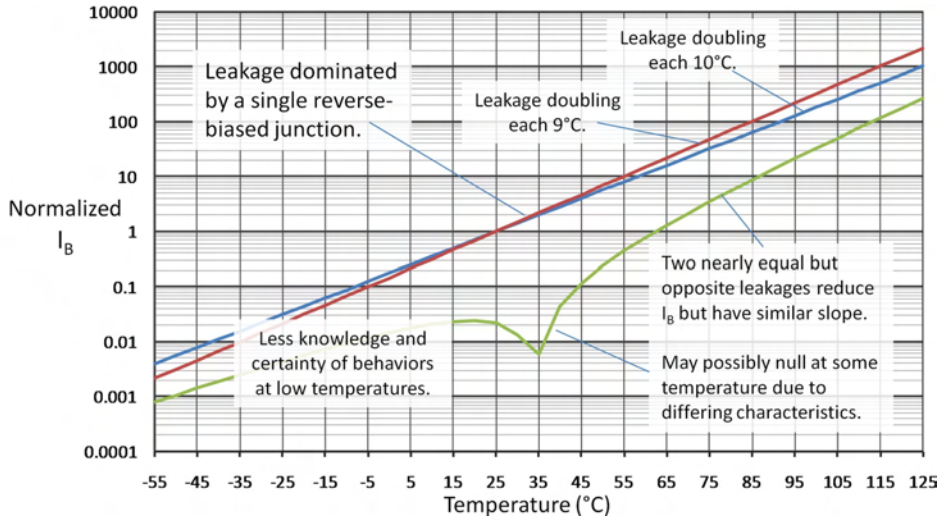


Figure 20: Reverse-biased leakage of a P-N junction approximately doubles with each 10°C increment in temperature.

10. Input bias current cancellation resistors: do you really need them?

Do you add a resistor to match the direct current (DC) resistance at the inputs of your operational amplifier (op amp) circuits? Check the circuits in **Figure 22**. Many of us were instructed to add Rb as "good practice," making its value equal to the parallel combination of R1 and R2. Let us look at the reason for this resistor and consider when it is appropriate and when it is not.

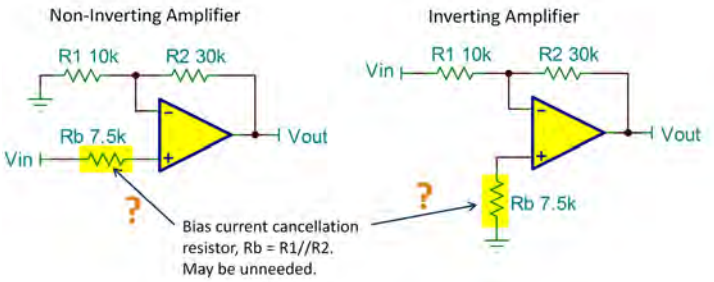


Figure 22: Resistor added to non-inverting input to match the source resistances.

The purpose of Rb is to reduce the voltage offset caused by the input bias current. If both inputs have the same input bias current, equal current flowing through equal resistances will create equal and opposite offset voltages. Thus, input bias current will not contribute to the offset voltage of the circuit. The basic idea has merit in some instances. But before adding Rb, is it always necessary?

Many times, the parallel resistance of R1 and R2 is low enough, and input bias current is low enough, that the offset created without Rb is insignificant. Before adding this resistor, calculate the error. Let us assume for this application that the input bias current of the op amp is 10 nA. Without using Rb, the input-referred offset voltage due to the input bias current will be:

$$\text{Input offset voltage due to } I_B = (10\text{ nA})\,(7.5\text{ k}\Omega) = 75\ \mu\text{V} \qquad (1)$$

Will 75 µV of input offset affect your circuit? Many times the answer will be no, so why add the resistor?

Consider the offset voltage of the op amp you are using. It may be pointless to be concerned with 75 µV if, for example, the offset-voltage specification of your op amp is 1 mV. So compare the error produced by the input bias current to the offset-voltage specification before routinely adding Rb to your circuit.

Transimpedance applications often use high feedback-resistor values to amplify very small currents (**Figure 23**). Here again, you may be tempted to add Rb to balance the resistance at both inputs. But these applications generally use FET- or complementary metal-oxide semiconductor (CMOS)-input op amps. With their very low input bias current, the offset error is generally very small.

Thermal noise produced by Rb and possible external noise pickup at this high-impedance node may be additional reasons to eliminate Rb. With minimal error from the input bias current, why add possible noise to the circuit?

There may occasionally be a clear and valid case for using a bias current cancellation resistor. But many circuits derive no significant benefit, and may even suffer reduced performance.

To see this original post, click here.

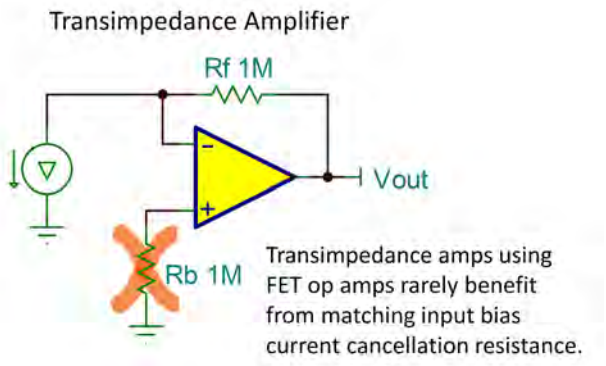
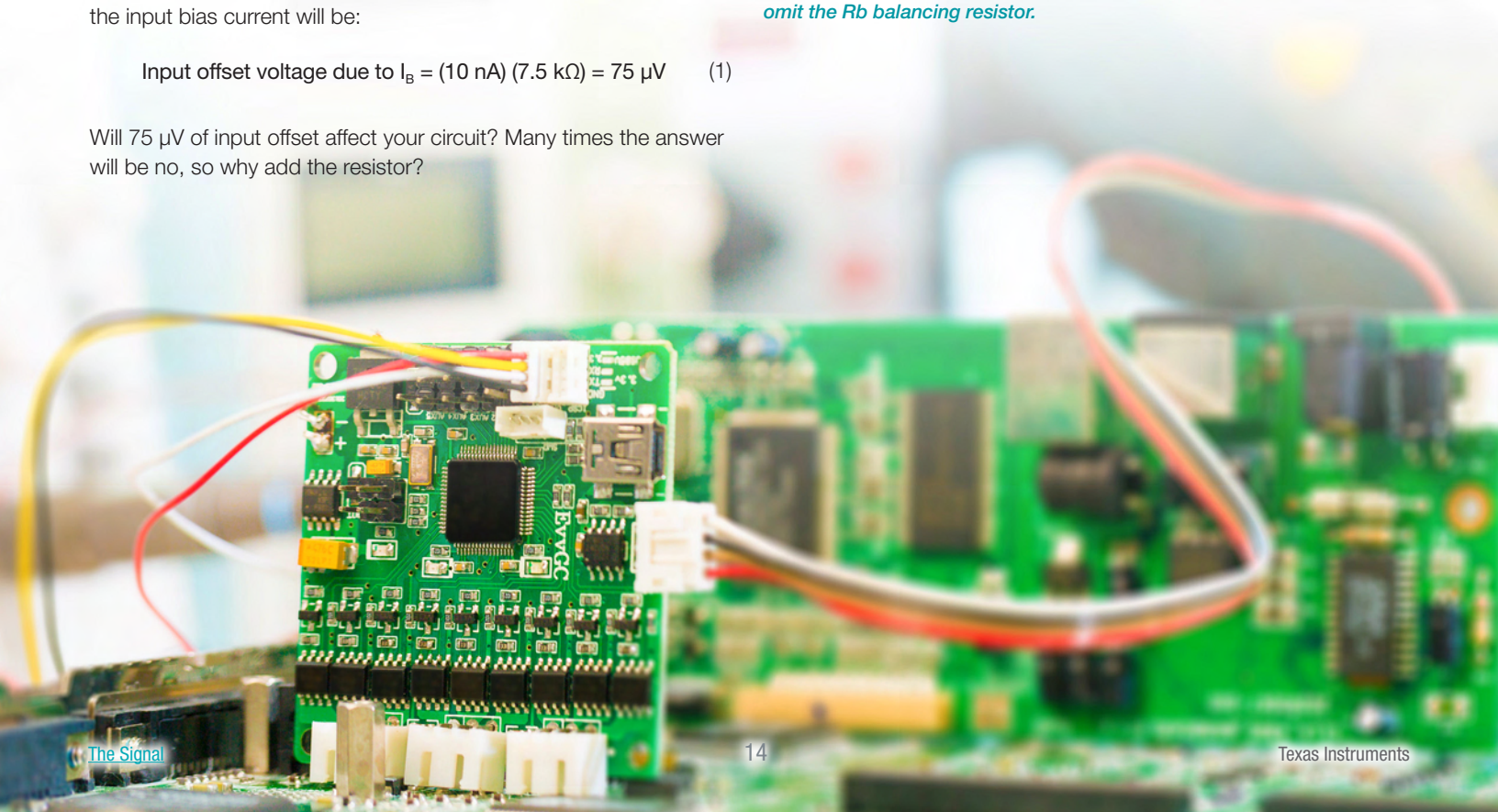


Figure 23: High gain transimpedance circuits using FET op amps should omit the Rb balancing resistor.



11. Internal input bias current cancellation of bipolar op amps

In section 10, I reviewed the use of an input-bias-current cancellation resistor to balance the source resistance at the two inputs of an operational amplifier (op amp). I concluded that this practice is often not necessary and may even be detrimental.

I ended the previous section by saying that there are certain op amps for which this practice is definitely not recommended: amplifiers with bipolar input transistors that have internal input bias current cancellation. Their current sources, I1 and I2, supply base current for the input transistor pair (**Figure 24**). These currents are derived by mirroring carefully matched base currents into the op amp's input terminals.

While these currents are accurately matched to the base current of the input transistor (typically within a few percent), they are not perfect. They leave a small residual input bias current that could be positive or negative. The residual current may be quite different on the two input terminals. They may even be opposite polarities. Any possible benefit from matching source resistance (as in **Figure 25**) relies on nearly matching input bias currents. Internal input bias current cancellation renders this practice useless.

Which op amps have input bias current cancellation? Datasheets sometimes do not make this feature apparent. The effects are generally revealed, however, in the details of input-bias-current specifications.

Figure 26a shows the input-bias-current specification for the OPA209, a low-noise op amp with input-bias-current cancellation. Note that the input bias current is preceded by a ± symbol to indicate that current could flow in either direction, your first hint. Also note that the specifications for input offset current are the same magnitude as the input bias current (actually identical on this op amp). These specifications reveal that this device has internal input bias current cancellation.

Figure 26b shows a hypothetical specification for the OPA209, assuming it did not have bias current cancellation. Note the much larger input bias current. And now, the input offset current is much smaller than the input bias current because the two input bias currents are nearly equal. Depending on the circuit and application, this hypothetical op amp might benefit from the use of a bias current cancellation resistor, as shown in **Figure 24**.

Internal input bias current cancellation is generally found on precision and low-noise op amps with input from bipolar junction transistors (BJTs) – ones that would otherwise have an uncomfortably high input bias current. Internal cancellation makes these amplifiers useful in a wider range of circuits.

Do you ever design circuits that rely on a known polarity of input bias current? It would not be wise with these canceled-input devices, right?

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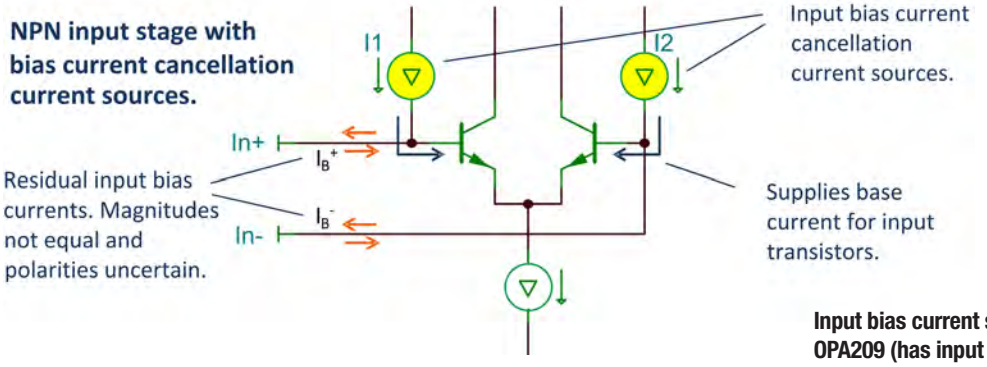

Figure 24: BJTs with internal current sources for input bias current cancellation.

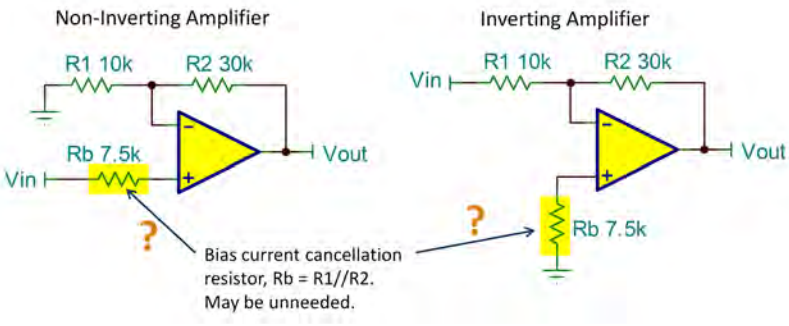

Figure 25: Op amp circuit with bias-current-cancellation resistor added to non-inverting input.

Input bias current specification for OPA209 (has input bias current cancellation).

Input Bias Current	Min	Typ	Max	Unit
Input bias current		±1	±4.5	nA
Input offset current		±0.7	±4.5	nA

± Indicates bias current could flow in either direction.

Input offset current same or similar to input bias current.

(a)

Hypothetical specification for same op amp assuming no bias compensation.

Input Bias Current	Min	Typ	Max	Unit
Input bias current		40	80	nA
Input offset current		1.5	5	nA

Offset current, $I_{OS} = (I_B^+) - (I_B^-)$

Input offset current much smaller than input bias current.

(b)

Figure 26: Specifications of an op amp with input-bias-current cancellation (a); and a similar op amp without input-bias-current cancellation (b).