19. Simulating gain bandwidth: the generic op amp model

It may not always be obvious how the gain-bandwidth product (GBW) of an [operational amplifier](http://www.ti.com/lsds/ti/amplifiers/op-amps/op-amps-overview.page) (op amp) may affect your circuits. Macromodels have a fixed GBW. Though you can look inside these models, it is best not to tinker with them. What to do?

You can use a generic op amp model in the simulation program with integrated circuit emphasis (SPICE) to check your circuits for sensitivity to GBW. Most SPICE-based circuit simulators have a simple op amp model that you can easily modify. Figure 47 shows one in [TINA-TI software.](http://www.ti.com/tool/tina-ti)

Figure 47: Using TINA-TI software to create a generic op amp model in SPICE to check circuits for sensitivity to GBW.

First, set its direct current (DC) open-loop gain to 1 M (120 dB). Then, a dominant pole frequency (entered in hertz) will create a GBW of the amplifier in megahertz. In this example, a 10-Hz dominant pole creates a GBW of 10 MHz. Figure 48 shows the open-loop response for three different GBWs: 5 MHz, 10 MHz and 100 MHz.

Figure 48: Open-loop response with GBWs of 5 MHz, 10 MHz and 100 MHz.

Note that that this simple model also includes a second pole (some folks call it a nuisance pole). In some cases, you may want to make this second pole a very high frequency, such as 10 GHz. This will create an ideal 90 degrees phase margin for any reasonable GBW. In this example, I set the second pole at 100 MHz, equal to the highest GBW that I am simulating. You can see the effect of this second pole in the 100-MHz GBW response, causing the open-loop response to bend downward at 100 MHz. It causes the unity-gain bandwidth to pull in to approximately 78 MHz, similar to what you might see with a real op amp of this GBW. Unity-gain bandwidth and GBW of a real op amp are not necessarily the same number.

> Active filter designs can be tricky to judge GBW requirements and are a good case for using this technique. [WEBENCH® Filter Designer,](http://www.ti.com/lsds/ti/analog/webench/webench-filters.page) used to design the Chebyshev filter in Figure 49, provides GBW recommendations, but its guidelines may be more stringent than needed in some circumstances. For this design, it recommends a 100-MHz or greater GBW to achieve nearly ideal filter-design characteristics. I simulated the design using the three GBWs shown in Figure 48: 5 MHz, 10 MHz and 100 MHz. With these results, you might decide that a GBW less than 100 MHz could be satisfactory. For final simulations, you should use the macromodel for the op amp you select.

Figure 49: A Chebyshev filter designed in WEBENCH Filter Designer software, but GBW may be more stringent than necessary.

I used the parameter-stepping function in TINA-TI software, varying the dominant pole to change the GBW. Other simulators have similar capability. Of course, you could change parameters manually, too. Either way, varying the GBW of a generic op amp model will give you some insight on its effect in your circuits.

To see this original post with comments, [click here](http://e2e.ti.com/blogs_/archives/b/thesignal/archive/2013/02/26/simulating-gain-bandwidth-the-generic-op-amp-model).

20. Slew rate: the op amp speed limit

Slewing behavior of [operational amplifiers](http://www.ti.com/lsds/ti/amplifiers/op-amps/op-amps-overview.page) (op amps) is often misunderstood. It is a meaty topic, so let us sort it out.

The input circuitry of an op amp circuit generally has a very small voltage between the inputs – ideally zero, right? But a sudden change in the input signal temporarily drives the feedback loop out of balance, creating a differential error voltage between the op amp inputs. This causes the output to race off to correct the error. The larger the error, the faster it goes; that is, until the differential input voltage is large enough to drive the op amp into slewing.

If the input step is large enough, the accelerator is jammed to the floor. More input will not make the output move faster. (Figure 50 shows why in a simple op amp circuit.) With a constant input voltage to the closed-loop circuit, there is zero voltage between the op amp inputs. The input stage is balanced, and the current IS1 splits equally between the two input transistors. With a stepfunction change in V_{IN} greater than 350 mV for this circuit, all of the IS1 current is steered to one side of the input transistor pair. That current charges (or discharges) the Miller compensation capacitor, C1. The output slew rate (SR) is the rate at which IS1 charges C1, equal to IS1/C1.

Figure 50: A large change in the input signal creates an output slewing condition.

There are variations, of course. Op amps with slew enhancement add circuitry to detect this overdriven condition and enlist additional current sources to charge C1 faster – but they still have a limited slew rate. The positive and negative slew rates may not perfectly match. They are close to equal in this simple circuit, but this can vary with different op amps. The voltage needed to slew an input stage (350 mV for this design) varies from approximately 100 mV to 1 V or more, depending on the op amp.

While the output is slewing, it cannot respond to incremental changes in the input. The input stage is overdriven and the output rate-of-change maxes out. But once the output voltage nears its final value, the error voltage across the op amp inputs reenters the linear range. Then the rate of change gradually reduces to make a smooth landing at the final value.

Figure 52: The slew rate is the same for any closed-loop gain but the onset of slewing is more gradual and occurs at higher output voltage in higher gains.

There is nothing inherently wrong with slewing an op amp – no damage or fines for speeding. But to avoid gross distortion of sine waves, you should limit the signal frequency and/or output amplitude so that the maximum slope does not exceed the amplifier's slew rate. Figure 51 shows that the maximum slope of a sine wave is proportional to VP and frequency. With 20 percent less than the required slew rate, the output is distorted into a nearly triangle shape.

> Large-signal square waves with very fast edges tilt on the rising and falling edges according to the slew rate of the amplifier. The final portion of a rising or falling edge will have rounding as the amplifier reaches its small-signal range, as shown in Figure 50.

In a noninverting circuit, a minimum 350-mV step is required to make this op amp slew, regardless of gain. Figure 51 shows the slewing behavior for a 1-V input step with gains of 1, 2 and 4. The slew rate is the same for each gain (Figure 52). In $G = 1$, the output waveform

transitions to small-signal behavior in the final 350 mV. In $G = 2$ and $G = 4$, the small-signal portion is proportionally larger because the error signal fed back to the inverting input is attenuated by the feedback network. If connected in a gain greater than 50, this amplifier would be unlikely to slew because a 350-mV step would overdrive the output.

Slew rate is usually specified in voltage per microseconds, perhaps because early [general-purpose op amps](http://www.ti.com/lsds/ti/amplifiers/op-amps/general-purpose-op-amps-overview.page) had slew rates in the range of 1 V/μs. Very [high-speed amplifiers](http://www.ti.com/lsds/ti/amplifiers/op-amps/high-speed-op-amps-overview.page) are in the 1,000-V/μs range, but you would rarely see it written as 1 kV/μs or 1 V/ns. Likewise, a [nanopower op amp](http://www.ti.com/lsds/ti/amplifiers/op-amps/ultra-low-power-op-amps-overview.page) might be specified as 0.02 V/μs but seldom as 20 V/ms or 20 mV/μs. There's just no good reason why for some things; it is just the way we do it.

To see this original post with comments, [click here](http://e2e.ti.com/blogs_/archives/b/thesignal/archive/2013/06/03/slew-rate-the-op-amp-speed-limit).

21. Settling time: a look at the character of the settling waveform

Settling time is the time required for an [operational amplifier](http://www.ti.com/lsds/ti/amplifiers/op-amps/op-amps-overview.page) (op amp) to respond to an input-voltage step and then enter and stay within a specified error range of the final value. It is important in applications that drive an [analog-to-digital converter](http://www.ti.com/lsds/ti/data-converters/adcs/adcs-overview.page) (ADC), digitizing rapidly changing inputs. But let us look beyond the definition and focus on the character of settling waveforms.

Figure 53: As closed-loop gain is increased, bandwidth is reduced and response is slower.

In [section 20,](#page-1-0) I showed how an op amp transitions from a slewing ramp to a small-signal settling portion of the waveform; see Figure 53. As the gain increases, you can see the slower closure to final value.

This is due to reduced closed-loop bandwidth in higher gain. This example op amp is tuned to have virtually 90 degrees phase margin in $G = 1$. Notice that there is no overshoot, even in unity gain. Its virtually perfect first-order response serves as a benchmark for comparison, but you are unlikely to find an op amp with such generous phase margin in $G = 1$.

The response in Figure 54 is more realistic (maybe a bit pessimistic). These waveforms are produced by the same op amp but with an approximately 35 degrees phase margin at $G = 1$. (The ideal op amp responses are also shown for comparison.) Its smallsignal overshoot is approximately 32 percent in $G = 1$. It appears to be less overshoot with the 1-V step shown because only the smallsignal portion of the response produces this overshoot behavior. A larger input step would have the same magnitude overshoot but look proportionally even smaller. That is why you should always [check overshoot and stability with small input-voltage steps.](http://e2e.ti.com/blogs_/archives/b/thesignal/archive/2012/09/10/spiceing-op-amp-stability)

Figure 55 shows an expanded view of the $G = 1$ small-signal response. Note that the settling of the final humps to a final steady value appear to require two complete up/down cycles. The wiggles continue, smaller and smaller – beyond the resolution of this graph. An additional cycle or two might be required to settle to high accuracy.

When you visualize this final settling behavior, you may imagine a compressed time scale in the final over/undershoots, as if the natural frequency of this ringing is shifting upward with each hump. But every

> cycle of settling requires the same time. Excessive ringing can be costly – a good reason to select a reasonably well-behaved op amp.

The true settling time to high accuracy (16 bits or greater) often includes other factors. Behaviors produced by fancier phase-compensation techniques and thermal effects can add to the settling time. The amplifier can also be perturbed by glitches from the input switching of an ADC. Optimizing all this can be tricky business. Still, it is important to visualize the primary effects at work –

slew rate combined with a second-order system response.

To see this original post with comments, [click here](http://e2e.ti.com/blogs_/archives/b/thesignal/archive/2013/06/11/settling-time).

Figure 55: An expanded view of a G = 1 small-signal showing that the period of ringing is constant.

Figure 54: Waveforms produced by the same op amp, but with approximately 35° phase margin at G = 1.