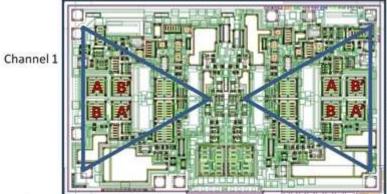


Bruce Trump Oct 30, 2012

Some circuits benefit when the characteristics of two more op amps are closely matched. So inside a dual or quad op package, how closely do their behaviors match? Hummm?

The most common request on our <u>precision amplifier E2E forum</u> is for matching offset voltage and offset voltage temperature drift. If you are making your own <u>instrumentation amplifier</u>, for example, matching op amp offsets would produce a net zero offset. But check out the geometry of the situation in figure 1.



Channel 2

This dual op amp has a cross-quad, common centroid input stage and a well balanced layout. Transistor A and A' are in parallel. B and B' are in parallel.

Figure 1.

Each op amp has input transistors that must be well matched to achieve low offset voltage of that one amplifier. We go to great lengths to carefully match these two transistors (and perhaps other pairs of components). The cross-quad connection shown is the most basic technique—each transistor divided into two halves, A and A', B and B' so that the geometric center is the same for both pairs. Today, we intermingle transistors in more elaborate ways. *Common centroid* is the general term.

So here's the point... We go to extremes to carefully match two common-centroid input stage transistors on one side of the IC. What remains is residual random mismatch. Why would another two transistors on the other side of the IC have the same random mismatch? The answer is that they probably don't. There could possibly be other causes of offset that are matched, but we try to eliminate all sources of systematic offset so any remaining is likely to be random. Sorry, but offset voltage is not likely to be closely matched. Here is how we usually show it in the data sheet:

Offset Voltage specifications for OPA2171...

Input Offset Voltage	Min	Тур	Max	Units
Input Offset Voltage		±0.25	±1.8	mV
Temperature Drift		±0.3	±2	μV/°C

± Indicates offset voltage could be either polarity in each op amp.

Figure 2.

So characteristics that rely on matching of internal components—op amps in a dual or quad are unlikely to match any better than single op amps. Examples include:

- Offset Voltage—relies on transistor matching
- Offset Voltage Temperature Drift—relies on transistor matching
- Input Offset Current of a bipolar (BJT) amplifier—relies on match of transistor beta

Characteristics that depend on a fundamental characteristic of the internal components—op amps in a dual or quad are likely to be better matched than single op amps:

- Gain-Bandwidth Product-depends on absolute capacitor values and current
- Slew Rate—depends on absolute capacitor values and current
- Input Bias Current of BJT op amp without input bias current cancellation

Old-timers may remember when early dual op amps did tend to match better as a percentage of their specified value. But the performance of these older devices was modest, at best. They were very simple designs, lacking the very careful attention to internal component matching and well-balanced design and IC layout that are common today.

Thanks for reading and comments welcome,

Bruce email: thesignal@list.ti.com (Email for direct communications. Comments below.)

Index to all The Signal blogs.



Soufiane Bendaoud over 12 years ago

Hi Bruce, a frequent questions I used to get was "what do I do with the unused op amp?" of course this could apply for a dual or a quad too. So my answer was usually connect it in a positive unity gain (follower), assuming you have a split supply. I personally never experienced a problem on the bench with such a configuration, what do you think?



Bruce Trump over 12 years ago

Soufiane-- Yes, this is a frequent question and it's already on my short list of future topics. Your suggestion for dual supply applications is perfect. It gets tricky in single supply situations. More later.



Steve Marum over 12 years ago

Would another source of mismatch be that the common centroid of channel 1's input transistors is in a different location than the common centroid of channel 2's input transistors? For example, a thermal gradient across the chip will affect each pair differently.



Bruce Trump over 12 years ago

Yes, Steve. Layouts of this type are never perfectly symmetrical, in spite of our best efforts. So two common-centroid layouts get somewhat different interfering stimuli. Furthermore, the common-centroid pair rejects linear gradients (thermal and processing) well but higher order gradients, not so well. Another important factor is that the individual transistors that comprise a common-centroid pair have their own random mismatches. Random mismatches just don't match very well.