# DESIGNING WITH DIGITAL IC'S

*One-shots and clocks are among the most important digital circuits. This month we learn about those circuits and how they are used.*

JOSEPH J. CARR

**Part 8** THE MONOSTABLE multivibrator (or "one-shot") can be used in a variety of applications. Those circuits are used to clean up noisy digital signals, to "stretch" pulses, as timers, and on and on. The circuit is termed "monostable" because it has only one stable output state. That stable state might be either high or low depending on the design. Normally, the monostable remains in the stable state. But when a valid trigger pulse is received, the monostable goes to the unstable state, but only for a predetermined period of time. The monostable output then reverts back to the stable condition.

There are two main categories of monostable multivibrators: retriggerable and nonretriggerable. Of those, the latter is the type most people think of when considering those circuits. Thus, unless otherwise stated, assume that a monostable multivibrator is nonretriggerable.

Figures 1 and 2 show the timing diagrams for the two types of monostables. Figure 1 shows a nonretriggerable monostable in which the stable state is low. A trigger pulse is received at time $t_1$, so the output snaps high and remains so for period T. When period T expires, the output returns to the low state. It remains low until another valid trigger pulse is received ($t_4$).

The essential characteristic of a nonretriggerable circuit is shown in Fig. 1. That characteristic can be seen by examining what happens at $t_2$. At that time, a second trigger pulse is received, but since the output is in the unstable (active) state that pulse is ignored. The pulse at time $t_2$ has no effect on the output; such a trigger pulse is considered invalid.

One common application of nonretriggerable monostables is switch debouncing. Ordinary mechanical switches are noisy when the contacts close. Because the two electrical contacts of the switch "bounce" one or more times before a solid connection is made. The period of contact bounce might be several milliseconds, during which each bounce creates a noise pulse. Those pulses can cause many problems for digital circuits, so they must be suppressed.

To use a nonretriggerable monostable for that task, select one whose output period, T, is longer than the bounce period (5 ms, for instance). When the monostable is inserted in series with the switch, its output will go high when the first bounce pulse is received, and will remain in that state until after the bounce pulses die out. As for the balance of the digital circuit, all it will see is the 5 ms one-shot pulse; it is thus spared the indignity of a noisy signal.

The timing diagram for a retriggerable monostable is shown in Fig. 2. Again, the period of the monostable multivibrator is T, which is initiated by a trigger pulse at time $t_1$. Normally, the output would remain high until T expired at time $t_3$. But at time $t_2$, a second trigger pulse is received. That pulse "retriggers" the circuit for another period T. The total time that the output remains high is not 2T, but T plus the expired portion of the first period (i.e. $T + (t_2 - t_1)$).

One application of the retriggerable monostable is in alarm circuits designed to monitor repetitive events. For example, consider its use in a medical respiration alarm. The alarm senses the patient's breathing and generates a pulse in response to that breathing that is used to trigger the monostable. The period of the monostable is set such that a normal breathing pattern will cause continuous retriggering. If the breathing pattern is disrupted, the monostable does not receive a retriggering pulse so the circuit "times out" and the alarm sounds.

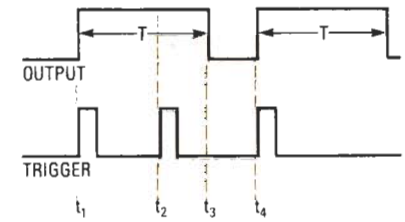


**FIG. 1—TIMING DIAGRAM for a non-retriggerable monostable multivibrator.**

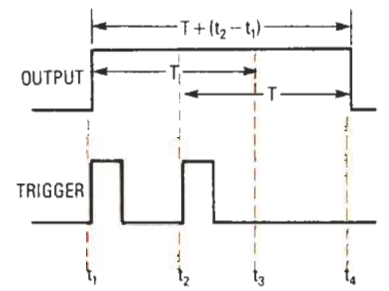


**FIG. 2—TIMING DIAGRAM for a retriggerable monostable multivibrator.**

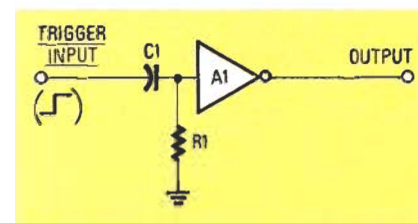


**FIG. 3—INVERTER-BASED monostable multivibrator. As shown, the circuit is positive-edge triggered.**

## Some circuit examples

The simple circuit of Fig. 3 is an example of a half-monostable or quasi-monostable multivibrator. A1 is a CMOS inverter (or a CMOS gate wired as an inverter). When a trigger pulse is received, the output will snap low (active), and it remains low for a period of time determined by the values of R1 and C1. A serious constraint on that circuit is that the trigger pulse must be longer than the output period set by R1 and C1. As shown, the circuit goes low on the positive (leading) edge of the triggering pulse; that is called positive-edge triggering. To obtain negative-edge triggering (triggering on the negative, or trailing edge of the pulse), tie R1 to +V instead of ground.

Figure 4 shows a monostable based on a 4013 CMOS D flip-flop. In that circuit, the D input of the 4013 is connected to +V, so that input is always high. The CLR

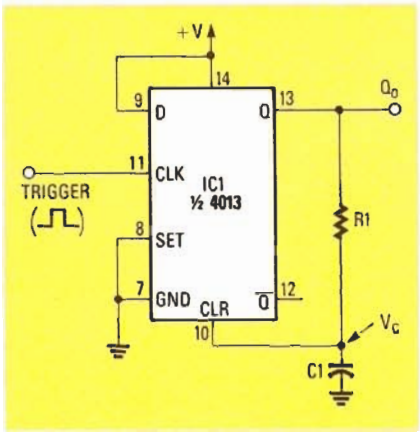


**FIG. 4—A FLIP-FLOP can be configured as a monostable multivibrator. Here is one circuit that uses a 4013 D flip-flop.**

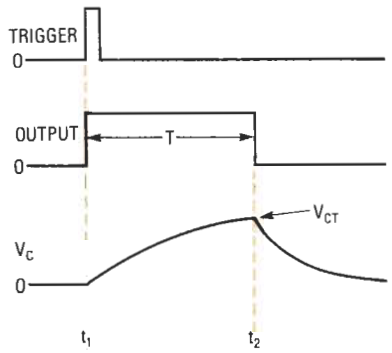


**FIG. 5—TIMING DIAGRAM for the circuit shown in Fig. 4.**

input is connected to capacitor C1, so it will initially be low. That input will go high, however, when the voltage across C1, $V_C$, reaches the appropriate level. Since C1 is charged through R1, which is connected to the Q output, C1 will reach the level where the CLR input will go high at some time T after Q goes high (the time determined by the value of R1 × C1).

The timing diagram for that circuit is shown in Fig. 5. Immediately prior to time $t_1$, the voltage across C1 (i.e. $V_c$) is zero, and the Q output is low. At $t_1$, a trigger pulse is received, which causes the Q output to go high. That causes a current to flow through R1, which causes C1 to charge and $V_C$ to rise. Voltage $V_c$ will continue rising until it reaches the "clear trip" voltage. That is the voltage required at the CLR input to force the Q output low. At that instant, $t_2$, Q snaps low and capacitor C1 begins discharging through R1. The output was high for a fixed period ($t_1 - t_2$) that was determined by the time constant R1 × C1 and the voltage required to clear the flip-flop.

But note what happens between time $t_2$ and $t_3$. That time is a "refractory" period during which the flip-flop either won't retrigger, or will produce an erroneous output period, because capacitor C1 was partially charged at the instant the trigger pulse was received (i.e. $V_C$ is not 0).

The refractory period can be shortened considerably by the adding a quench diode (D1 in Fig. 6) to the circuit. The quench diode is placed in parallel with R1 in such a way that it is reverse-biased when Q is low (or unbiased if $V_C$ is less than or equal to 0.6 volts). During the active period ($t_1 - t_2$), diode D1 is reverse-biased so it will not affect the timing. (An exception to this rule is long-duration timers where the value of R1 is very large, and the leakage resistance of D1 is less than 100 × R1.) But when the flip-flop is cleared, and Q goes low, voltage $V_C$ forward-biases D1, forcing it to conduct. The charge on C1 is thus "dumped" through diode D1, shortening the discharge time and, as a result, the refractory time.

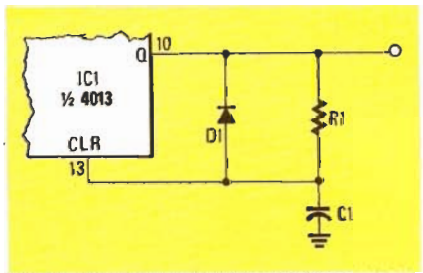


**FIG. 6—ADDING A QUENCH DIODE shortens the refractory period.**

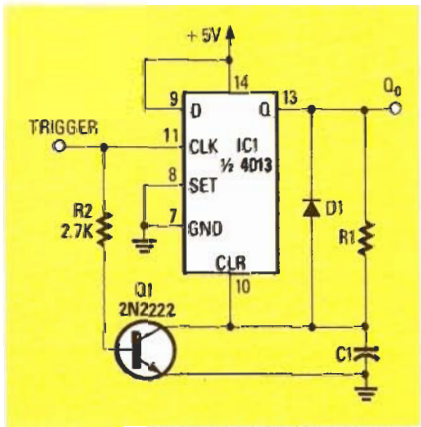


**FIG. 7—THE CIRCUIT of Fig. 4 can be made retriggerable by modifying it as shown here.**

Figure 7 shows a version of the retriggerable monostable built around a D flip-flop. In that circuit, a transistor switch is added. Its purpose is to discharge $V_C$ when a positive trigger pulse is received. Such a pulse will forward bias Q1, thereby connecting its low collector-emitter resistance across C1. That transistor must have a high enough beta to be fully saturated by the trigger pulse, and a $V_{CE(SAT)}$ rating of 0.6 volts or less.

Note that neither circuit shown in Fig. 5 and Fig. 6 will return to exactly 0 volts until long after the $t_1 - t_2$ period has expired. That's because D1 will quench $V_C$ down to only 0.6 or 0.7 volts, which is the level required to forward-bias the diode. Normally, however, that poses no serious problems.

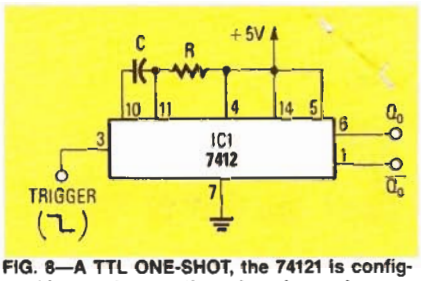


**FIG. 8—A TTL ONE-SHOT, the 74121 is configured here to be negative-edge triggered.**

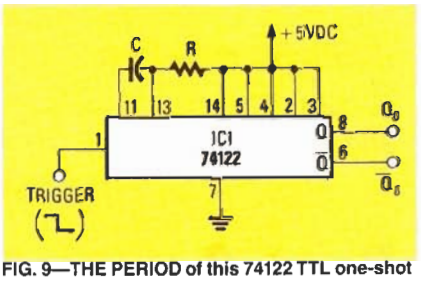


**FIG. 9—THE PERIOD of this 74122 TTL one-shot is determined by R1 and C1.**

A pair of TTL one-shot devices are shown in Figs. 8 and 9: the 74121 and 74122. Both of those devices are shown with negative-edge triggering inputs. The period of the output pulse is determined by: T = 0.69R1C1, where T is the period in seconds, the resistance of R1 is measured in ohms, and the capacitance of C1 is measured in microfarads.

That relationship can be rearranged to yield either C1 or R1 in terms of T, which is the usual situation when selecting values. (Normally, we know the desired T, will select an arbitrary C1, and then calculate R1.) Let's work out an example. Suppose we want a 10 microsecond (10μs) pulse. Let's select a trial value of .001 μF for C1 and see if the required value of R1 is reasonable:

$$R1 = T/0.69C1$$

$$R1 = \frac{1 \times 10^{-5}}{(0.69)\ 1 \times 10^{-9}}$$

$$R1 = 14{,}493 \text{ ohms}$$

For most applications, a 15 kilohm unit (a standard value) can be used.

Both 74121 and 74122 are TTL devices, so the Q output will be 0 to 0.8 volts for low, and 2.4 to 5.0 volts for high. The $\overline{Q}$ outputs use the same voltages levels.

The 555 is an extremely popular timer/oscillator that uses bipolar technology. The device will operate at supply voltages ranging from +4.5- to +18-volts DC, so it is compatible with most IC digital logic families. In addition, standard 555 outputs sink or source up to 200 mA of current, so the device can be used to drive relays, LED's, and some incandescent lamps without the need for external transistors.

Figure 10 shows a 555 configured as a monostable multivibrator. The trigger in-

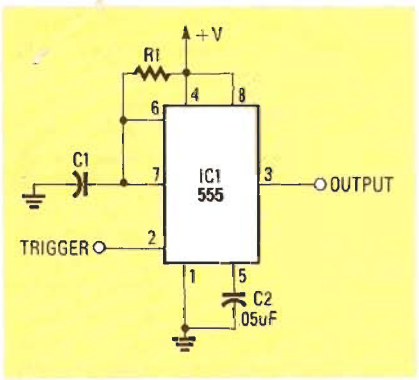


FIG. 10—A POPULAR DEVICE, the 555 timer IC is shown here configured as a monostable multivibrator.

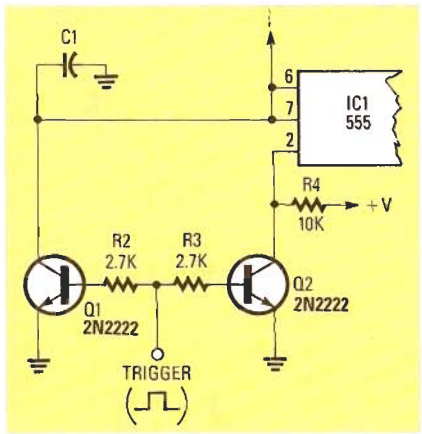


FIG. 11—THE CIRCUIT of Fig. 10 can be modified to make it retriggerable as shown here.

put is normally high. That input must be dropped below +V/3 for triggering to occur. When such a trigger pulse is received, the output terminal snaps high for a period that is determined by T = 1.1R1C1, where T is the time in seconds, the resistance of R1 is measured in ohms, and the capacitance of C1 is measured in farads.

For example, find the period of the output pulse when R1 = 47K and C1 = 0.1μF. Solving, T = (1.1)(47,000)(1 × $10^{-7}$); T = 0.0052 seconds = 5.2 ms.

A retriggerable 555 monostable multivibrator circuit is shown in Fig. 11. Similar to the D-flip-flop based circuit we looked at earlier, that circuit uses an external transistor switch to dump the charge in the timing capacitor. Both transistors are turned on by the positive-going trigger pulse.

Note that the polarity of the trigger pulse is reversed from the circuit of Fig. 10. Normally, the trigger input of the 555 (pin 2) is held at +V by pull-up resistor R4. But when a positive trigger pulse forward-biases Q2, pin 2 is brought near ground—so triggering is effected. At the same time, transistor Q1 is also forward-biased, so it will have an extremely low collector-emitter resistance. Since that resistance is shunted across capacitor C1, the charge on C1 is bled off rapidly to ground. That action has the effect of resetting the timing of the output pulse to zero. The output pulse will remain high for period T = 1.1R1C1, plus whatever percentage of the period that had expired prior to receipt of the second trigger pulse.

Our last monostable multivibrator is the operational amplifier version shown in Fig. 12; its timing diagram is shown in Fig. 13.

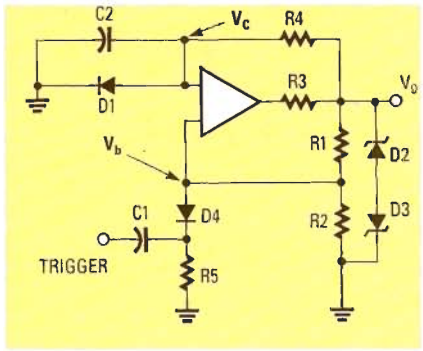


FIG. 12—AN OP-AMP COMPARATOR is used here as the heart of a monostable multivibrator.

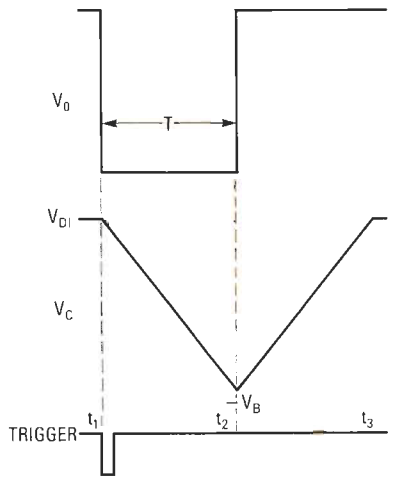


FIG. 13—TIMING DIAGRAM for the circuit of Fig. 12.

That circuit uses an operational amplifier as a comparator. A comparator is an op-amp that is used to compare the relative states of its two inputs. Thus, if one input is a known reference level, and the other is variable, the output of the comparator will indicate whether the variable input is at a higher or lower voltage than the reference.

The stable state of the circuit in Fig. 12 is high. While the circuit is in that stable, untriggered state, the output is at $+V_O$, while $V_C$ is clamped to approximately 0.7 volts by diode D1. On receipt of a trigger pulse, the output snaps to $-V_O$, which causes $V_C$ to begin charging through R4 towards $-V_O$. At some point ($t_2$), $-V_C$ will be equal to $-V_B$, and the output will snap high again (clamped to 0.7 VDC by D1). The duration of the active-low output pulse ($t_1 - t_2$) is:

$$T = (RC)\ln\frac{1 + (V_{D1}/V_O)}{1-\beta}$$

Where T is the output duration in seconds, R is the resistance of R4 in ohms, C is the capacitance of C2 in farads, and β is equal to R2/(R1 + R2). If $V_O$ is much greater than $V_{D1}$, and R1 = R2, then that equation can be simplified to T = 0.69RC.

Diodes D2 and D3 are used to clamp the output to some specific value. $+V_O$ is clamped to $V_{D2}$ + 0.7 volts, while $-V_O$ is held to $V_{D3}$ + 0.7 volts. Normally, $V_{D2} = V_{D3}$, and the output voltage is symmetrical.

## Clocks

Many circuits and devices depend upon a clock signal for proper operation. Even certain circuits made from non-clocked devices require a clock signal for synchronization of events.

But, what is a clock signal? It is a chain of squarewaves or pulses that is generated by a circuit called an astable multivibrator. As its name indicates, an *a*stable is a circuit that has no stable states. Once triggered the output of the circuit will snap back and forth between high and low.

Some of the clock circuits we'll be looking at in the rest of this article are based on inverters (TTL or CMOS). Instead of using dedicated IC's to generate a clocking signal, it is often possible to use spare NAND or NOR gates to form inverters. Figures 14-*a* and 14-*b* show two ways to use two-input NAND gates as inverters—either tie both inputs together or tie the unused input permanently high. Figures 14-*c* and 14-*d* show how NOR gates can be used as inverters. That is done either by tying the two inputs together, or by tying the unused input *low*.

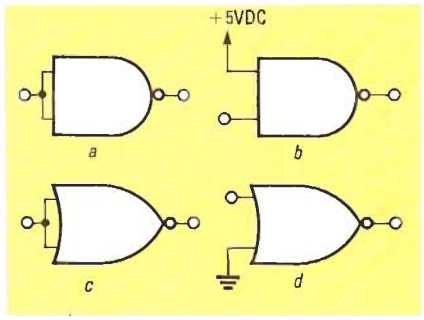


FIG. 14—INVERTERS can be fashioned from leftover NAND and NOR gates.

## TTL Clocks

Figure 15 shows the use of two TTL inverters (or inverter-connected gates per Fig. 14) in a clock circuit. Two resistors are used to bias the inverters, and each resistor is connected from the output back

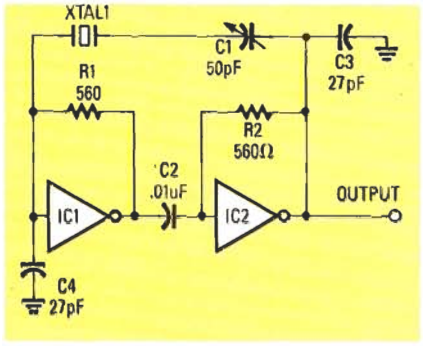


FIG. 15—TWO INVERTERS are used in this astable multivibrator.

to the input of its own inverter. The output of IC1 is capacitor-coupled to the input of IC2. A feedback network, consisting of a variable capacitor and a crystal, determines operating frequency. That network is connected between the output of IC2 and the input of IC1.

The operating frequency is determined mainly by the crystal, and to a lesser degree by capacitor C1. The effect of C1 is to change the resonant frequency of the crystal a small amount by changing its capacitive load. Thus the capacitor acts as a "fine-tuning" control. If operating frequency is not critical, C1 can be replaced with a fixed capacitor.

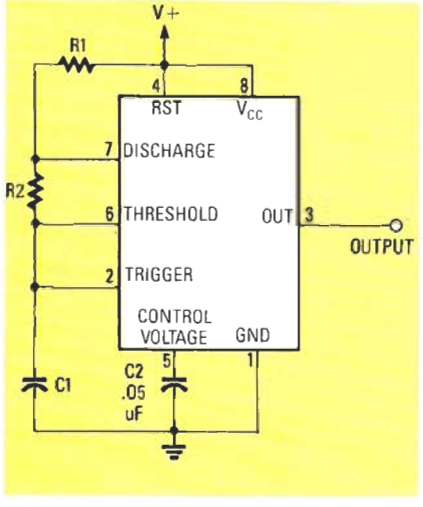


FIG. 16—THE FREQUENCY of this 555-based astable is determined by R1, R2, and C1.

The clock circuit shown in Fig. 16 is based upon the 555 IC timer. The output frequency is a function of R1, R2, and C1, and is found from:

$$f = \frac{1.44}{C1(R1 + 2R2)}$$

where $f$ is the frequency in hertz, the resistances of R1 and R2 are measured in ohms, and the capacitance of C1 is measured in farads.

Note that the 555 is not actually a TTL circuit. It is a bipolar IC that can operate at supply voltages from +4.5- to +18-volts DC. If a supply voltage of +5 is used, then the 555 will work with TTL circuits. The 555 output (pin 3) will sink or source up to 200 mA, so it can drive more TTL devices than a "standard" TTL output.

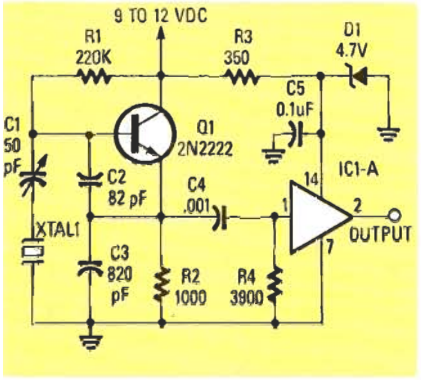


FIG. 17—IN THIS TTL-COMPATIBLE astable a bipolar crystal oscillator drives a 7414 Schmitt trigger.

One last TTL-compatible clock circuit is shown in Fig. 17. That circuit uses a bipolar crystal oscillator that drives a 7414 TTL Schmitt trigger. The oscillator shown operates from about 700 KHz to 15 MHz, depending on the crystal used. The exact frequency is set by using trimmer capacitor C1. Ordinarily one would not use a circuit such as the one shown in Fig. 17 unless a precise oscillator frequency is required.

CMOS clock circuits can operate from a wider range of supply voltages than TTL, and they generally require less current. Several different forms of CMOS astable multivibrator/clock circuits are possible.

Figure 18 shows a simple RC-timed circuit based on the 4093 CMOS Schmitt trigger. The trigger-circuit output will snap high when a positive-going input reaches a given voltage (V1), and snaps low when the same input voltage reaches a second point (V2) in the negative-going direction. The values of V1 and V2 vary with supply voltage used. In the circuit shown, when +V = 5, V1 = 2.9 and V2 = 2.3; when +V = 10, V1 = 5.9 and V2 = 3.9. The hysteresis of a Schmitt trigger is V1 − V2, so it is 0.6 volts when +V = 5, and 2 volts when +V = 10.

The 4093 is basically a two-input NAND gate with Schmitt inputs. Since one input is tied permanently high, circuit action is controlled entirely by the input that is connected to R and C. When power is first

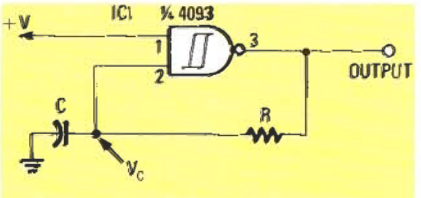


FIG. 18—THIS CMOS ASTABLE is based on the 4093 Schmitt trigger.

applied, the voltage across the capacitor, $V_C$, is zero, so the input to the 4093 is low. Given the rules for NAND-gate operation, that means that the output is high. Thus, one end of resistor R sees a high potential so capacitor C charges at a rate determined by the RC time constant and the output voltage. When $V_C$ reaches the positive-going trip point, the output snaps low. At that point, the voltage across the capacitor begins to discharge through R. That discharge continues until $V_C$ reaches the lower trip point, and the output snaps high again. That process repeats, and the result is a squarewave output (see Fig. 19).

Figure 20 shows another CMOS clock circuit; that one is based on either a pair of

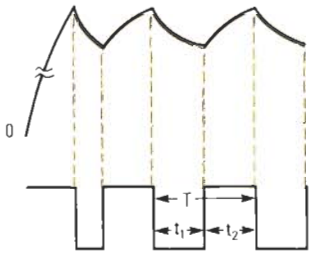


FIG. 19—TIMING DIAGRAM for the circuit of Fig. 18.

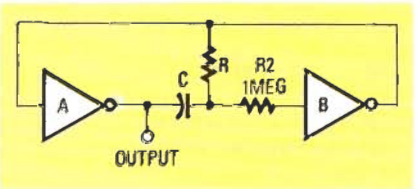


FIG. 20—THE OUTPUT FREQUENCY is determined by the values of R and C.

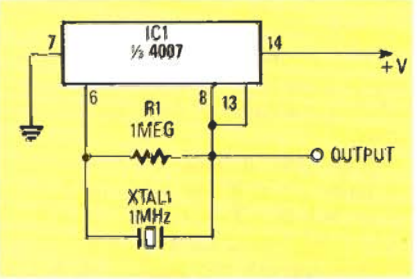


FIG. 21—THE CRYSTAL in this circuit controls the operating frequency.

inverters or inverter-connected gates. The circuit of Fig. 20 bears a certain similarity to the TTL oscillator shown earlier, but its frequency is determined by the R-C combination (not a crystal). The operating frequency, in hertz, is approximately 1/(2.25RC), where R is measured in ohms and C in farads.

A 1-MHz CMOS crystal oscillator, based on the 4007 is shown in Fig. 21. The crystal in the feedback path controls the operating frequency.

The so-called "classic" CMOS crystal oscillator shown in Fig. 22 first appeared in some of the earliest RCA applications

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