Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers

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abstract: *A unity gain IC power buffer that uses NPN output transistors while avoiding the usual problems of quasi-complementary designs is described. Free of parasitic oscillations and stable with large capacitive loads, the buffer has a 20MHz bandwidth, a 100V/μs slew and can drive ±10V into a 75Ω load. Standby current is 5mA. A number of applications using the buffer are detailed, and it is shown that a buffer has many uses beyond driving a heavy load.*

introduction

An output buffer can do much more than increase the output swing of an op amp. It can also eliminate ringing with large capacitive loads. Fast buffers can improve the performance of high speed followers, integrators and sample/hold circuits, while at the same time making them much easier to work with.

Interest in buffers has been low because a reasonably priced, high-performance, general purpose part has not been available. Ideally, a buffer should be fast, have no crossover distortion and drive a lot of current with large output swing. At the same time, the buffer should not eat much power, drive all capacitive loads without stability problems and cost about the same as the op amps it is used with. Naturally, current limiting and thermal overload protection would be nice.

These goals have been a dream for twenty years; but thanks to some new IC design techniques, they have finally been reached. A truly general purpose buffer has been made that is faster than most op amps but not hard to use in slow applications. It is manufactured using standard bipolar processing, and die size is 50 × 82 mils.

The electrical characteristics of the buffer are summarized in table I. Offset voltage and bias current win no medals; but the buffer will usually be driven from an op amp output and put within the feedback loop, virtually eliminating these terms as errors. Loaded voltage gain is mostly determined by the output resistance. Again, any error is much reduced with the buffer inside a feedback loop.

Unloaded, the output swings within a volt of the positive supply and almost to the negative rail. With ±150mA loading, this saturation voltage increases by 2.2V. Except for output voltage swing, performance is little affected for a total supply voltage between 4V and 40V. This means that it can be powered by a single 5V logic supply or ±20V op amp supplies.

Bandwidth and slew rate decrease somewhat with reduced load resistance. The values given in table I are for a 100Ω in parallel with 100pF. The speed is quite impressive considering that quiescent current is but 5mA.

table I. Typical performance of the buffer at 25°C. Supply voltage range is 4V to 40V.

parameter	value
output offset voltage	70mV
input bias current	75μA
voltage gain	0.999
output resistance	7Ω
positive saturation voltage	0.9V
negative saturation voltage	0.1V
output saturation resistance	15Ω
peak output current	±300mA
bandwidth	22MHz
slew rate	100V/μs
supply current	5mA

design concept

The functional schematic in figure 1 describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q30, such that the collector current of the output follower, Q29, never drops below the quiescent value (determined by I_1 and the area ratio of Q12 and Q28). As a result, the high frequency response is essentially that of a simple follower even when Q30 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V^+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower current, giving low output resistance at low quiescent current. The output will swing to the negative rail, which is particularly useful with single-supply operation.

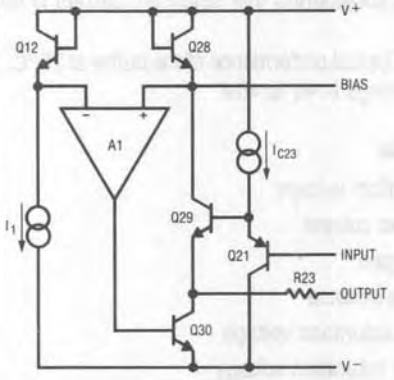


figure 1. In the buffer, main signal path is through followers Q21 and Q29. Op amp keeps Q29 turned on even when Q30 is supplying load current, so response is that of followers.

basic design

Figure 2 shows the essential details of the buffer design using the concept in figure 1 (for clarity, parts common to simplified and developed schematics use the same number). The op amp uses a common base pnp pair, Q10 and Q11, degenerated with R6 and R7 for an input stage. The differential output is converted to single-ended by a current mirror, Q13 and Q14; and this drives the output sink transistor, Q30, through a follower, Q19.

A clamp, Q15, is included to insure that the output sink transistor does not turn off completely. Its biasing circuitry, Q6 through Q9, is arranged such that the emitter current of Q15 is about equal to the base current of Q19 with no output load.

The control loop is stabilized with a feedforward capacitor, C1. Above 2MHz, feedback is predominantly through the capacitor. The break frequency is determined by C1 and R7 plus the emitter resistance of Q11. The loop is made stable for capacitive and resonant loading by R23, which limits the phase lag that can be induced at the emitter of Q29.

A resistor, R10, has been added to improve the negative slew response. With a large negative transient, Q29 will cut off. When this happens, R10 pulls stored charge from Q28 and provides enough voltage swing to get Q30 from its clamp level into conduction.

Start-up biasing is done with a collector FET, Q4. Once in operation, the collector current of Q6 is added to the drain current of Q4 to bias Q5. These currents plus the current through Q9 and Q10 flow through Q12 to set the output quiescent current (along with R10).

follower boost

The boost circuit in figure 3 reduces the buffer standby current by at least a factor of three while improving performance. It does this by increasing the effective current gain of Q29 so that the current source current, I_{C23}, can be drastically cut. Secondly, it can give under 0.5Ω follower output resistance at less than 3mA bias, something that normally takes over 40mA. Hard as it may be to believe, the boost does not degrade the high frequency response of the final design.

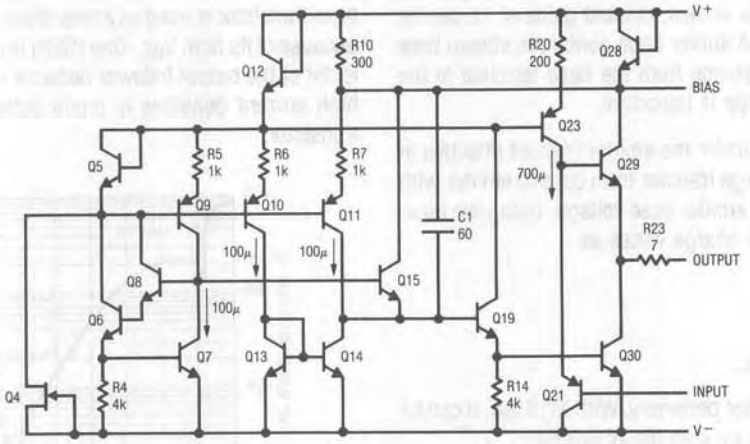


figure 2. Implementation of the buffer in figure 1. Simple op amp uses common base pnp input transistors (Q10 and Q11). Control loop is stabilized with feedforward capacitor (C1); and clamp (Q15) keeps Q30 from turning off entirely.

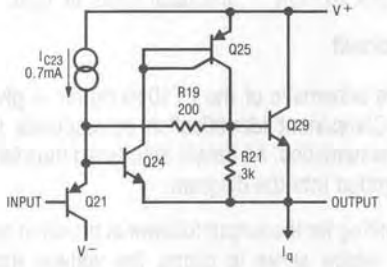


figure 3. This boost circuit raises effective current gain and transconductance of the output transistor, giving low standby current along with low output resistance.

If R19 is removed (opened), circuit operation becomes clearer. Output resistance is determined by Q24, with Q25 and Q29 providing current gain. If the current through R21 is larger than the base current of Q29, output resistance is proportionately reduced. Without R21, output resistance depends on Q29 bias, like a simple follower.

The purpose of R19 is to provide a direct ac path at high frequencies and kill unneeded gain in the boost feedback loop. If R21 is properly selected, voltage change across R19 with loading is less than 40mV, so a small value causes no problems (increasing load does cause Q21 bias current to increase). The quiescent drop across R19 is set by sizing Q24, Q25 and Q29 geometries.

charge storage pnp

At high frequencies, a lateral pnp looks like a low impedance between the base and emitter because charge stored between the emitter and subcollector (the pnp base) has a capacitive effect. The input pnp, Q21, has been designed to have more than 30 times the stored charge of a standard lateral for a given emitter current. This stored charge couples in the input to slew internal stray capacitances and drive the output follower while the boost circuitry is coming into action.

Stored charge can be maximized in a lateral pnp by using large emitter area and wide base spacing. Dimensions of several mils are practical; diffusion lengths are in the order of 6 mils with good processing.

A sketch of a charge storage pnp is shown in figure 4. With the dimensions shown, current gains of 10 can be obtained regularly. A sinker base contact is shown here because a low resistance from the base terminal to the area under the emitter is important.

The charge stored *under* the emitter is most effective in obtaining a fast charge transfer from base to emitter with minimum change of emitter base voltage. Using the notation in figure 4, this charge varies as

$$Q_E \propto \frac{W_B A_E}{S_E}$$

$$\propto (X_C - X_E)X_E,$$

where S_E is the emitter periphery. With X_C fixed, it can be shown that Q_E is maximized for $X_E = 0.5X_C$.

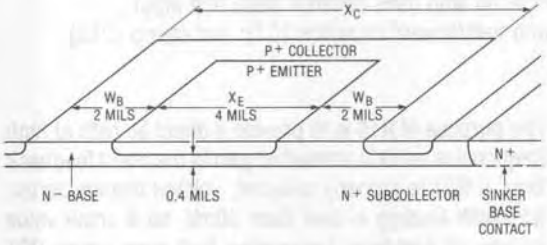


figure 4. Charge storage pnp is lateral structure with base and emitter dimensions of several mils. As above, current gains of 10 are practical.

isolation-base transistor

Transistors can be made by substituting an isolation diffusion for the normal base diffusion. Figure 5 shows the impurity profile of such a transistor. Base doping under the emitter is three orders of magnitude higher than standard transistors, and the base extends all the way to the subcollector. The measured current gains of 0.1 are not lower than might be expected.

The emitter-base voltage of an isolation-base transistor is about 120mV greater than a standard IC transistor when operating at the same emitter current. Production variations in V_{BE} are much less than standard npns, probably because net base doping is little affected by anything but the isolation doping.

As will be seen on the complete schematic, the isolation-base transistor is used as a bias diode for current sources because of its high V_{BE}. One (Q28) is also used in the collector of the output follower because the behavior at very high current densities is much better than a standard transistor.

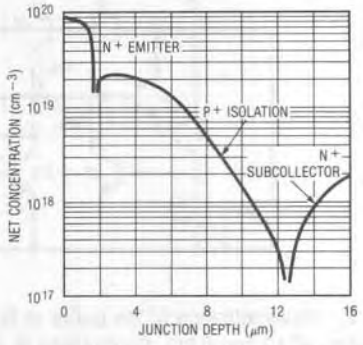


figure 5. Impurity profile of isolation-base transistor. In contrast, typical standard npn has peak base concentration of $5 \times 10^{16} cm^{-3}$ and base width of $1\mu m$.

complete circuit

A complete schematic of the LT1010 buffer is given in figure 6. Component identification corresponds to the simplified schematics. All details discussed thus far have been integrated into the diagram.

Current limiting for the output follower is provided by Q22 and Q31, which serve to clamp the voltage into the follower boost circuitry when the voltage across R22 equals a diode drop.

Negative current limit is less conventional because putting a sense resistor in the emitter of Q30 will seriously degrade negative slew under load. Instead, the sense resistor, R17, is in the collector. When the drop across it turns on Q27, this transistor supplies current directly to the sink current control amplifier, limiting sink current.

Should the output terminal rise above V^+ because of some fault condition, Q27 can saturate, breaking the current limit loop. Should this happen, Q26 (a lateral collector near Q27 base) takes over to control current by removing sink drive through Q16. This reserve current limit oscillates, but in a controlled fashion.

Clamp diodes, from the output to each supply, should be used if the output can be driven beyond the supplies by a high-current source. Unlike most ICs, the LT1010 is designed so that ordinary junction diodes are effective even when the IC is much hotter than the external diodes.

Current limit is backed up by thermal overload protection. The thermal sensor is Q1, with its base biased near 400mV. When Q1 gets hot enough to pull base drive off Q2 (about 160°C), the collector of Q2 will rise, turning on Q16 and Q20. These two transistors then shut down the buffer. Including R2 generates hysteresis to control the frequency of thermal limit oscillation.

Base drive to Q20 is limited by R15, a pinched base resistor. The value of this resistor varies as transistor h_{fe} over temperature and in production, controlling the turn off current near 2mA. An emitter into the isolation wall capacitor, C2, keeps Q20 from turning on with fast signals on its collector.

In current limit or thermal limit, excessive input-output voltage might damage internal circuitry. To avoid this, back-to-back isolation zeners, Q32 and Q33, clamp the input to the output. They are effective as long as the input current is limited to about 40mA.

Other details include the negative saturation clamp, Q17 and Q18. This clamp allows the output to saturate within 100mV of the negative supply rail without increasing supply current while recovering cleanly from saturation. The base of Q17 is connected internally into Q30 to sense voltage on the internal collector side of the saturation resistance to insure optimum operation at high currents.

When sinking large currents, the base of Q19 loads the control amplifier. This unbalances the control loop and reduces the output follower bias current. To compensate for this, the base current of Q30 is routed to the bias diode, Q12, through Q19. A small resistor, R19, aids compensation. This action raises the bias to Q23 and is responsible for increasing the input pnp bias current with sink current.

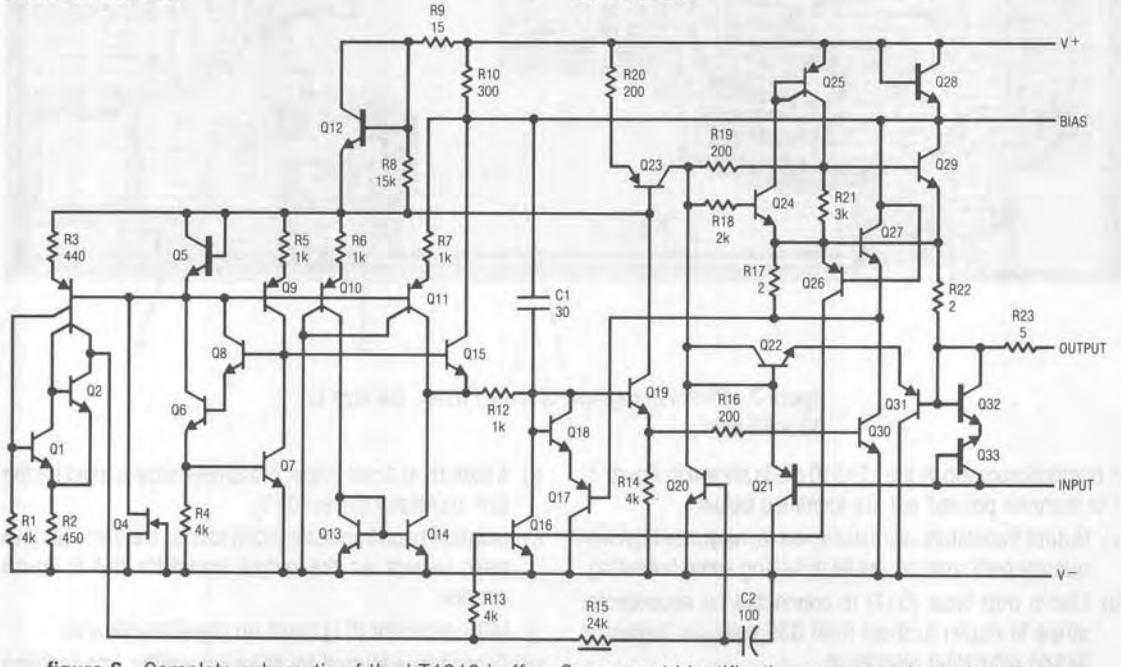


figure 6. Complete schematic of the LT1010 buffer. Component identification corresponds to simplified schematics. The isolation-base transistors are drawn with heavy base, as is the charge storage pnp. Follower drive boost has been included along with negative saturation clamp (Q17 and Q18) and protection circuitry.

Final details of the design are that the collectors of Q10 and Q11 are segmented so that only a fraction of the emitter current is sent to the current mirror, with the rest dumped to V^-. This allows the transistors to be operated at their f_T peak without requiring large C1. Lastly, R8 has been included to shape the temperature characteristics of output stage quiescent current.

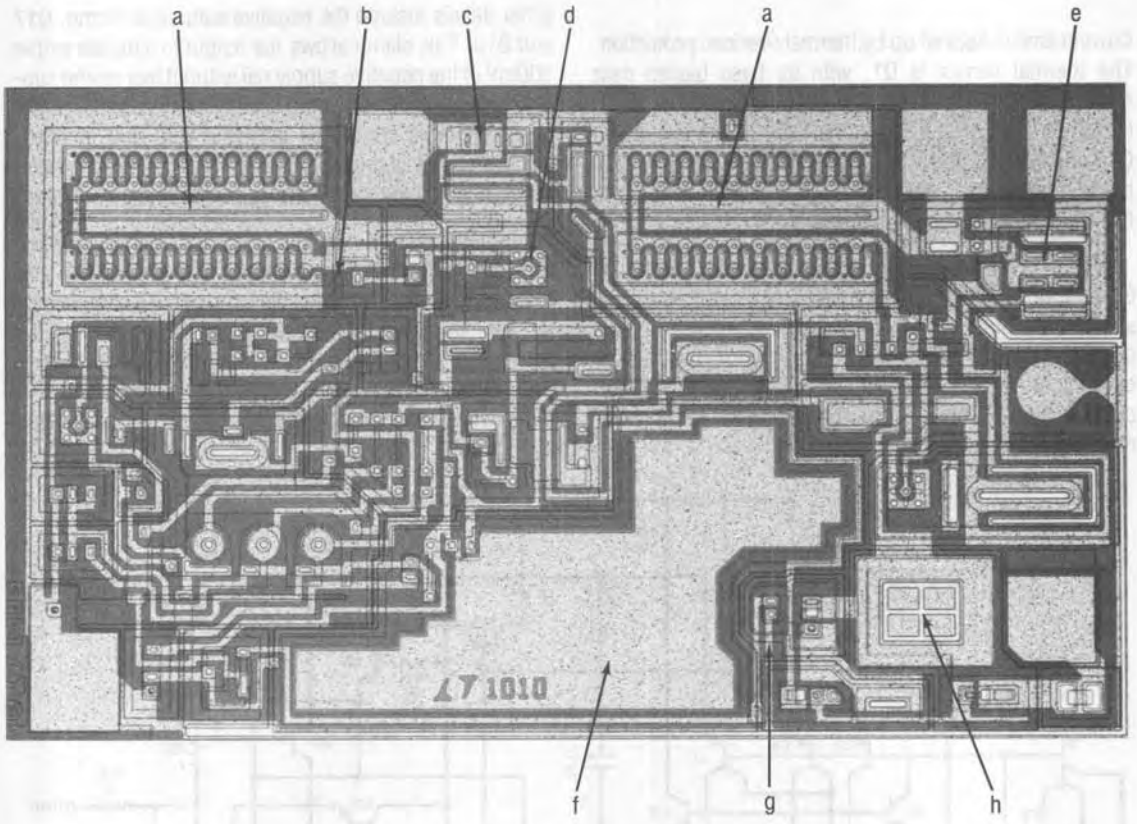


figure 7. Photomicrograph of the LT1010. Die size is 50 × 82 mils.

A photomicrograph of the LT1010 die is shown in figure 7. The features pointed out are identified below.

a) Output transistors were designed to maximize high frequency performance, while obtaining some ballasting.

b) Clamp pnp base (Q17) is connected by subcollector stripe to region furthest from Q30 collector contact to isolate saturation resistance.

c) Output resistors are in floating tub so that IC tubs are not forward biased when junction diodes clamp output below V^-.

d) A high f_T, 0.3 mil stripe, cross geometry is used for the sink transistor driver (Q19).

e) Isolation-base transistor (Q28) carries the same 500mA peak current as the output transistor but is much smaller.

f) MOS capacitor (C1) takes up considerable area.

g) Capacitance formed by diffusing emitter into isolation wall takes advantage of unused area.

h) Charge storage pnp.

buffer performance

Table I in the introduction summarizes the typical specifications of the LT1010 buffer. The IC is supplied in three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3, and the plastic TO-220. The bias terminal is not available in the TO-39 package because it has only four leads, compared to five for the other packages.

The thermal resistance for one output transistor, excluding the package, is 20°C/W because it was kept as small as possible to enhance speed. This explains the junction-to-case thermal resistance of 40°C/W for the TO-39 package and 25°C/W for the TO-3 and TO-220, again for one transistor. With ac loads, both transistors will be conducting; if the frequency is high enough, thermal resistance is reduced by 10°C/W.

The operating case temperature range for the LT1010 is −55°C to 125°C. The maximum junction temperature for the internal power transistors is 150°C. A commercial version, the LT1010C, is also available. It rated for 0°C to 100°C case temperature with a maximum junction temperature of 125°C.

The following curves describe the buffer performance in some detail. The fact that quiescent current boost (5mA–40mA) is not available on the TO-39 package should be noted.

bandwidth

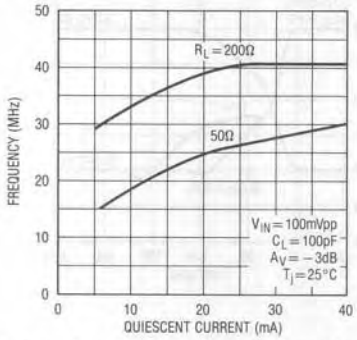


figure 8. The dependence of small signal bandwidth on load resistance and quiescent current boost is shown here. The 100pF capacitive load that is specified limits the bandwidth that can be obtained with boost and light loads.

phase delay

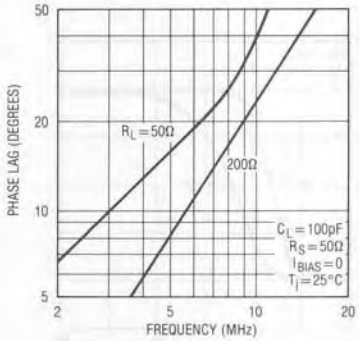


figure 9. The phase delay gives more useful information about high frequency performance than bandwidth. This is a plot of phase delay as a function of frequency with 50Ω and 100Ω loads. Capacitive loading is 100pF, and quiescent current is not boosted.

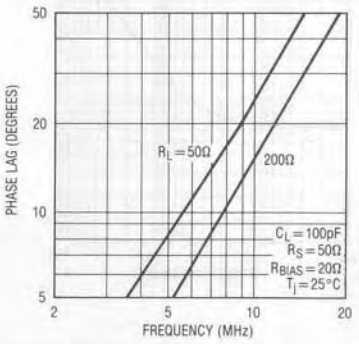


figure 10. This shows reduction in phase lag with quiescent current boosted to 40mA ($R_{BIAS} = 20\Omega$).

step response

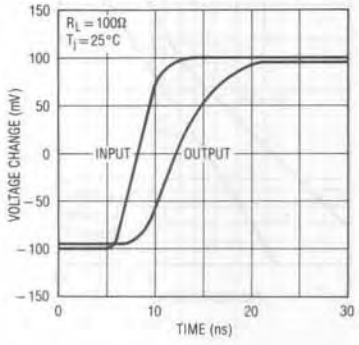


figure 11. The small signal step response with 100Ω load shows a 2ns output delay. This gives an excess phase delay of 15° at 20MHz, explaining why the −3dB bandwidth is greater than the frequency for 45° phase delay.

capacitive loading

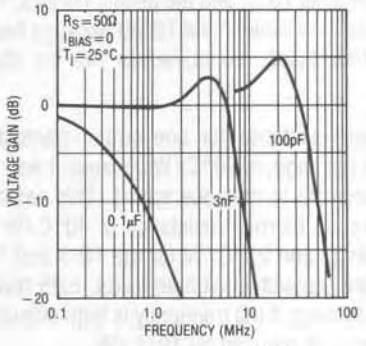


figure 13. These frequency response plots, with capacitive load only, show that nothing unusual happens as load capacitance is varied over a wide range. Minor peaking is reduced with quiescent current boost.

output impedance

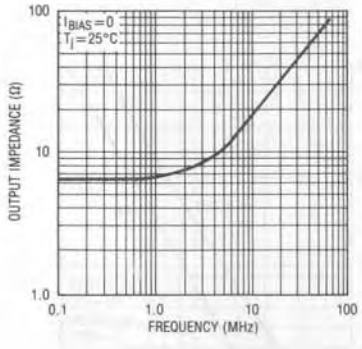


figure 12. The unloaded small signal output impedance stays down to 1MHz, indicating the frequency limit of the follower boost circuitry.

slew response

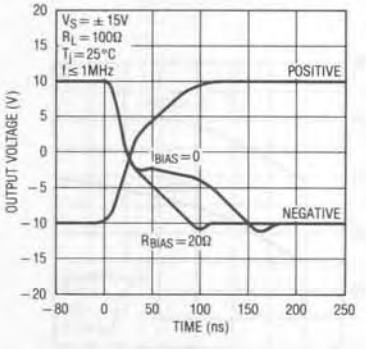


figure 14. The negative slew delay is reduced by using quiescent current boost (40mA). Positive slew is not affected by boost.

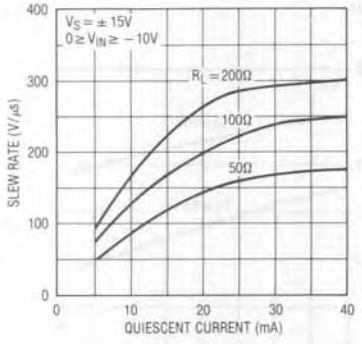


figure 15. The worst-case slew response, going from 0V to −10V, is plotted here. It is clear that substantial improvement can be made with quiescent current boost.

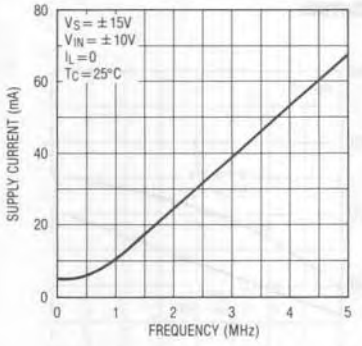


figure 17. The no load supply current increases above 1MHz under large signal conditions. This is a quiescent current boost caused by charging of internal capacitances. It does give very good power bandwidth even with load, although the excess dissipation may cause the IC to go into power limit.

input offset voltage

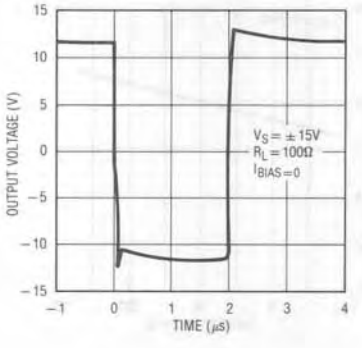


figure 16. This 500ns slew residue is caused by recovery of the follower boost circuitry. For positive outputs, the boost circuit is hit hard by the input through the charge storage pnp. For negative outputs, it is hit by the leading edge overshoot on the output. Recovery is from a positive boost overshoot in both cases.

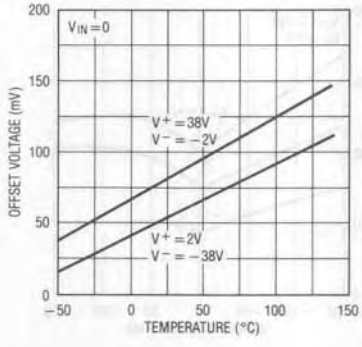


figure 18. The offset voltage is determined by matching between the output follower and the input pnp. The charge storage pnp on the input is run at high injection levels to maximize stored charge. Therefore, the high offset voltage drift shown here is no surprise. The offset voltage change with supply voltage shown in the figure is mostly positive supply sensitivity. Changing the negative supply by 35V shifts offset by 5mV.

input bias current

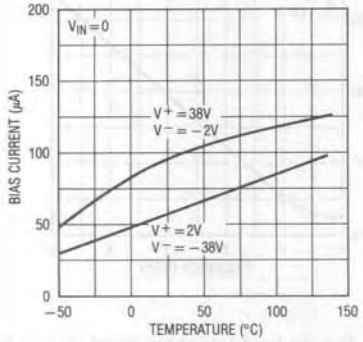


figure 19. The increase in bias current with temperature reflects the current gain characteristics of the charge storage pnp. Sensitivity of bias current to supply voltage is about three times greater on positive supply.

voltage gain

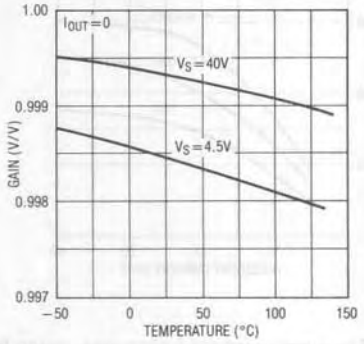


figure 21. The unloaded voltage gain is high enough to be ignored in most any application. In practice, gain will be determined by the load working against the output resistance.

output resistance

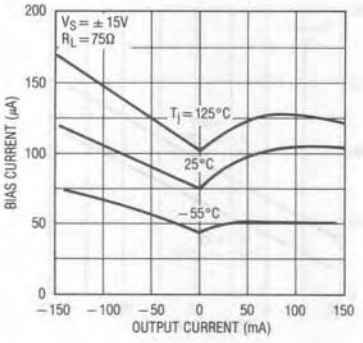


figure 20. The change in input bias current with load current is not excessive, but it shows that the follower is not designed for working with high source resistances. For positive output current, increase is caused by follower boost. For negative output, it results from sink transistor base current increasing bias to the input pnp current source.

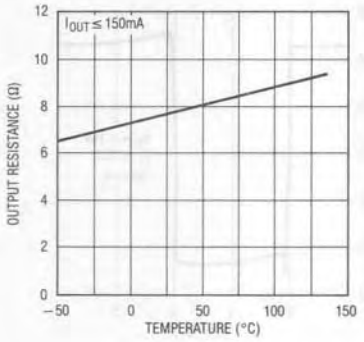


figure 22. The output resistance is essentially independent of dc output loading. The temperature sensitivity is shown here.

output noise voltage

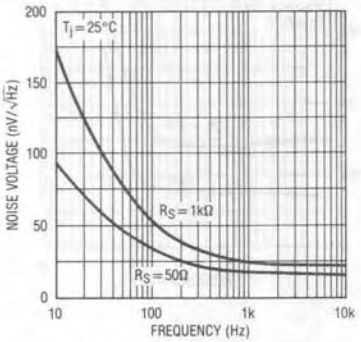


figure 23. The noise performance of a buffer is of small concern unless it is grossly bad. This plot shows that the buffer noise is low by comparison to the excess output noise of op amps.

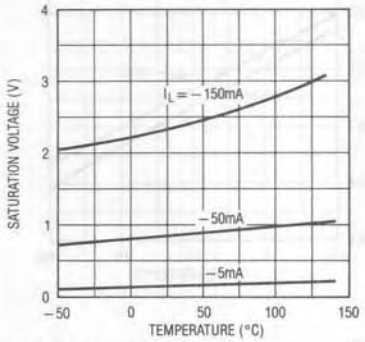


figure 25. This curve gives the negative saturation voltage. Unloaded saturation voltage is $<0.1V$, again increasing linearly with current. The saturation characteristics are negligibly affected by supply voltage and are used to determine output swing under load.

saturation voltage

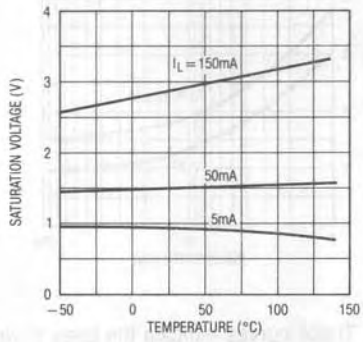


figure 24. The positive saturation voltage (referred to the positive supply) is plotted here as a function of temperature. Unloaded saturation voltage is 0.9V, with the saturation voltage increasing linearly with current to 150mA.

supply current

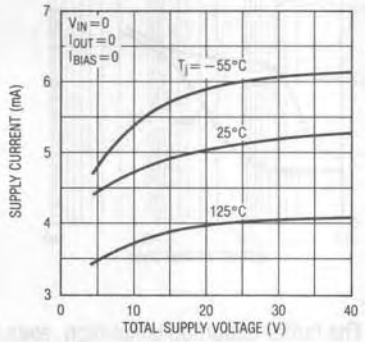


figure 26. Supply current is not greatly affected by supply voltage, as shown in this expanded-scale plot. This accounts for the 4V to 40V supply range with unchanged specifications.

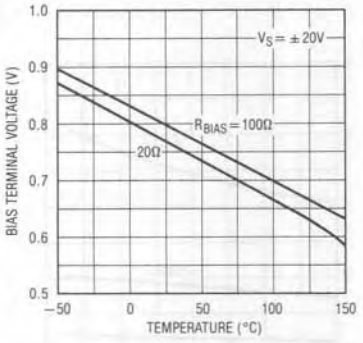


figure 27. The quiescent current boost is determined by the bias terminal voltage across an external resistor. This expanded-scale plot shows the change in bias terminal voltage with temperature. The voltage increases less than 20mV as the total supply voltage is raised from 4.5V to 40V.

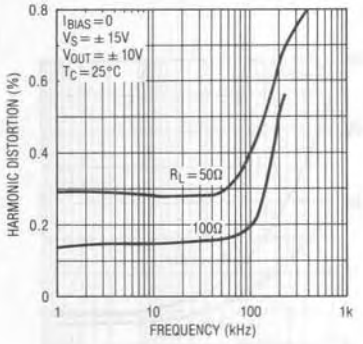


figure 29. Distortion is low to 100kHz, even without quiescent current boost. The influence of load resistance is indicated here.

total harmonic distortion

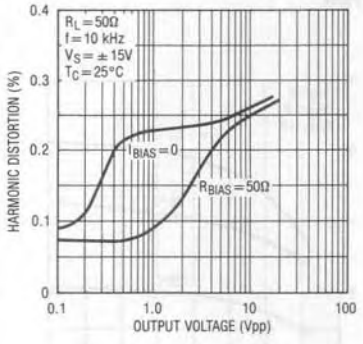


figure 28. The buffer distortion is not high, even when it is outside a feedback loop, as shown here. The reduced-distortion curve is for 20mA supply current.

maximum power

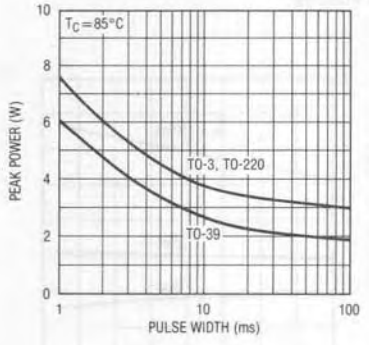


figure 30. These curves indicate the peak power capability of one output transistor for $T_C = 85°C$. With ac loading, power is divided between the two output transistors. This can reduce thermal resistance to 30°C/W for the TO-39 and 15°C/W for the TO-3, as long as the frequency is high enough that the peak rating of neither transistor is exceeded.

short circuit characteristics

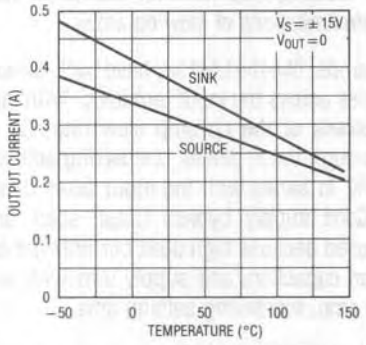


figure 31. The output short circuit current is plotted here as a function of temperature. Above 160°C it falls off sharply because of thermal limit. The peak output current is equal to the short circuit current; with capacitive loads greater than 1nF, current limiting can reduce slew rate.

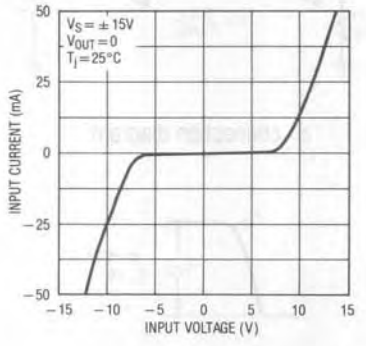


figure 32. The input characteristics, with the output shorted, are plotted here. The input is clamped to the output to protect internal circuitry. Therefore, it is necessary to externally limit input current. The output-current limit of IC op amps is adequate protection.

isolating capacitive loads

The buffered follower in figure 33a shows the recommended method of isolating capacitive loads. At lower frequencies, the buffer is within the feedback loop so that offset voltage and gain errors are negligible. At higher frequencies (above 80kHz here) op amp feedback is through C1 so that phase shift from the load capacitance acting against the buffer output impedance does not cause instability.

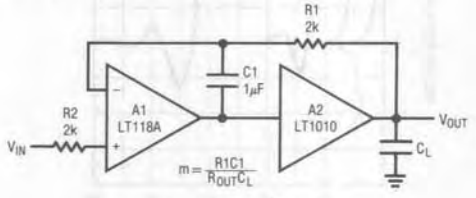
The initial step response is the same as if the buffer were outside the feedback loop; the gain error of the buffer is then corrected by the op amp with a time constant determined by R1C1. This is shown in figure 33b.

With small load capacitors, the bandwidth is determined by the slower of the two amplifiers. The op amp and the buffer in figure 33 give a bandwidth near 15MHz. This is reduced for capacitive loads greater than 1nF (determined by the output impedance of the buffer).

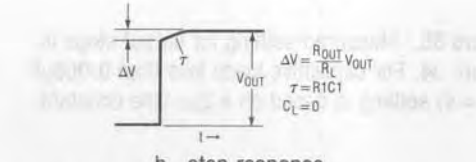
Feedback-loop stability with large capacitive loads is determined by the ratio of the feedback time constant (R1C1) to that of the buffer output resistance and load capacitance ($R_{OUT}C_L$). A stability factor, m, can be expressed as

$$m = \frac{R1C1}{R_{OUT}C_L},$$

where R_{OUT} is the buffer output resistance.



a. connection diagram



b. step response

figure 33. Capacitive loading on this buffered follower reduces bandwidth without causing ringing. Step response with no capacitive load has residue as shown here.

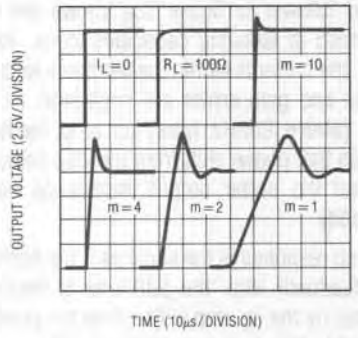


figure 34. Large signal step response (±5V) of the buffered follower in figure 33 for indicated loads.

The measured large signal step response for the circuit in figure 33a is given in figure 34 for various loads. For $m \geq 4$ ($C_L \leq 0.068\mu F$) there is overshoot but no ringing. For $m < 1$ ($C_L > 0.33\mu F$) ringing becomes pronounced.

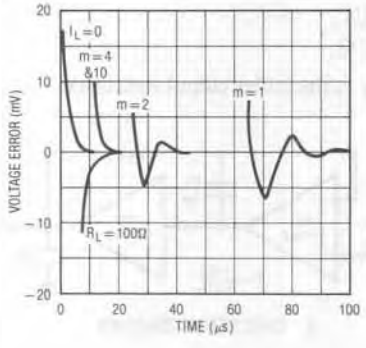


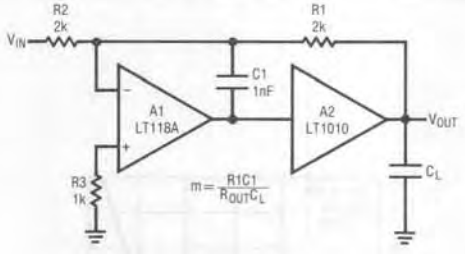
figure 35. Measured settling for output steps in figure 34. For capacitive loads less than 0.068μF (m = 4) settling is based on a 2μs time constant.

The settling time constant is determined by R1C1 for $m \geq 4$. Without capacitive loading, the initial error on the output step is smaller, so time to settle is less. The settling characteristics are shown in figure 35.

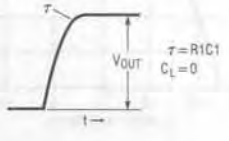
With R1C1 as shown in figure 33, any op amp with a bandwidth greater than 200kHz will give the same results on stability. Settling time, however, will be dominated by the slew rate limitations of slow op amps.

Certain op amps, like the LM118, have back-to-back protection diodes across the input terminals. With input rise times in excess of the op amp slew rate, C1 can be charged through these diodes, increasing settling time. Including R2 in series with the input takes care of the problem. Good supply bypass (22μF solid tantalum) should be used because high peak currents are required to drive load capacitors and supply transients can feed into the op amp, increasing settling time.

The same load isolation technique is shown applied to an inverting amplifier in figure 36. The response differs in that the output rise time and bandwidth are limited by R1C1. This does reduce overshoot for $m \geq 4$, as shown in figure 37. For $m < 4$, response approaches that of the follower.



a. connection diagram



b. step response

figure 36. With an inverter, bandwidth and rise time are limited by $R1C_L$. For $m \geq 4$, capacitive loading has little effect on bandwidth.

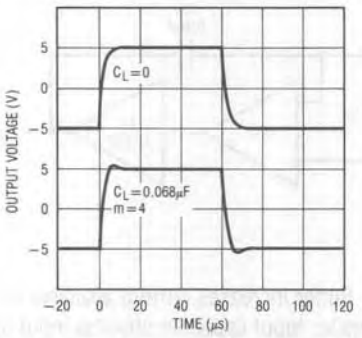
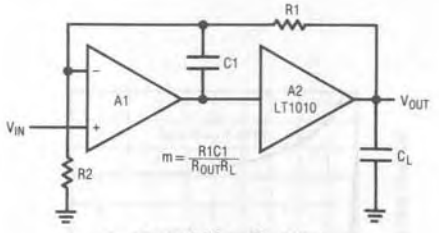


figure 37. Large signal pulse response of the inverter in figure 36.

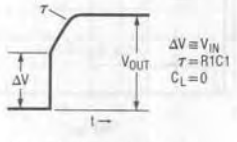
Although the small signal bandwidth is reduced by C1, considerable isolation can be obtained without reducing it below the power bandwidth. Often, bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

An alternate method of isolating capacitive loads is to buffer an inverter output with the follower shown in figure 33.

Capacitive load isolation for non-inverting amplifiers is shown in figure 38, along with the step response for small C_L. Rise time of the initial step is reduced with increasing C_L, and response approaches that of the inverter.



a. connection diagram



b. step response

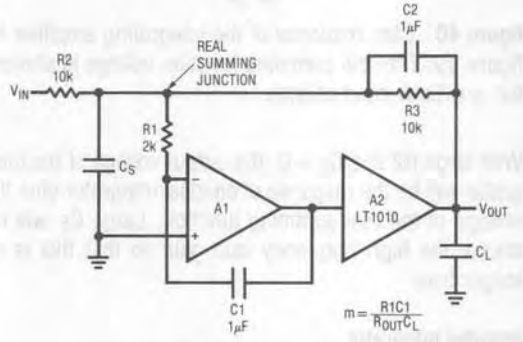
figure 38. With non-inverting amplifier, rise time of initial step decreases with increasing C_L. Stability requirements are the same as for follower and inverter.

integrators

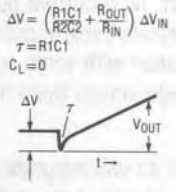
A low pass amplifier can be formed just by using large C1 with the inverter in figure 36, as long as the op amp is capable of supplying the required current to the summing junction and the increase in closed loop output impedance above the cutoff frequency is not a problem (it will never rise above the buffer output impedance).

If the integrating capacitor must be driven from the buffer output, the circuit in figure 39 can be used to provide capacitive load isolation. The method does introduce errors, as is shown in the figure.

The op amp does not respond instantly to an input step, and the input current is supplied by the buffer output. The resulting change in buffer output voltage is seen at the real summing junction and is corrected at an R1C1 time constant. As the output ramps, the voltage change across C1 generates a current through R1, shifting the real summing junction off ground.



a. connection diagram



b. step response

figure 39. Capacitive load isolation for a low pass or integrating amplifier when integrating capacitor must go to buffer output. Response given is for negative input step.

Figure 40 shows the voltage on the real summing junction for an input square wave. Both error terms are apparent in the top curve. With $C_L = 0.33\mu F$, response is reasonable. This suggests that m = 1 be used as a stability criterion for this type of circuit if the shift of real summing node voltage with output ramp is a problem. A capacitor can be used on the real summing junction to absorb current transients and reduce spiking, as shown in the lower curve.

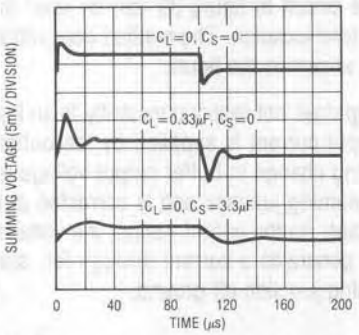


figure 40. Step response of the integrating amplifier in figure 39. The real summing junction voltage is shown for ±0.5mA input change.

With large R2 and $C_S = 0$, the output voltage of the integrator will be the response of an ideal integrator plus the voltage of the real summing junction. Large C_S will increase the high frequency loop gain so that this is no longer true.

impulse integrator

With certain sensors, like radiation detectors, the output is delivered in short, high-current bursts. Frequently, it is necessary to integrate these impulses to determine net charge. A complication with some solid-state sensors is that the peak voltage across them must be kept low to avoid error.

The circuit in figure 41 will integrate high current pulses while keeping the summing node under control. Although it increases noise gain, C_S is often required for stability and to absorb the leading edge of fast pulses. The buffer increases the peak current available to the summing node and improves stability by isolating C_f and C_S from the op amp output. Increased output drive capability is a bonus.

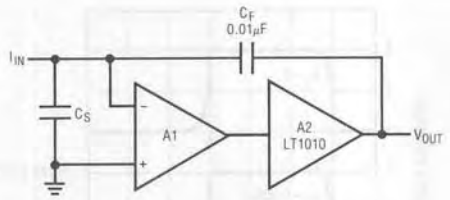


figure 41. Buffer increases current available to summing node. Input capacitor absorbs input impulses and raises loop gain.

The summing node response to a 100mA, 100ns input impulse is shown in figure 42 for three different cases. With $C_S = 0.33\mu F$, the LT118A will settle faster than the LF156 because of its higher gain-bandwidth product; but C_S cannot be made much smaller for $C_f = 0.01\mu F$. The LF156 works with $C_S = 0.02\mu F$ and settles even faster because it goes through unity gain at a frequency where the LT1010 is better able to handle $C_f = 0.01\mu F$ as a load capacitance. However, the smaller C_S does allow the summing node to get further off null during the input impulse.

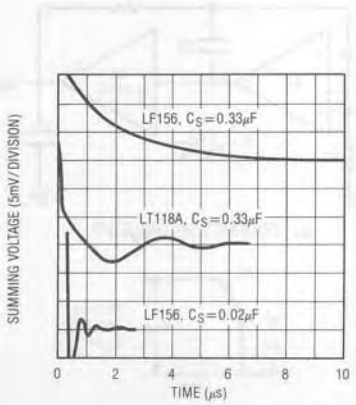


figure 42. Summing node voltage of impulse integrator in figure 41 with 100mA, 100ns input impulse and −10mA recovery.

parallel operation

Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

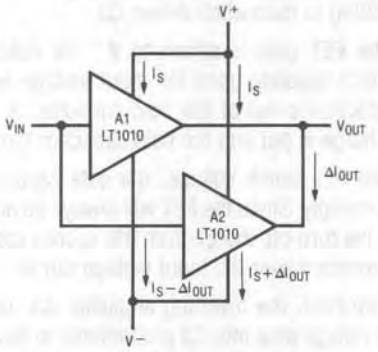


figure 43. When two buffers are paralleled, a current can flow between outputs, but total supply current is not greatly affected.

When the inputs and outputs of two buffers are connected together as shown in figure 43, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT}\ V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25°C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage above, the 25°C limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.

wideband amplifiers

Figure 44 shows the buffer inside the feedback loop of a wideband amplifier that is not unity gain stable. In this case, C1 is not used to isolate capacitive loads. Instead, it provides an optimum value of phase lead to correct for the buffer phase lag with a limited range of load capacitances.

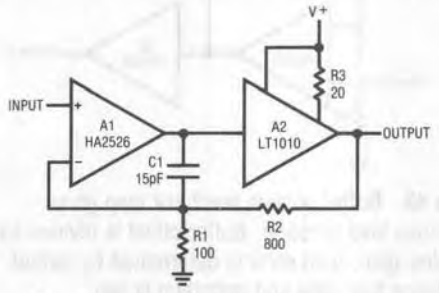


figure 44. Capacitive load isolation described earlier does not apply for amplifiers that are not unity gain stable. This 8MHz, $A_V = 9$ amplifier handles only 200pF load capacitance.

With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+. Alternately, devices in the TO-39 package can be operated in parallel.

Putting the buffer outside the feedback loop, as shown in figure 45, will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.

The 50Ω video line splitter in figure 46 puts feedback on one buffer, with others slaved. Offset and gain accuracy of slaves depends on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers, special attention should always be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground clip lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

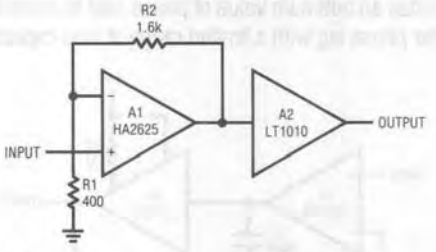


figure 45. Buffer outside feedback loop gives capacitive load isolation. Buffer offset is divided by amplifier gain, gain error is determined by output resistance tolerance and distortion is low.

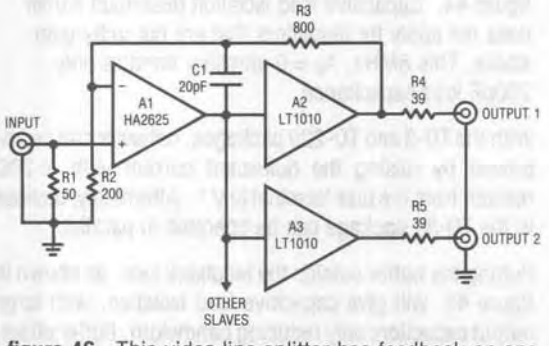


figure 46. This video line splitter has feedback on one buffer with others slaved. Offset and gain accuracy of slaves depends on matching with master.

track and hold

A 5MHz track and hold circuit is shown in figure 47. It has a power bandwidth of 400kHz with a ±10V signal swing.

The buffered input-follower drives the hold capacitor, C4, through Q1, a low resistance (<5Ω) FET switch. The positive hold command is supplied by TTL logic with Q3 level shifting to the switch driver, Q2.

When the FET gate is driven to V^- for hold, it pulls charge that depends upon the input voltage and drain-gate capacitance out of the hold capacitor. A compensating charge is put into the hold capacitor through C3.

Below the FET pinch voltage, the gate capacitance increases sharply. Since the FET will always be pinched off in hold, the turn-off charge from this excess capacitance will be constant over the input voltage range.

Going into hold, the inverting amplifier, A4, makes the positive voltage step into C3 proportional to the negative step on the switch gate, plus a constant to account for the increased capacitance below pinch-off. The step into hold is made independent of the input level with R7 and adjusted to zero with R10 (initially setting up for $V_{IN} = \pm 5V$ avoids special problems at input voltage extremes). The circuit is brought into adjustment range for a particular design with an appropriate value for C3, although a couple hundred ohms in series with C3 may be advised for larger values to insure the stability of A4.

The positive input voltage range is determined by the common mode range of the op amps. However, if the output of A4 saturates, gate-capacitance compensation will be affected.

The input voltage must be above the negative supply by at least the pinch voltage of the FET to keep it off in hold. In addition, the negative supply must be sufficient to maintain current in D2; or gate-capacitance compensation will suffer. The voltage on the emitter of Q2 can be made more negative than the op amp supplies to extend the operating range.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended.* Raising buffer quiescent current to 40mA with R3 improves frequency response.

*Overheating of the buffer causes a sharp reduction in slew rate before thermal limit is activated.

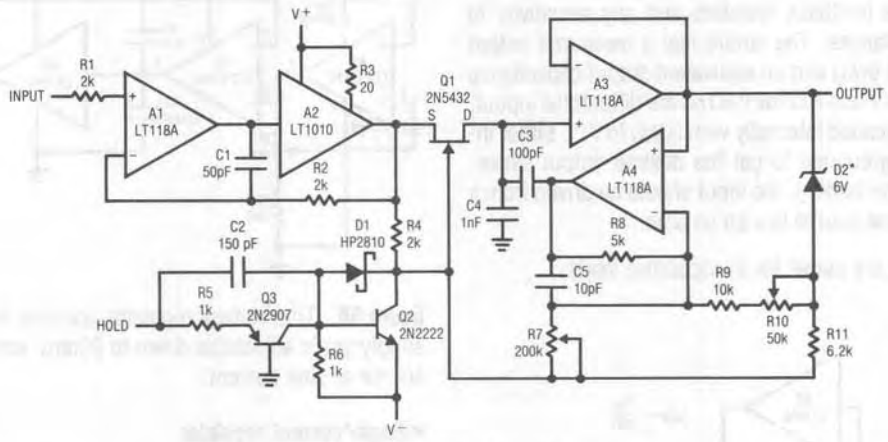


figure 47. A 5MHz track and hold. With buffer, bandwidth and slew rate is little affected by the hold capacitor. Compensation for gate capacitance of FET switch is included.

This circuit is equally useful as a fast acquisition sample and hold. A LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

Using an LT118A and lower feedback resistors would give much lower output capacitance at the expense of output resistance.

bidirectional current sources

The voltage-to-current converter in figure 48 uses the standard op amp configuration. It has differential input, so either input can be grounded for the desired output sense. Output is bidirectional.

Maximum output resistance is obtained by trimming the resistors. High frequency output characteristics will depend on the bandwidth and slew rate of the op amp, as well as stray capacitance to the op amp inputs. This ±150mA current source had a measured output resistance of 3MΩ and 48nF equivalent output capacitance.

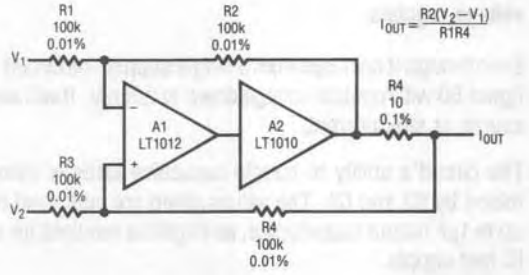


figure 48. This voltage/current converter requires excellent resistor matching or trimming to get high output resistance. Buffer increases output current and capacitive load stability with small R4.

In figure 49, an instrumentation amplifier is used to eliminate the feedback resistors and any sensitivity to stray capacitances. The circuit had a measured output resistance of 6MΩ and an equivalent output capacitance of 19nF. Pins 7 and 8 of the LM163 are differential inputs, but they are loaded internally with 50kΩ to V^-. Either input can be grounded to get the desired output sense. Because of the loading, the input should be driven from a low impedance source like an op amp.

Both circuits are stable for all capacitive loads.

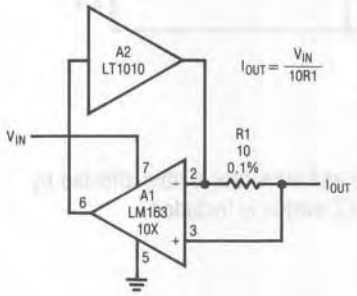


figure 49. Voltage/current converter using instrumentation amplifier does not require matched resistors.

voltage regulator

Even though it operates from a single supply, the circuit in figure 50 will regulate voltage down to 200mV. It will also source or sink current.

The circuit's ability to handle capacitive loads is determined by R3 and C1. The values given are optimized for up to 1μF output capacitance, as might be required for an IC test supply.

The purpose of C1 is to lower the drive impedance to the buffer at high frequencies because the high frequency output impedance of the LM10 runs above 1kΩ. Without C1 there could be low level oscillation at certain capacitive loads.

It is important to connect pin 4 of the LM10 and the bottom of R2 to a common ground point to avoid poor regulation because of ground loop problems.

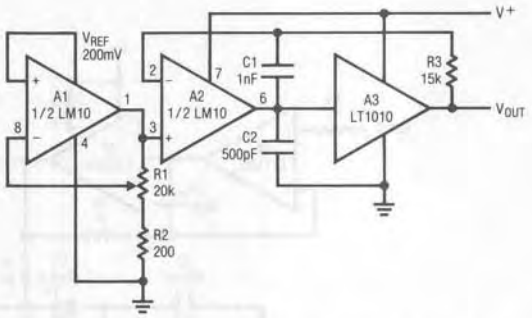


figure 50. This voltage regulator operates from a single supply yet is adjustable down to 200mV and can source or sink current.

voltage/current regulator

Figure 51 shows a fast power buffer that regulates the output voltage at V_V until the load current reaches a value programmed by V_I. For heavier loads it is a fast, precision current regulator.

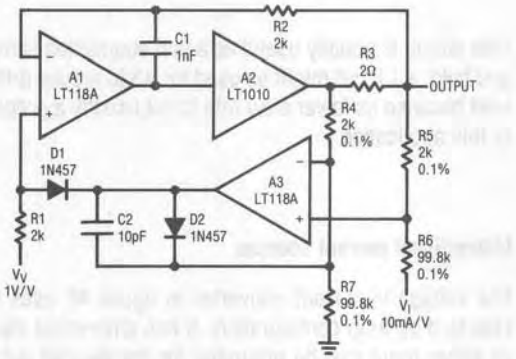


figure 51. This circuit is a power buffer with automatic transition into precision, programmable current limit. Fast, clean response into and out of current limit is a feature of the design.

With output current below the current limit, the current regulator is disconnected from the loop by D1, with D2 keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery, as well as capacitive load stability, are determined by C1. Recovery from short circuit is clean.

Bidirectional current limit can be provided by adding another op amp connected as a complement to A3. Increased output current and less sensitivity to capacitive loading are obtained by paralleling buffers.

This circuit can be used to make an operational power supply with a bandwidth up to 10MHz that is well suited to IC testing. Output impedance is low without output capacitors and current limit is fast so that it will not damage sensitive circuits. The bandwidth and slew rate are reduced to 2MHz and 15V/μs† (without paralleling) by the 0.01μF required for supply bypass on many ICs. Large output capacitors can be accommodated by switching a larger capacitor across C1.

supply splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown in figure 52 can source or sink 150mA.

The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

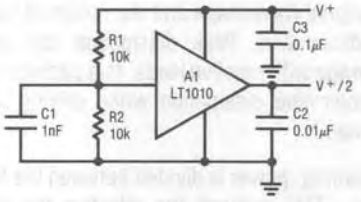


figure 52. Using the buffer to supply an artificial ground ($V^+/2$) to operate dual supply op amps and comparators from a single supply.

overload clamping

The input of a summing amplifier is at virtual ground as long as it is in the active region. With overloads this is no longer true unless the feedback is kept active.

Figure 53 shows a chopper-stabilized current-to-voltage converter. It is capable of 10pA resolution, yet is able to keep the summing node under control with overload currents to ±150mA.

During normal operation, D3 and D4 are not conducting; and R1 absorbs any leakage current from the zener clamps, D6 and D7. In overload, current is supplied to the summing node through the zener clamps rather than the scaling resistor, R2. A capacitor on the input absorbs fast transients.

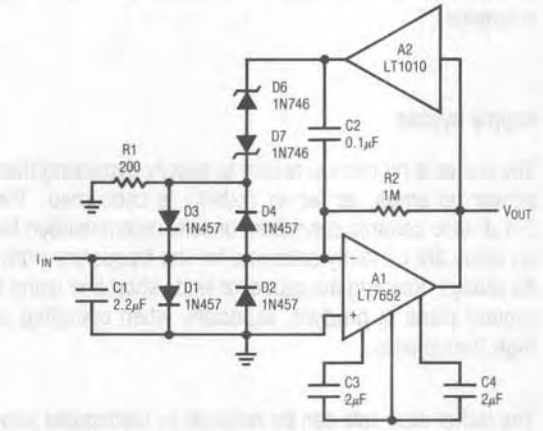


figure 53. Chopper-stabilized current/voltage converter has picoampere sensitivity, yet is capable of keeping summing node under control with 150mA input current.

† Slewing large capacitors causes high buffer dissipation.

conclusions

A new class-B output stage has been described that is particularly well suited to IC designs. It is fast and avoids the parasitic oscillation problems of the quasi-complementary output. This has been combined with the charge storage transistor, a new diode structure and a novel boost circuit to make a general-purpose buffer that combines speed, large output drive and low standby current. The buffer has been well characterized and shows few disagreeable characteristics.

The applications section has demonstrated that buffers can be quite useful in everyday analog design. They also make touchy wideband amplifiers easy to use. The availability of a low cost, high-performance IC buffer should be a stimulus to expanding upon these applications. Buffers no longer need to be considered an exotic component; they will become a standard analog design tool.

acknowledgement

Thanks are due to Felisa Velasco for special engineering assembly which was key to product development and to Guy Hoover for doing most of the experimental work presented here.

appendix

The following summarizes some design details that might otherwise be overlooked when first using the buffer. An equivalent circuit is given, and guaranteed electrical characteristics from the data sheet are listed for reference.

supply bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The 0.1μF disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/μs, using 10μF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by 10μF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

power dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is 150°C/W for the TO-39 package, 100°C/W for the TO-220 package and 60°C/W for the TO-3 package. Circulating air, a heat sink or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to 30°C/W for the TO-39 package and 15°C/W for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. Figure 30 indicates the peak dissipation capabilities of one output transistor.

overload protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

drive impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

equivalent circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown in figure A for both small and large signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. The output of A1 saturates to its supply terminals.

Loaded voltage gain can be determined from the unloaded gain, A_V, the output resistance, R_{OUT}, and the load resistance, R_L, using

$$A_{VL} = \frac{A_{VL}\,R_L}{R_{OUT} + R_L}.$$

Maximum positive output swing is given by

$$V_{OUT}^{+} = \frac{(V^{+} - V_{SOS}^{+})\,R_L}{R_{SAT} + R_L},$$

where V_{SOS} is the unloaded output saturation voltage and R_{SAT} is the output saturation resistance.

The input swing required for this output is

$$V_{IN}^{+} = V_{OUT}^{+}\left(1 + \frac{R_{OUT}}{R_L}\right) - V_{OS} + \Delta V_{OS},$$

where ΔV_{OS} is the clipping allowed in making the saturation measurements (100mV).

The negative output swing and input drive requirements are determined similarly. The values given in figure A are typicals; worst-case numbers are obtained from the data sheet reproduced on the back page.

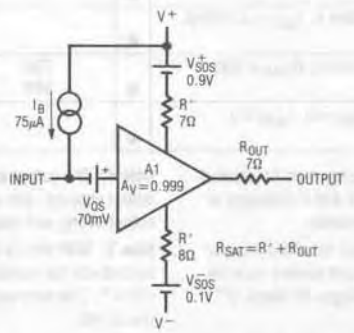
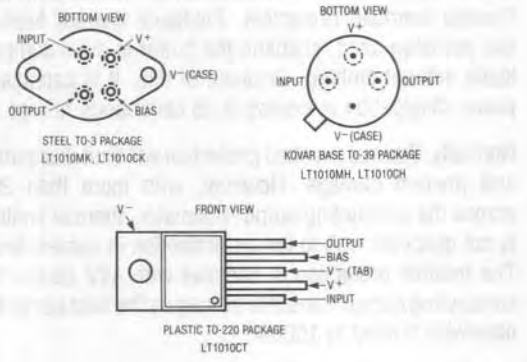


figure A. An idealized buffer, A1, as modified by this equivalent circuit describes the LT1010 at low frequencies.

absolute maximum ratings

Total Supply Voltage ..... ±22V
Continuous Output Current ..... ±150mA
Continuous Power Dissipation (Note 1)
LT1010MK 5.0W
LT1010CK 4.0W
LT1010CT 4.0W
LT1010MH 3.1W
LT1010CH 2.5W
Input Current (Note 2) ..... ±40mA
Operating Junction Temperature
LT1010M ..... −55°C to 150°C
LT1010C ..... 0°C to 125°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

connection diagrams



electrical characteristics

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)		LT1010M MIN	LT1010M MAX	LT1010C MIN	LT1010C MAX	UNITS
V_{OS}	Output Offset Voltage	Note 3		20	110	0	150	mV
			●	**−10**	**220**	**−20**	**220**	mV
		$V_S = \pm 15V$, $V_{IN} = 0$		40	90	20	100	mV
I_B	Input Bias Current	$I_{OUT} = 0$		0	150	0	250	μA
		$I_{OUT} \leq 150mA$		0	250	0	500	μA
			●	**0**	**300**	**0**	**800**	μA
A_V	Large Signal Voltage Gain		●	**0.995**	**1.00**	**0.995**	**1.00**	V/V
R_{OUT}	Output Resistance	$I_{OUT} = \pm 1mA$		6	9	5	10	Ω
		$I_{OUT} = \pm 150mA$		6	9	5	10	Ω
			●		**12**		**12**	Ω
	Slew Rate	$V_S = \pm 15V$, $V_{IN} = \pm 10V$						
		$V_{OUT} = \pm 8V$, $R_L = 100\Omega$		75		75		V/μs
V_{SOS}^+	Positive Saturation Offset	Note 4, $I_{OUT} = 0$			1.0		1.0	V
			●		**1.1**		**1.1**	V
V_{SOS}^-	Negative Saturation Offset	Note 4, $I_{OUT} = 0$			0.2		0.2	V
			●		**0.3**		**0.3**	V
R_{SAT}	Saturation Resistance	Note 4, $I_{OUT} = \pm 150mA$			18		22	Ω
			●		**24**		**28**	Ω
V_{BIAS}	Bias Terminal Voltage	Note 5, $R_{BIAS} = 20\Omega$		750	810	700	840	mV
			●	**560**	**925**	**560**	**880**	mV
I_S	Supply Current	$I_{OUT} = 0$, $I_{BIAS} = 0$			8		9	mA
			●		**9**		**10**	mA

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages or 40°C/W with the H package. See applications information.

Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V^+ or 0.5V below V^-.

Note 3: Specifications apply for $4.5V \leq V_S \leq 40V$, $V^- + 0.5V \leq V_{IN} \leq V^+ - 1.5V$ and $I_{OUT} = 0$, unless otherwise stated. Temperature range is $-55°C \leq T_j \leq 150°C$, $T_C \leq 125°C$, for the LT1010M and $0°C \leq T_j \leq 125°C$, $T_C \leq 100°C$, for the LT1010C. The ● and **boldface type** on limits denote the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V^+. The increase is equal to the bias terminal voltage divided by this resistance.