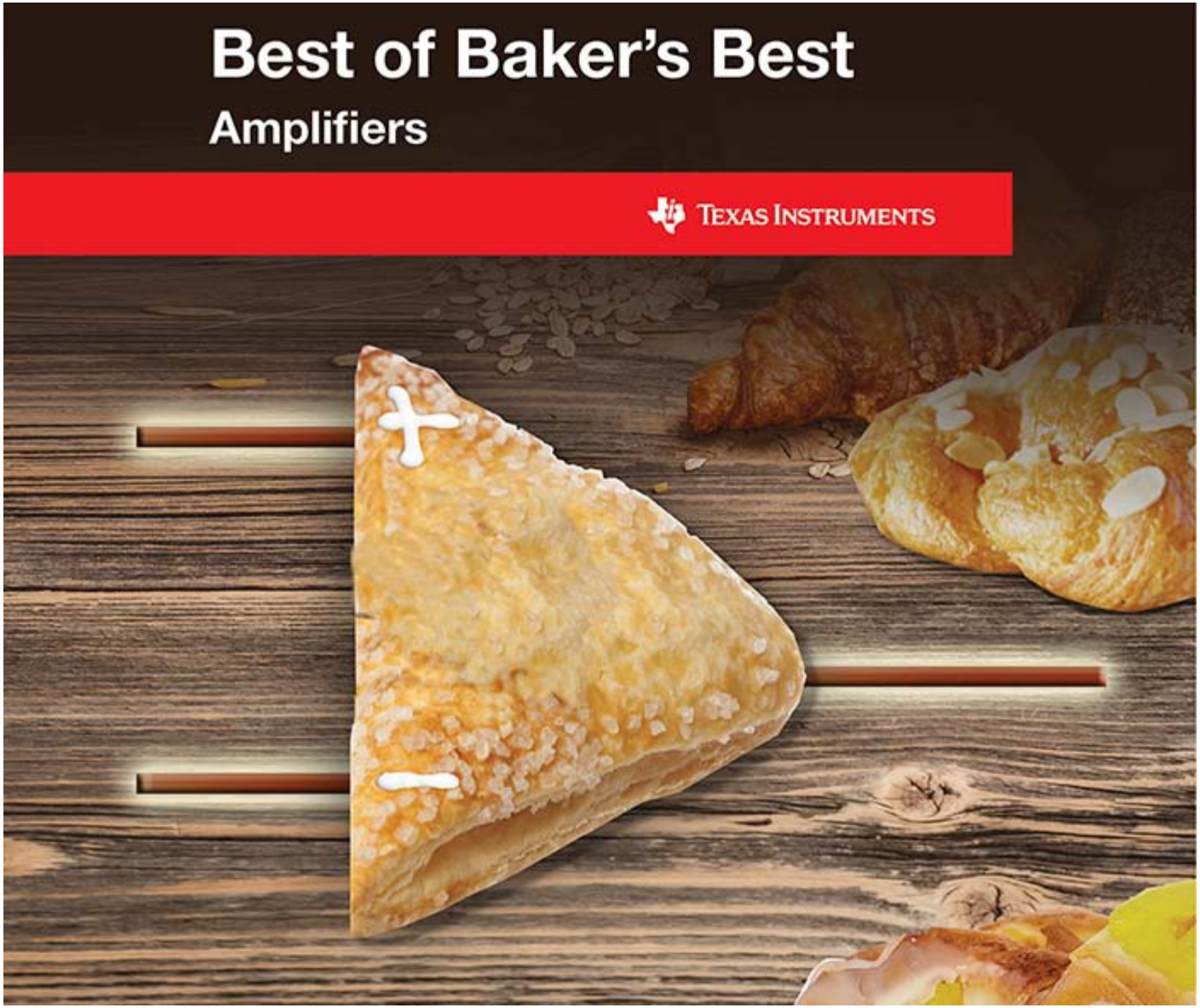
Best of Baker's Best

Amplifiers

Texas Instruments



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Introduction

The Best of Baker's Best – *Amplifiers*

Introduction by Bonnie Baker

Amplifiers have been around for a long time. These beasts were just coming alive in the 1930s - 1940s, at the hands of several individuals including Harold S. Black, George Philbrick and H. W. Bode. Since the advent of the solid state operational amplifier (op amp), enabled by the invention of silicon transistors and the integrated circuit (IC), the amplifier has increasingly become a staple for signal conditioning in most electronic systems. Given the long time span between these beginning years and the present, you would think that we have finally come to terms with understanding this five-terminal device. Furthermore, isn't there something else out there that has successfully obsoleted these devices?

Some people I have worked with are surprised when I tell them that the op amp is not dying out, but rather they are dynamic and permanent fixtures in the electronics world. This is particularly true as long as the real-world remains in the analog domain. Amplifiers, including instrumentation amplifiers (INA) and programmable gain amplifiers (PGA), are here to stay as standalone devices and as integrated functions inside complex ICs. And, to take it a step further, there is still a lot to learn about amplifiers and their appropriate placement in your application circuits.

The following excerpts from the EDN Baker's Best column represent the best of the amplifier short articles. They have been compiled for your convenience. Please enjoy your read through and let me know what you think!

Chapter 1: Operational amplifiers

When is good enough good enough?

If you are having difficulty making product-selection decisions in a consumer circuit, such as the temperature-sensor circuit in **Figure 1**, you can quickly solve this problem by choosing the absolute best performing parts for each socket. Is this statement true or false? Using this type of logic may give you a confident feeling that your circuit will work correctly the first time. However, following such logic goes only so far when you try to justify the cost-versus-performance factors of the products you are using.

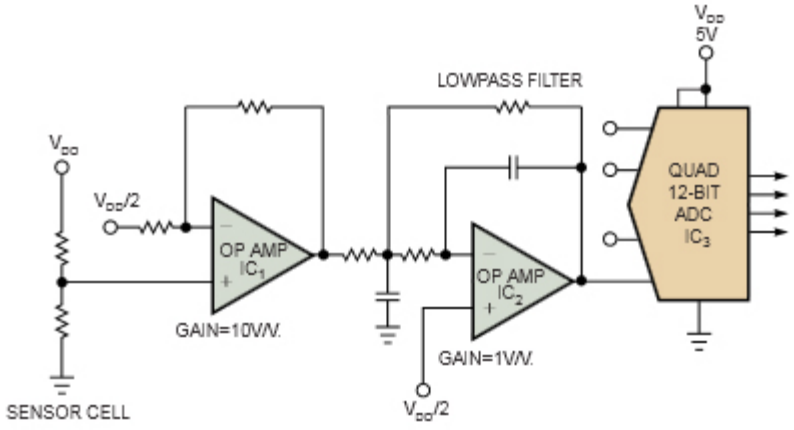

Figure 1 In this typical 12-bit temperature-sensing circuit for consumer applications, the gain of IC_1 is 10V/V, and the gain of IC_2 is 1V/V.

In **Figure 1**, note that a 12-bit converter is at the end of the signal chain. So, are the highest performance analog products in front of the ADC appropriate? How do you determine which products are good enough for your system? Avoiding production-floor notifications or field failures may be your definition of "good enough."

Instead of choosing the best products, you can use the RSS (root-sum-square) algebraic approach. One criterion is to keep the signal within the dynamic range of the full-scale range of the ADC. The product characteristics that influence the extent of the dynamic range are the system's cumulative offset and gain errors.

As an example, assume that the maximum offset error of IC_1 and IC_2 is 0.5 mV. The offset error of the ADC is ±1 LSB or ±1.22 mV. (The full-scale range of the ADC is 5V.) The gain error of both the sensor cell and the IC_1 amplifier configuration depends on the ±1% maximum resistor tolerances as well as on a maximum sensor-resistor tolerance of ±2%. The ADC's contributed gain error is 0.098% or equals 4.9 mV maximum at full scale.

To determine the dynamic-range limitations of the circuit, if you combine all of these terms, you would calculate the combined RSS value of offset and gain, bringing these errors to the ADC's input. With the RSS formula, you take the square root of the sum of the squares of several terms that are statistically independent. You cannot use an RSS formula with entities that have correlated variations that are not statistically independent.

For instance, the worst-case sensor-resistive offset error would be ±94 mV×10V/V. The contribution of the amplifier-gain stage, IC_1, is ±500 µV×10, the filter-stage (IC_2) offset error is ±500 µV, and the ADC (IC_3) offset error is ±1.22 mV. The cumulative possible offset error at the ADC's input is $\sqrt{(sensor^2 + IC_1^2 + IC_2^2 + IC_3^2)}$ =940 mV. This calculation illustrates that the sensor cell contributes the most error with little impact from the amplifiers or the ADC. Using the same logic, you would use the RSS formula to determine gain-error contribution that limits the dynamic range from the four stages in this circuit.

So, during your first consumer-product-selection attempt, you can use RSS calculations. These calculations can assist you in making logical and economical product decisions. Once you take this first step, make sure you use the same evaluation technique in your manufacturing process to quantify the effects of the processes–such as solder reflow–that you impose on these devices and the end-of-life effects due to environmental exposures.

References

1. Sandler, Steven M. "A Comparison of Tolerance Analysis Methods," AEi Systems LLC, 1998.

Just use a 100Ω resistor: Understanding a rule of thumb for oscillating amplifiers

So there I was, a new hire for a leading-edge analog-electronics company. As it was my first job, I was wide-eyed and excited–confronting new problems left and right. One problem I ran into involved the stability of an amplifier circuit. In this application, a buffer-amplifier circuit, with a capacitive load, sang like a bird. Because I had a huge community of experts around me, I ran around and asked for advice. The words of wisdom that came down to me were, "Oh, put a 100Ω load resistor between the amplifier output and the load capacitor." When I asked why, the engineer said, "Just do it. *Trust* me; it will work."

So, I built a new circuit as suggested, and, lo and behold, the circuit still oscillated. This new circuit was still singing, but it was producing a new frequency. I returned to the engineer who gave me the first bit of great advice. His recommendation: "Change the 100Ω resistor to a 500Ω resistor," still with no explanation. It solved my problem, but, given my work load, I did not return to his suggestion for several years. Now, it has come back to haunt me. I need to know what is really going on!

What I did not understand then but understand now is that a capacitor and a resistor that hang on the output of an amplifier change the amplifier's open-loop-gain curve. The combination of the load capacitor, C_L; the load resistor, R_L; and the amplifier's open-loop resistance, R_O, introduces a pole to the open-loop-gain curve, and C_L and R_L then introduce a zero to the open-loop-gain curve (**Figure 1**). Creating this pole and zero does not disrupt the amplifier's stability as long as they cancel each other out before the open-loop-gain curve crosses the closed-loop-gain curve. If the open-loop-gain and closed-loop-gain curves cross with a 40-dB/decade closure rate, the amplifier circuit will be marginally unstable or, worse yet, will oscillate.

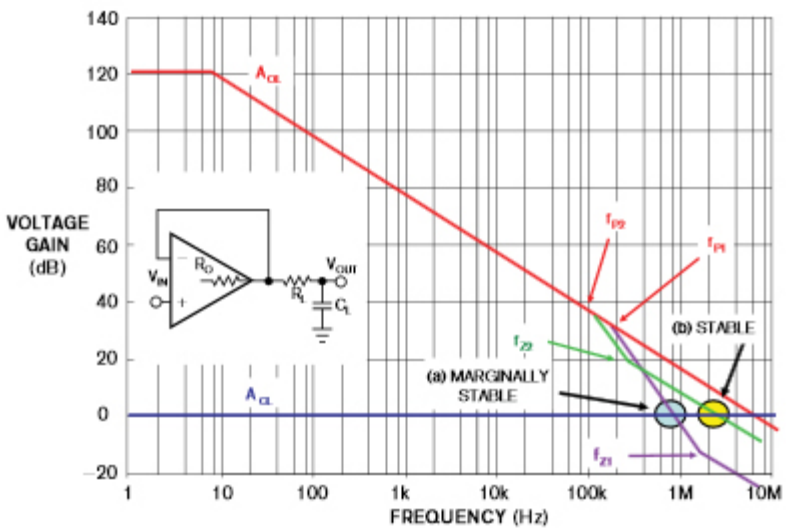

Figure 1 A buffer-amplifier circuit with a capacitive load can be marginally stable (a) or very stable (b). Keep the rate of closure between the open-loop-gain, A_{OL}, and the closed-loop-gain, A_{CL}, slope at 20 dB/decade.

You can find the pole and zero locations in this circuit in the following **equations**:

$$f_P = \frac{1}{2\pi(R_O + R_L)C_L}.$$

$$f_Z = \frac{1}{2\pi R_L C_L}.$$

What have I learned from this situation? It pays to understand why an engineer's rule of thumb works. If you comprehend the general guidelines, you will be OK. If you are not on top of the explanation, however, it will come back to bite you.

References

1. Oljaca, Miro, and Bonnie Baker, "Start with the right op amp when driving SAR ADCs," EDN, Oct 16, 2008.

Where did all that racket come from?

Since arriving in the market, CMOS single-supply amplifiers have been beneficial to single-supply-system designers worldwide. Key players affecting the THD+N (total-harmonic-distortion-plus-noise) characteristics of dual-supply amplifiers are input noise and output-stage crossover distortion. The THD+N performance of a single-supply amplifier also originates in the amplifier's input and output stages. However, the input stage's impact on THD+N complicates the nature of this specification with single-supply amplifiers.

Several types of single-supply amplifier topologies can accept input signals across the power supplies. In the complementary-differential-input-stage topology, when the amplifier's inputs are near the negative rail, the PMOS transistors are on, and the NMOS transistors are off (**Figure 1**). When the amplifier's inputs are closer to the positive rail, the NMOS transistors are on, and the PMOS transistors are off.

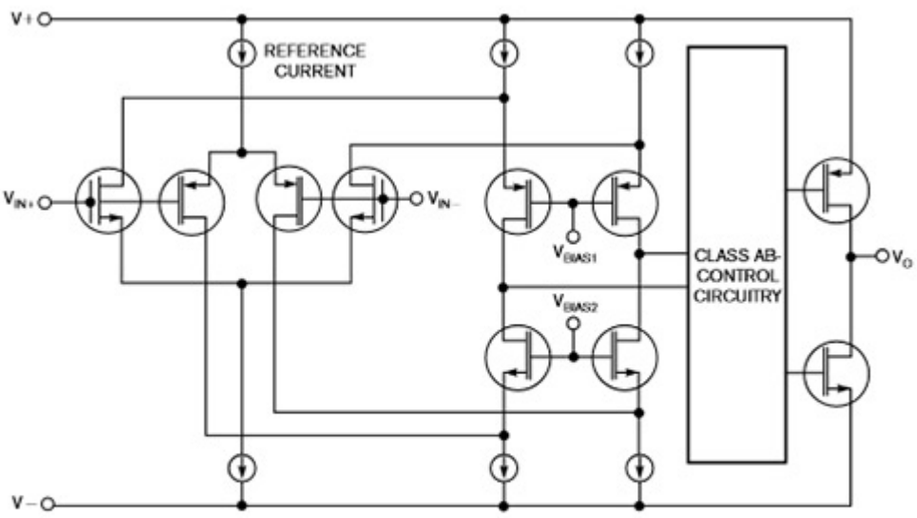

Figure 1 In the complementary-differential-input-stage topology, when the amplifier's inputs are near the negative rail, the PMOS transistors are on, and the NMOS transistors are off.

This design topology has significant variations in the amplifier's offset voltage across the common-mode input range. In the input region near ground, the PMOS transistor's offset error is dominant. In the region near the positive power supply, the NMOS-transistor pair dominates the offset error. Both pairs are on as the amplifier's inputs pass between these two regions. The end result is that the input offset voltage changes between the stages. When the PMOS and NMOS transistors are both on, the common-mode voltage region is approximately 400 mV. This crossover-distortion phenomenon affects the amplifier's THD. If you configure the complementary-input amplifier in a noninverting configuration, the input crossover distortion can affect the amplifier's THD+N performance. For instance, in **Figure 2** the THD+N is 0.0006% if you avoid using the input transition. If the THD+N tests include the amplifier's input crossover distortion, the THD+N is 0.004%. You can avoid this type of amplifier crossover distortion by usingg an inverting configuration.

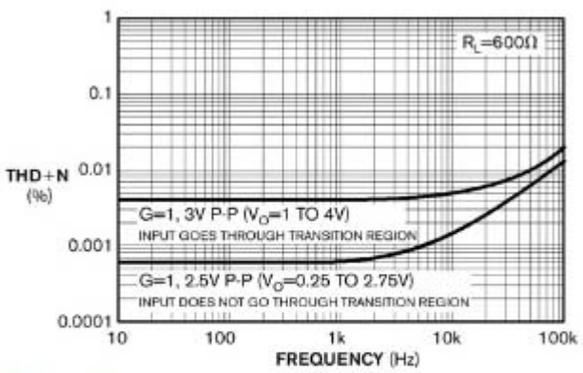

Figure 2 The THD+N is 0.0006% if you avoid using the input transition, or 0.004% if the THD+N tests include the amplifier's input crossover distortion.

Another major THD+N contributor can be the operational amplifier's output stage. The output stage of a single-supply amplifier usually has an AB topology. As the output signal sweeps from rail to rail, the output stage displays a crossover distortion similar to the input-stage crossover distortion, in that the output stage switches from transistor to transistor. Generally, a higher level of quiescent current through the output stage reduces the amplifier's THD. The amplifier's input noise is another contributor to the THD+N specification. A high level of input noise, high closed-loop gains, or both can increase the amplifier's overall THD+N level.

To optimize a complementary-input-single-supply amplifier's THD+N performance, place the amplifier in an inverting-gain configuration and keep the closed-loop gain low. If the system requires the amplifier to be configured as a noninverting buffer, an amplifier with a single-differential input stage and charge pump is a more appropriate choice.

References

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2. "OPA363, OPA2363, OPA364, OPA2364, OPA4364, 1.8V, 7MHz, 90dB CMRR, Single-Supply, Rail-to-Rail I/O Operational Amplifier," Texas Instruments, February 2003.

Is your amplifier offset way out of whack?

Have you ever spent a great deal of time selecting the perfect operational amplifier for your circuit, only to find that the offset voltage is wrong at the manufacturer's bench-specified input? What if you find that it is more than 10 times higher than specification in your application circuit? Do you send the chip in for failure analysis or just toss the chip out and have another look at your list of amplifiers? As an alternative, I suggest that you try to explain the offset error by re-examining your amplifier's specifications.

If you are using your amplifier as the key component in a transimpedance amplifier, an analog filter, a sample-and-hold circuit, an integrator, a capacitance transducer, or any other circuit with high-impedance components around your amplifier, you might find that the amplifier's input-bias current creates an offset-voltage error through the resistors in your circuit.

In the bipolar-amplifier days, the term "input-bias current" was an accurate descriptor, and it still is. A bipolar amplifier's input-bias current is the same as the base current of the NPN or PNP transistors at the input of the amplifier. The magnitude of the bipolar amplifier's input-bias current ranges from a few nanoamperes for low-power devices to hundreds of nanoamperes for higher-power devices.

The term "input-bias current" loses its meaning when you look at JFET or CMOS input amplifiers. With these types of amplifiers, the current sinking or sourcing from the amplifier's input pins is actually the leakage current from the input-ESD (electrostatic-discharge) cells (**Figure 1**). A more accurate descriptor for this current error is "input-leakage current." The magnitude of leakage current with JFET or CMOS amplifiers is less than 1 pA at 25°C. This specification is independent of the common-mode voltage and the magnitude-amplifier power. Almost all amplifiers have ESD cells for protection from an ESD event, but you will never see ESD-leakage current in bipolar amplifiers. The input-bias current swamps out the picoampere leakage current from the ESD cells.

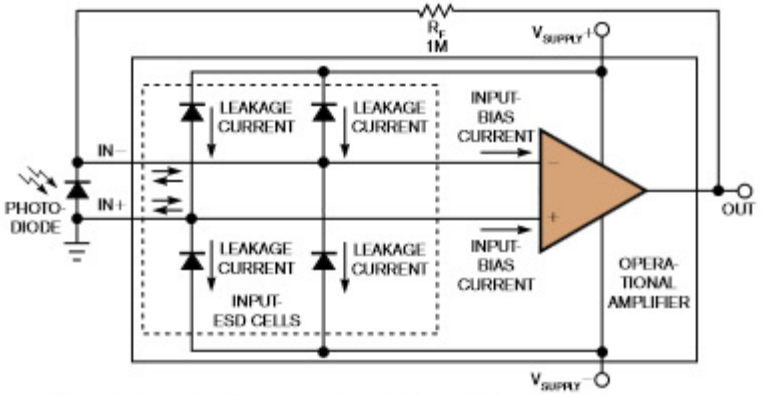


Figure 1 Input-bias or -leakage current creates a voltage drop across R_F.

Input-bias and input-leakage current can change over temperature. However, depending on the operational-amplifier design, the bipolar input-bias current can be fairly stable. The JFET and CMOS input amplifiers may not be, however. Because the leakage current is from the reverse-biased ESD diodes, the leakage current increases approximately two times per 10°C change.

In ensuring that the input-leakage current remains low with JFET and CMOS amplifiers, you must understand the impact of your PCB (printed-circuit board) on the picoampere levels of current. For instance, a small amount of dust, oil, or water molecules can increase leakage current and masquerade as input-bias current. The good news is that, if you exercise special care, you can build a PCB that will adhere to a 1-pA performance specification.

The most effective way you can reduce or minimize the effects of input-bias or input-leakage current is to check your circuit configurations. As you examine your circuits, look at the voltage characteristics of each node and make sure that you understand the impact of all of the current paths in your circuit.

A good holiday-season project

Which of the bulbs on a Christmas tree is the brightest? If you had the time and desire to answer this question, you could use a single photodiode to determine the brightness of your bulbs. Finding that brightest bulb among the many and the background light would be a laborious task, however, unless you expanded your design task to using two photodiodes. The two photodiodes let you find a light's position by monitoring the difference between their output signals.

If you use three op amps in a differential-photodiode-amp configuration, you will see greater accuracy in proximity and difference (**Figure 1**).

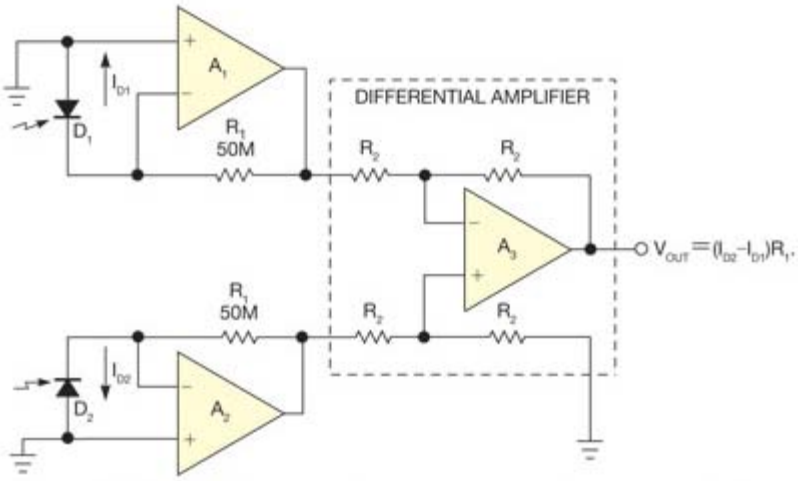


Figure 1 Differential inputs reduce common-mode errors and take the difference of the two photodiodes' signals.

The configurations of A_1 and A_2 act as traditional current-to-voltage converters or transimpedance amps. A_3 and R_2 form a difference amp, subtracting the output voltages of A_1 and A_2. In this circuit, the incident light on the photodiode causes current to flow through the diode from cathode to anode. Because the inverting input of A_1 and A_2 has high impedance, the photodiode's currents flow through the R_1 feedback resistors. The voltage at the inverting input of the amp tracks the voltage at the amp's noninverting input.

Consequently, the amp's outputs change in voltage along with the IR drop across the R_1 resistors. The output voltages of A_1 and A_2 contain both difference and common-mode signals. A_3 rejects the common-mode signal and delivers the differential-voltage signal to the circuit output at V_{OUT}.

The key performance parameters for A_1 and A_2 are input capacitance, bias current, offset, noise, and temperature drift. The goal is to select amps in which these parameters are as low as possible. A_1 and A_2 require low-inputcurrent CMOS or FET op amps.

You can implement a differential amp discretely or with an off-the-shelf product. As long as the resistors surrounding A_3 are equal, the dc-transfer function of this circuit is 1V/V.

If the resistors around A_3 are not equal, a noticeable gain error can occur between the two input signals. You can easily compensate for this type of error by replacing any of the four resistors with a potentiometer. More important, however, this type of mismatch can introduce nonlinearities in the system when the common-mode voltage of the two inputs changes. You define the common-mode voltage of the input signals as $(V_{A1OUT}+V_{A2OUT})/2$. Ideally, the differential amp rejects common-mode-voltage changes. The calculated CMR (common-mode-rejection) error due to resistor mismatches is $100\times(1+R_2/R_1)/(\%$ of mismatch error).

An equal illumination on the two photodiodes makes the output voltage 0V. D_1 and D_2 respond linearly to illumination intensity, which makes the magnitude of the output voltage a direct measurement of the difference between the direct light impinging on D_1 and D_2.

A single photodiode provides some measure of a light's intensity through the magnitude of the diode's output signal. However, background-light conditions can influence this magnitude, requiring calibrated and impractical measurement conditions. Adding a matched photodiode and monitoring the difference between the two diode outputs removes the equal offsets the two diodes produce. Background light adds only an offset to the photodiode's outputs, and the differential amp removes this effect.

References

1. Photodiode Monitoring with Op Amps, sboa035, Texas Instruments, January 1995.
2. Grame, Jerald. Photodiode Amplifiers: Op Amp Solutions. McGraw-Hill, ISBN: 0-07-024247, 2006.
3. Precision Unity Gain Differential Amplifier, SBOS145, Texas Instruments, August 1993.

Don't be fooled by your amplifier's bandwidth

As we design our SAR-converter analog circuits, we may be tempted to match the voltage-feedback amplifier's data-sheet bandwidth to the bandwidth of our analog signal source. We keep the amplifier bandwidths as low as possible, because faster amplifiers on the board potentially can produce layout headaches. These layout headaches come from putting higher-speed amplifiers in the circuit that are producing fast rise and fall times. The faster signals have the potential to produce EMI signals that other devices or traces on the board can receive, resulting in unexpected noise.

Given this scenario, it makes sense to keep the bandwidth of the circuit's amplifiers as low as possible. With a maximum signal frequency input from dc to 20 kHz, one would think that the required amplifiers would have very low unity-gain bandwidths or a gain-bandwidth product (GBWP).

On the contrary, you need higher-speed amplifiers in the circuit for two basic reasons. The primary reason is to accommodate the lost bandwidth in amplifier circuits that have a closed-loop noise gain greater than one. The other reason is to make sure the bits in your system at the end of the signal path can reliably convert the signal throughout the entire system's frequency range.

Figure 1 shows an example of how the amplifier's closed-loop gain affects the system's overall bandwidth. The GBWP of this amplifier is 20 MHz. The amplifier's closed-loop gain is 10V/V, or 20 dB. In our circuit, we already require an amplifier that has a bandwidth that is 10 times higher than our input signal. You can see this by comparing the intersect of the closed-loop gain ($f_{3\ dB}$) with the amplifier GBWP frequency (f_{GBWP}).

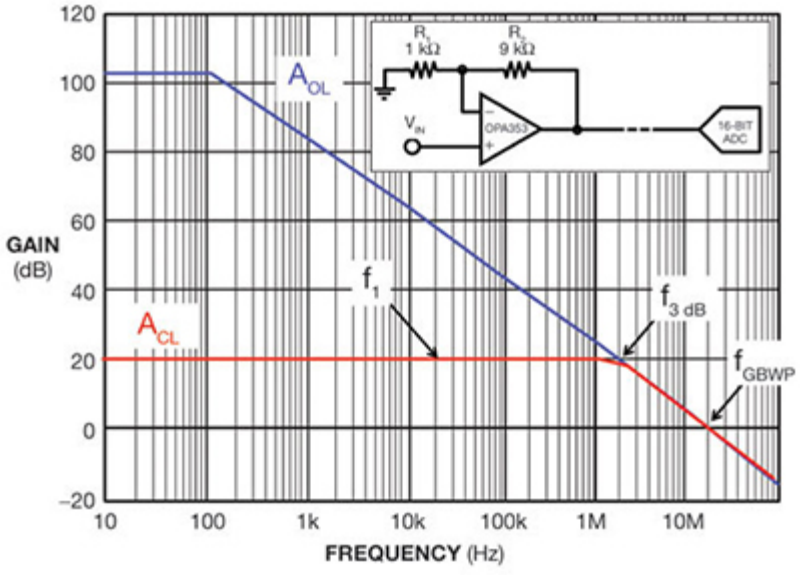


Figure 1: The system bandwidth becomes lower due to the closed-loop (A_{CL}) intercept point with the amplifier's open-loop gain (A_{OL}) and the need to accommodate bit accuracy across the entire frequency range at f_1.

The amplifier characteristics shown in **Figure 1** appear to be a perfect fit, but we are looking for the correct amplifier for a 16-bit system.

One sticky point with this circuit is that the amplifier's closed-loop gain is not equal to 20 dB all the way up to 2 MHz. In fact, the closed-loop gain at 2 MHz is 17 dB. This is down 3 dB, which is approximately 70.7% lower than the closed-loop gain, or a 29.3% increase is needed to get up to that curve.

Of course, the circuit's closed-loop gain does not instantaneously change from 20 dB to 17 dB at 2 MHz. Instead, it gradually gets closer to the closed-loop gain curve starting about a decade before 2 MHz. A 20-MHz bandwidth for an amplifier should be good enough, but let's do the math.

This intersection has a simple, first-order attenuation. The correct formula to determine the attenuation back from the 3-dB point toward 0 Hz is $f_1 = f_{3\ dB} \times \sqrt{(A_{CL\_DC}/A_{CL1})^2 - 1}$, where A_{CL1} is the target closed-loop gain, A_{CL_DC} is the closed-loop gain at dc, f_1 is the target frequency, and $f_{3\ dB}$ is the corner 3-dB frequency of this amplifier system. If you make A_{CL1} equal to 9.9988752, which produces a ~0.0112% error at the full-scale frequency, the bandwidth of the closed-loop system is approximately 100 times lower than $f_{3\ dB}$.

With our amplifier circuit, we are not so lucky. We have a 20-kHz signal that we need to increase by 10 times. At the end of the signal chain, we have a 16-bit converter. We find that a 20-kHz amplifier does not work for our circuit. With a signal gain of 10V/V, or 20 dB, the amplifier bandwidth needs to be at least 10 times higher than the signal. We also find that the amplifier bandwidth needs to be at least 100 times higher to maintain ADC integrity. This situation places our amplifier unity-gain bandwidth at 20 MHz. So much for lower- speed amplifiers.

References

1. High-Speed, Single-Supply, Rail-to-Rail OPERATIONAL AMPLIFIERS MicroAmplifier ™ Series, Texas Instruments, March 1999.

Sallen-Key lowpass-filter stopband limitations

When you design an analog, lowpass, antialiasing filter, you would expect its gain amplitude to continuously decrease beyond the filter's cutoff frequency. For the most part, this assumption is a safe one, but it's not necessarily true with the classic Sallen-Key lowpass-filter design. The Sallen-Key filter attenuates any signals in the frequency range above the cutoff frequency to a point, and then the response turns around and starts to increase in gain with frequency.

Figure 1 illustrates the behavior of three Sallen-Key lowpass filters using signal-supply amplifiers. In the top three curves, the diagram captures the open-loop gain of each amplifier as the response crosses 0 dB. During this test, the configuration for all three amplifiers is a dc noise gain of 1000V/V, or 60 dB. In the diagram, the bandwidth of op amps A, B, and C are 38 MHz, 2 MHz, and 300 kHz, respectively.

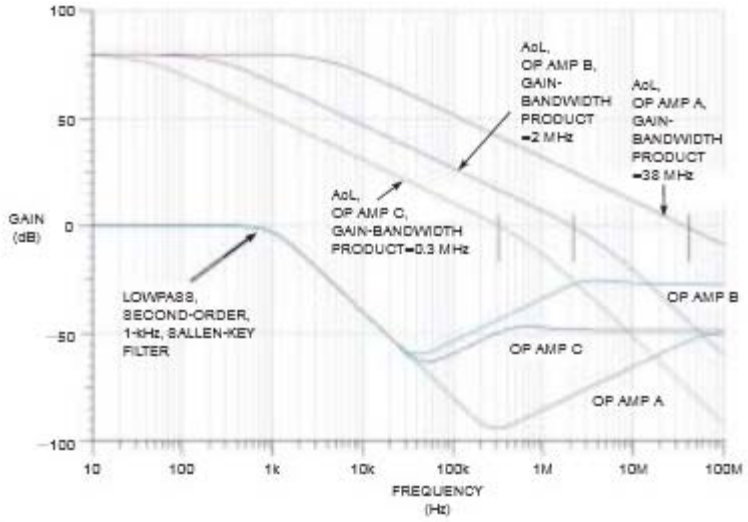


Figure 1 Note the frequency response of three Butterworth, second-order lowpass filters, along with the amplifier gain of each amplifier. The configuration for all three filters is Sallen-Key. The amplifier-gain curves start at the top of the diagram at 60 dB, and the filter curves start at 0 dB.

A second set of three curves in **Figure 1** shows the frequency response of second-order, Sallen-Key lowpass filters for each amplifier. The data indicates that the lowpass filters are performing as you would expect for a little more than a decade after the cutoff frequency of 1 kHz. Although the approximation method does not impact or correct this unexpected behavior, these filters use a Butterworth design. After the cutoff frequency, all three of the filter's responses show a slope of –40 dB/decade. You would expect this response from a second-order lowpass filter. Then, at some point, the filter gain begins to increase at a rate of 20 dB/decade. The difference in the frequency response at the point at which the three amplifiers change to a positive slope depends on the amplifier's output impedance. As the amplifier's open-loop gain decreases, its closed-loop output resistance increases. Eventually, each filter's response flattens at the 0-dB crossing frequency of the op amp's open-loop gain. It is no coincidence that the "flattening" of the filter response occurs at this crossing. As the frequency increases beyond this point, the amplifier's gain is less than 0 dB.

If you use a Sallen-Key lowpass filter, some characterization is in order. You can reduce the impact of the upward trend in the filter's response by following the offending active filter with a passive RC lowpass filter. The caveat to this action is that the following filter may interfere with the phase response of your intended filter, which may cause additional ringing in the time domain. Further, this action also creates a stage whose output is not low-impedance.

Alternative filters can solve the problem without adding an RC filter. When an inverting filter is an acceptable alternative, you can use a multiple-feedback circuit, which does not display this reversal in the gain response at higher frequencies and does not swing the input stage's common-mode voltage.

Choosing antialiasing-filter amplifiers

When you digitize an analog signal, you use a lowpass filter to prevent aliasing errors from out-of-band noise. Doing so attenuates superimposed, high-frequency noise on the analog signal before it reaches the ADC. If the noise on the input signal is more than half the sampling frequency of the converter, the magnitude of that noise stays the same, but the frequency changes as it aliases back onto your signal of interest. You cannot use a digital filter to reduce in-band noise after digitizing the signal.

Selecting the correct operational amplifier for an active lowpass-filter circuit can appear overwhelming as you read an amplifier's data sheet and view all of the specifications.

Before selecting the amplifier, however, you need to determine the filter-cutoff frequency, f_{CUT} (or –3-dB frequency). You can use filter-design programs to determine the filter's capacitor and resistor values.

Next, you should initially consider only two important specifications when selecting an amplifier for your active lowpass filter: gain-bandwidth product and slew rate. In **Figure 1**, for Q_i of less than 1, the gain-bandwidth product of the amplifier, f_{AMP}, must be at least $100\times gain\times f_{CUT}\times k_i$, where Q_i is the quality factor of the i^{th} partial filter and k_i is the ratio of the partial-filter-corner frequency to the overall-filter-corner frequency. For Q_i greater than 1, $f_{AMP}=100\times gain\times(f_{CUT}/a_i)\times\sqrt{[(Q_i^2-0.5)/(Q_i^2-0.25)]}$, where a_i is the i^{th} coefficient in the partial-filter-transfer function. The gain-bandwidth product of the operational amplifiers appears in the specification table of the respective product-data sheet.

A FEW BUTTERWORTH-DESIGN CONSTANTS

FILTER ORDER	i	a_i	$k_i=f_{CUT-i}/f_{CUT}$	Q_i
4	1	1.8478	0.719	0.54
	2	0.7654	1.390	1.31
5	1	1	1	NA
	2	1.6180	0.859	0.62
	3	0.6180	1.448	1.62

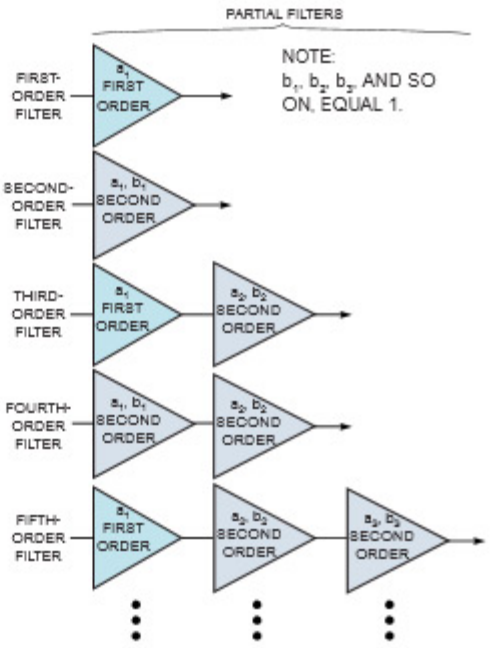


Figure 1 You build a multi-order analog filter by cascading first- and second-order filters.

You should also evaluate the effects of amplifier slew rate. Doing so ensures that your filter does not create signal distortions due to slew limitations. The slew rate depends on internal IC currents and capacitances. When you send large signals through the amplifier, internal currents charge these internal capacitors. The speed of this charging process depends on the amplifier's internal resistances, capacitances, and currents. To ensure that your active filter does not enter into a slew condition, you need to select an amplifier such that the slew rate $\geq(\pi V_{OUT\ P\text{-}P}f_{CUT})$, where $V_{OUT\ P\text{-}P}$ is the expected peak-to-peak output-voltage swing below your filter's cutoff frequency.

The most common topologies for active, second-order, lowpass filters are the noninverting Sallen-Key and the inverting multiple feedback. If you need a higher order filter, you can cascade both of these topologies.

When using the Sallen-Key circuit, input-common-mode-voltage range (V_{CMR}) and input bias current (I_B) can also affect you. In this configuration, V_{CMR} limits the range of your input signal. Additionally, the input bias current conducts through the external source resistance. The voltage drop that the input-bias-current error causes appears as an additional input-offset voltage. Also, be aware that this circuit has high-frequency feedthrough.

References

1. Bishop, J, B Trump, and RM Stitt, "FilterPro MFB and Sallen-Key Low-Pass Filter Design Program," Application Note (SBFA001A), Texas Instruments , November 2001.
2. Mancini, Ron, Op Amps for Everyone, ISBN-0-7506-7701-5, Elsevier-Newnes, April 2003.

Closer to real-world analog filters

There are two basic filter topologies that everyone recommends when they start to design their signal chain: multiple-feedback (MFB) or Sallen-Key topologies. But what are the differences and why would you choose one over the other?

The MFB topology (sometimes called *infinite gain* or *Rauch*) is often preferred because it has low sensitivity to amplifier variations, such as the open-loop gain or input range (**Figure 1**). The MFB topology creates a second-order filter. A MFB single-stage (second-order filter) provides two poles while inverting the signal. In designs where an even number of stages is required, such as a fourth- or eighth-order filter, the output polarity is the same as the input signal. A sixth-order filter consisting of three MFB stages inverts the signal three times, resulting in an inverted output after the third stage. This inversion may or may not be a concern in the application circuit, particularly if you have differential input/output stages.

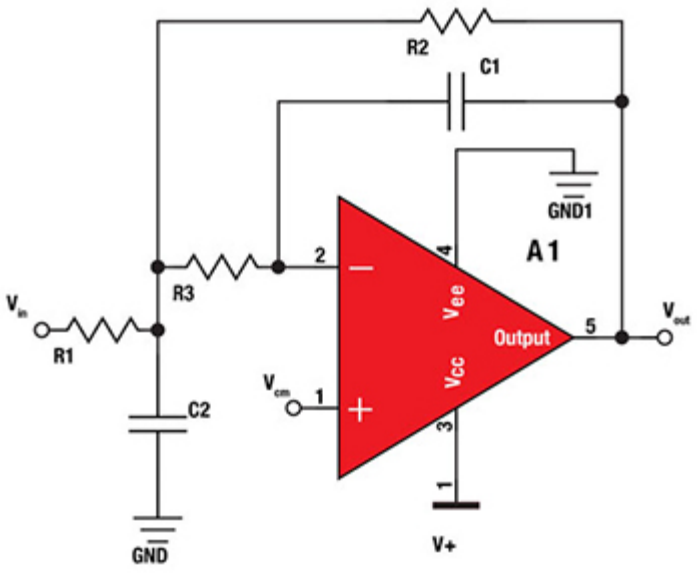


Figure 1: MFB second-order single-supply low-pass filter. The gain of this circuit is equal to $-R_2/R_1$, where $V_{CM}=V_+/2$.

In **Figure 1**, the gain circuit is negative and equal to the resistor ratio of R_2 and R_1. This arrangement allows a variety of negative gains. Generally, the MFB topology allows low sensitivity to component tolerances. The value required for C_1 in an MFB design can be quite low while the designer is trying to use reasonable resistor values. The caveat is that low capacitor values can result in significant errors due to parasitic capacitance and the input capacitance of the amplifier.

There are instances where the Sallen-Key topology is a better choice. A single, second-order Sallen-Key stage also provides two poles but is a non-inverting circuit. This may be preferable over a MFB single stage, but this is not the only potential advantage. As a rule of thumb, the Sallen-Key topology is better if:

1. gain accuracy is important, *and*
2. a unity-gain filter is needed, *and*
3. a low Q is required (for example, Q < 3)

At unity-gain, the Sallen-Key topology has excellent gain accuracy. This is because the op amp is in a unity-gain buffer configuration with a high open-loop gain. Consequently, the gain is independent of the resistors in the circuit. With the MFB topology, the R_2/R_1 resistor ratio and the resistor errors determine the gain. The unity-gain Sallen-Key topology also requires fewer components–two resistors versus three for the MFB (**Figure 2**).

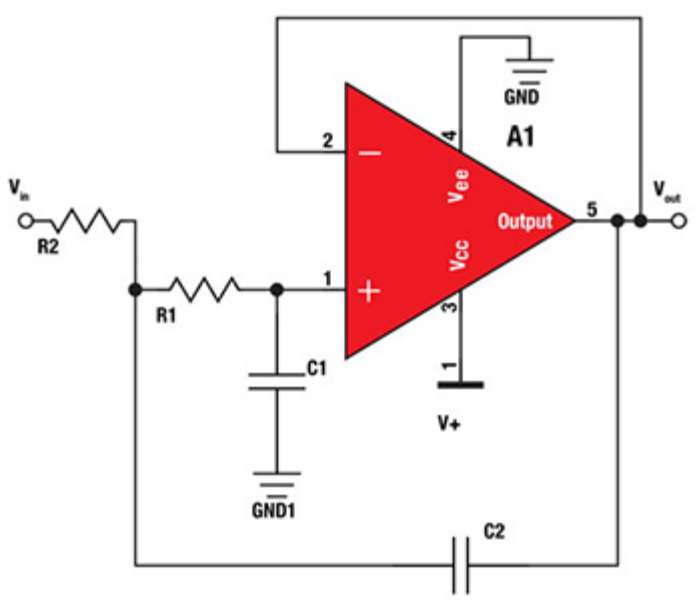


Figure 2: A Sallen-Key second-order, dual-supply, low-pass unity gain filter. The gain of this circuit is equal to 1V/V.

Your circuit also may require a low Q, the quality factor. The relationship between Q and the damping factor is Q = 1/2 ζ, where ζ is the damping factor. The higher the Q, the more easily the circuit oscillates, particularly at the 3 dB corner frequency.

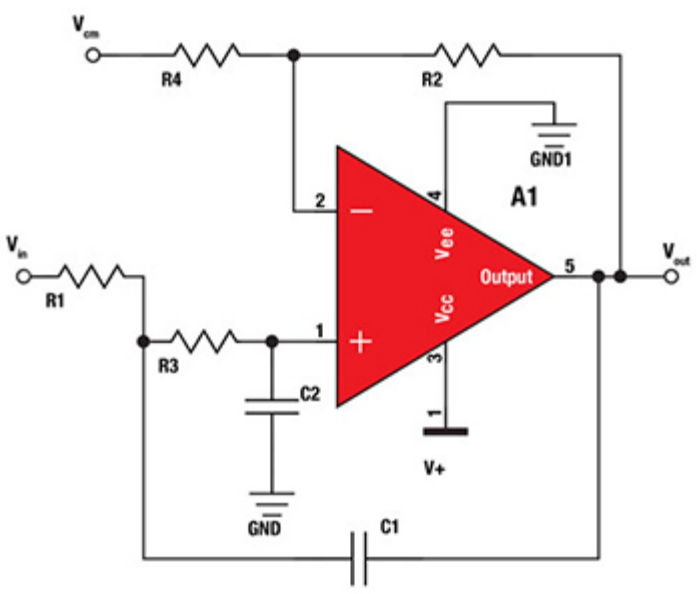


Figure 3: Sallen-Key second-order, single-supply filter. The gain of this circuit is $1+R_2/R_1$. $V_{CM}=V_+/2$.

The Sallen-Key topology may be preferable for low-Q, high-frequency filter sections.

Selecting the correct amplifier, for these circuits, presents an interesting challenge. It is not simply a matter of picking an amplifier with a gain-bandwidth-product that is 100 times higher than the filter's corner frequency. The amplifier bandwidth calculation involves variations of the amplifier's bandwidth and variations of the passive components over time, to mention a few. Sometimes amplifier manufacturers, such as Texas Instruments' WEBENCH Filter Designer Web software, provide a list of the appropriate amplifiers for the related filter. This program provides the actual amplifier suggestion along with options, if you would rather use an amplifier other than the suggested device. Filter Designer also provides SPICE simulations of the chosen filter's sine wave response, step response, and closed-loop ac response.

The WEBENCH Filter Designer program seems to have broken through some filter design barriers. All I can say is filter design has come a long way, baby.

References

1. WEBENCH Filter Designer program, Texas Instruments .

Simply an adjustable low-pass filter

A low-pass filter is the most common filter found in data acquisition systems. Typically this type of filter is used to reduce analog-to-digital converter (ADC) aliasing errors and noise outside the signal bandwidth. A signal path requires this type of dedicated filter to match the signal's requirements. If the circuit has a front-end multiplexer, it is possible to have a variety of signals that reach the ADC where each signal source has its own set of filter requirements. Consequently, a variety of different filters and corner frequency requirements may be required in the circuit prior to the multiplexer. These filters use independent operational amplifiers (op amps) in combination with fixed resistors and capacitors.

An alternative filter design solution is to have one programmable filter after the multiplexer (**Figure 1**). The obvious advantage is reduction in chip count, from multiple op amps to one single amplifier. Subsequently, the cost is lower when a single filter serves many analog inputs. You can use a dual digital potentiometer, two capacitors, and a single amplifier to configure a low-pass, second-order Butterworth response with a programmable corner frequency range of 1:100. Table 1 summarizes the digital potentiometer programmed settings.

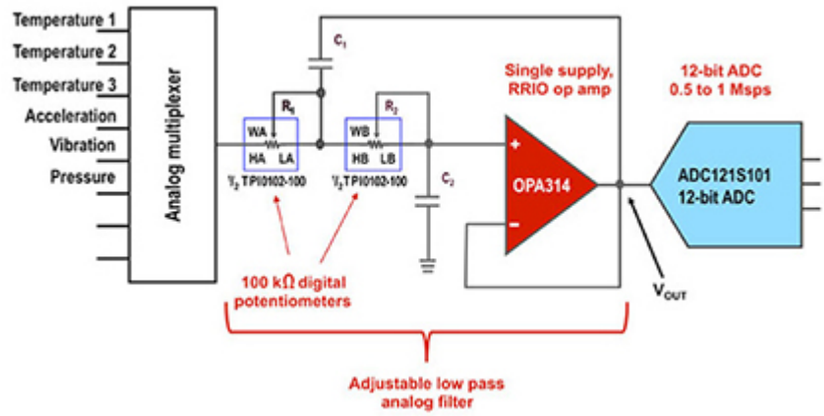


Figure 1: A second-order, analog filter using a dual digital potentiometer, two capacitors, and one operational amplifier reduces chip count.

With this circuit, it is possible to program second-order Bessel or Chebyshev filters with a programmable corner frequency range of 1:100. Additionally, you can realize a combination of Butterworth, Bessel, and Chebyshev filters with the same circuit using a 1:10 corner frequency range.

Figure 1 shows the details of a single-supply, unity gain, second-order programmable low-pass Sallen-key filter. The OPA314 is a single-supply, rail-to-rail op amp. The filter implementation requires two resistors and two capacitors. The dual TPL0102-100, a 100 kΩ 8-bit digital potentiometer, replaces the two resistors in this circuit. The capacitors are hard-wired in. A reprogramming of the dual digital potentiometer in **Figure 1** changes the filter's frequency cut-off and approximation (Butterworth, Bessel, vs. Chebyshev) of this second-order, low-pass filter.

You can calculate the appropriate resistance and capacitance with a little research, a sharp pencil, and a good eraser. An alternative to this tedious design exercise is to determine the capacitor and resistor values using TI's WEBENCH Filter Designer software.

In the input screen, enable the low-pass filter button and type in a filter bandwidth with Ao = 1 V/V, fc = 100, fs = 1000, and Asb = –35 dB. This will produce a second-order Butterworth filter. In this view, you can also select the supply requirements of Single Supply = +5 V. Then press the green button, "Start Filter Design."

The next page displays a list of filter response options that meet your requirements. Select a second-order Butterworth from the list and click "Open Design."

The Filter Designer Design Summary view (page 3) allows the user to adjust the capacitor seed value to the desired value of C1 and C2 on the left side of the screen, under the "Filter Topology Specifications" section. Change to Capacitor seed value to 15 e-9 or 15 nF, then press the "update" button. When this capacitor seed is set, the software changes the resistors in the circuit to appropriate values.

To produce the remaining filters in **Table 1**, return to page one and set the conditions for the next filter. As you do this make sure that fs is ten times higher than fc.

Cutoff Frequency, Hz	Calculated 1% R1 Value, Ohm	Closest Nominal Digital Pot, R1 Value, Ohm	Digital Pot. R1 Code, decimal	Calculated 1% R2 Value, Ohm	Closest Nominal Digital Pot, R2 Value, Ohm	Digital Pot. R2 Code
100	52.3K	52.3K	134	97.6K	97.7K	250
200	26.1K	26.2K	67	48.7K	48.8K	125
300	16.9K	16.8K	43	32.4K	32.4K	83
1k	5.23K	5.11K	13	9.76K	9.77K	25
2k	2.61K	2.7K	7	4.87K	4.69K	12
3k	1.69K	1.56K	4	3.24K	3.13K	8
10k	523	390	1	976	781	2

Table 1 shows the digital potentiometer program setting for Butterworth filter with corner frequencies ranging from 100 to 10 kHz (C1 = 33 nF, C2 = 15 nF).

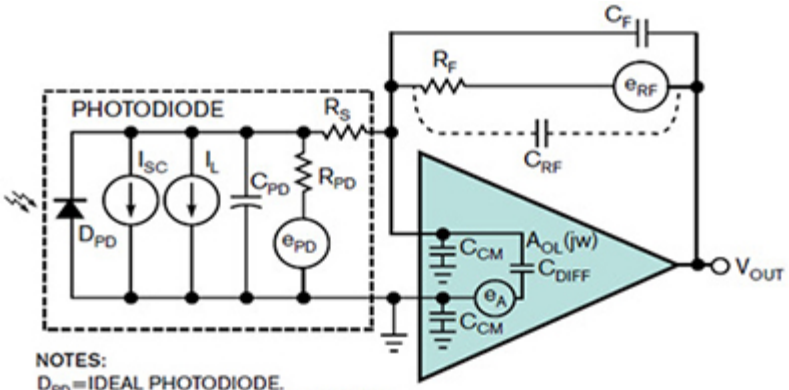
In this design, you have learned to quickly produce an adjustable analog filter. This is one technique to design a programmable anti-aliasing filter. Can you think of another way to do this? Send in your ideas and we can discuss them!

Photo-sensing circuits: The eyes of the electronic world are watching

Silicon photo sensors have been in electronic circuits since the inception of the era of silicon electronics. More than likely, scientists quickly discovered the photo-sensing characteristics of silicon in the lab, as they worked from the daylight hours into the evening. To this day, IC designers regularly cover their wafers under test to shield out extraneous light. Although the light sensitivity of silicon is an undesirable by-product of the silicon, system designers have exploited this transfer of light into electrical energy in various systems. Consequently, a wide variety of applications use silicon to sense the intensity and characteristics of light.

In these systems, a silicon sensor converts light into charge or an electrical current. These silicon sensors are the "eyes" in the electronics world that users can employ to analyze blood, search noninvasively for tumors, detect smoke, position equipment, or perform chromatography, to name a few applications. Basically, system designers understand how to convert light into a current, but the real challenge is determining how to convert the low-level currents from the photo sensor into a useful electrical representation. To further exacerbate the difficulty of the design, the required accuracy in these applications continues to increase.

The traditional design topology of the transimpedance amplifier captures this low-level signal in a hybrid approach that starts with an amplifier and a high-value resistor in the feedback loop. The circuit design uses resistance to provide a real-time, linear representation of the light source. This circuit places the photodiode across the amplifier's inverting input and ground of the operational amplifier. A resistor with a value of 100 kΩ to 10 MΩ connects the inverting input of the amplifier to the output. You then connect the noninverting input to ground (**Figure 1**). Light excitement on the photo sensor generates charge. The only path of escape for this charge is through the high-value resistor in the amplifier's feedback loop.



NOTES:
D_{PD} = IDEAL PHOTODIODE.
I_{SC} = CURRENT GENERATED BY LIGHT.
I_L = LEAKAGE CURRENT.
C_{PD} = DEVICE CAPACITANCE.
e_{PD} = DEVICE-VOLTAGE NOISE.
R_{PD} = DEVICE PARALLEL RESISTANCE.
R_S = DEVICE LEAD RESISTANCE.
C_F = FEEDBACK CAPACITOR.
R_F = FEEDBACK RESISTOR.
C_{RF} = FEEDBACK-RESISTOR PARASITIC CAPACITANCE.
e_{RF}, e_A = RESISTOR- AND AMPLIFIER-VOLTAGE NOISE.
C_{CM} = COMMON-MODE-AMPLIFIER CAPACITANCE.
C_{DIFF} = DIFFERENTIAL-AMPLIFIER CAPACITANCE.
$A_{OL}(jw)$ = AMPLIFIER OPEN-LOOP GAIN.

Figure 1 A transimpedance photo-sensing circuit is not without its design challenges.

The simplistic approach in **Figure 1** is not without its design challenges. The operational amplifier must have relatively low-picoampere input-bias currents and low input capacitance. An appropriate amplifier for this circuit would have a FET- or a CMOS-input stage with low-voltage noise and microvolt-offset specifications. In the end, the designer optimizes the stability, bandwidth, low-noise performance, and layout of this transimpedance-amplifier circuit.

The final design method is not always intuitively obvious. The photo sensor, operational amplifier, amplifier-feedback element, and these parts' parasitics combine to create quite a rat's nest of formulas for consideration. The signal after the transimpedance amplifier requires a multipole analog filter. In this manner, combining the input and filtering stages separates the signal of interest from the noise floor. A sampling ADC digitizes the signal after the analog filter.

Photo-sensing circuits have changed over the years. The first approach was purely analog, using the transimpedance amplifier and following it with a lowpass filter. From the classic transimpedance amplifier, the switched integrator has gained favor. The switched integrator was the first step toward bringing the digital portion of the circuit closer to the signal source. The migration of the photo-sensing-application product has moved on to totally integrated systems, such as the charged digitizing ADC.

Transimpedance-amplifier stability is key in light-sensing applications

A variety of precision applications sense light and convert that information into a useful digital word. At the system's front end, a preamplifier converts the photodiode's current-output signal to a usable voltage level. **Figure 1** shows the front-end circuit of this system, which comprises a photodiode, an operational amplifier, and a feedback network.

(Figure 1) The transfer function of this system is:

$$V_{OUT} = \frac{I_{SC} \times R_F}{1+1/(A_{OL}(j\omega)\times\beta)},$$

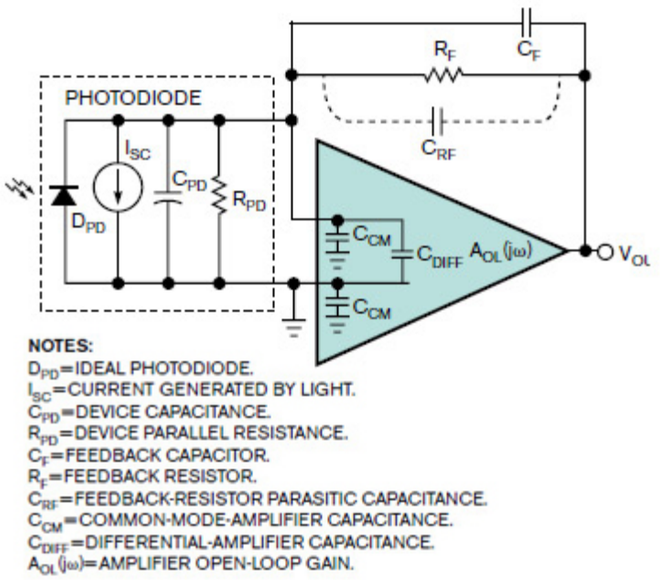


Figure 1 This transimpedance photo-sensing circuit comprises a photodiode, an operational amplifier, and a feedback network.

where $A_{OL}(j\Omega)$ is the open-loop gain of the amplifier over frequency; β is the system-feedback factor, equaling $1/(1+Z_F/Z_{IN})$; Z_{IN} is the distributed input impedance, equaling $R_{PD}||j\Omega(C_{PD}+C_{CM}+C_{DIFF})$; and Z_F is the distributed feedback impedance, equaling $R_F||j\Omega(C_{RF}+C_F)$.

A good tool for determining stability is a Bode plot. The appropriate Bode plot for this design includes the amplifier's open-loop gain and the 1/β curve. System elements determining the noise-gain frequency response are the photodiode's parasitics and the operational amplifier's input capacitance, as well as R_F, C_{RF}, and C_F in the amplifier's feedback loop.

Figure 2 shows the frequency response of the 1/β curve and the amplifier's open-loop-gain response: $f_P=1/(2\pi(R_{PD}||R_F)(C_{PD}+C_{CM}+C_{DIFF}+C_F+C_{RF}))$, and $f_Z+1/(2\pi(R_F)(C_F+C_{RF}))$. The $A_{OL}(j\Omega)$ curve intersects the 1/β curve at an interesting point. The closure rate between the two curves suggests the system's phase margin and, in turn, predicts the stability. For instance, the closure rate of the two curves is 20 dB/decade. Here, the amplifier contributes an approximately –90° phase shift, and the feedback factor contributes an approximately 0° phase shift. By adding the 1/β phase shift from the $A_{OL}(j\Omega)$ phase shift, the system's phase shift is –90°, and its margin is 90°, resulting in a stable system. If the closure rate of these two curves is 40 dB/decade, indicating a phase shift of –180° and a phase margin of 0°, the circuit will oscillate or ring with a step-function input.

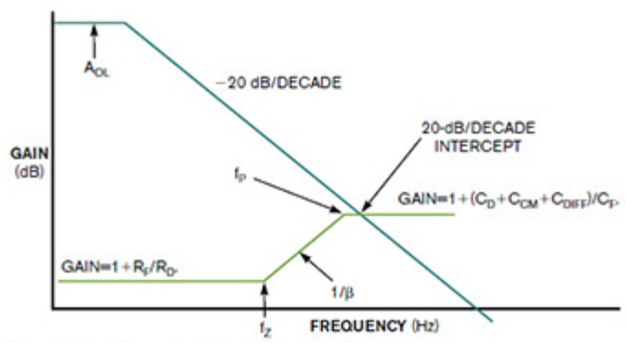


Figure 2 The closure rate between the open-loop-gain frequency response and the feedback-gain response is 20 dB/decade.

One way to correct circuit instability is to add a feedback capacitor, C_F, or to change the amplifier to have a different frequency response or different input capacitance. A conservative calculation that allows variation in amplifier bandwidth, input capacitance, and feedback-resistor value places the system's pole of 1/β at half the frequency where the two curves intersect:

$$C_F = \left[2\times\sqrt{\frac{(C_{PD}+C_{CM}+C_{DIFF})}{2\pi R_F f_{GBW}}}\right] - C_{RF},$$

where f_{GBW} is the gain-bandwidth product of the amplifier. In this design, the system's phase margin is 65°, and the step function's overshoot is 5%.

References

1. Baker, Bonnie, "Photo-sensing circuits: The eyes of the electronic world are watching," EDN, Aug 7, 2008.

Transimpedance-amplifier noise issues

How much noise is too much noise in a photodiode-preamplifier circuit? You can derive the noise performance of a transimpedance amplifier (**Figure 1a**) with calculations or by using a Spice simulation. When calculating the noise performance of the circuit, consider six regions in the frequency spectrum (**Figure 1**b) and add each region with a root-sum-square equation or the following equation:

$$V_{OUT}(NOISE_{RMS}) = \sqrt{e_1^2 + e_2^2 + e_3^2 + e_4^2 + e_5^2 + e_{RF}^2}.$$

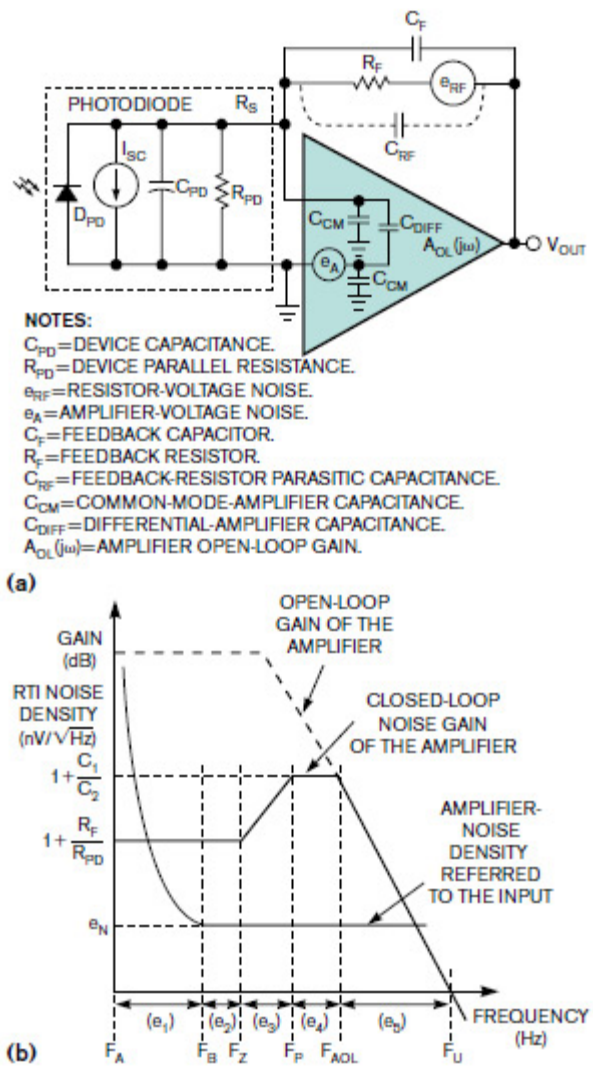


Figure 1 A typical transimpedance photo-sensing circuit (a) has five regions of overall noise response (b).

The first five regions are equal to the multiple of the areas under the closed-loop-gain and amplifier-noise-density curves. The area under the noise-density curve in the e_1, flicker-noise (1/f), region is $V_{1/f:fB-fA}=A_N\sqrt{\ln(f_B/f_A)}$, where A_N is the amplifier's input-noise-density at 1 Hz and f_B is the corner frequency where the flicker noise tapers off. For many CMOS or FET amplifiers, the flicker-noise region usually ranges from dc to 100 or 1000 Hz. A calculation proves that the contribution to noise in this low-frequency region is relatively low:

$$e_1 = (1+R_F/R_{PD}) \times A_N \times \sqrt{\ln(f_B/f_A)},$$

where R_F is the feedback resistor and R_{PD} is the device's parallel resistance.

In the e_2 region, multiply the broadband noise of the amplifier, the closed-loop dc-noise gain ($1+R_F/R_{PD}$), and the square root of the region's bandwidth. Again, the contributed noise in this region is usually relatively low because of its location in the lower frequency range.

$$e_2 = (1+R_F/R_{PD}) \times e_N \times \sqrt{f_P - f_Z}.$$

Calculate the noise contribution and the e_3 region in the same manner with $f_P=1/[2\pi(R_{PD}||R_F)(C_{PD}+C_{CM}+C_{DIFF}+C_F+C_{RF})]$ and $f_Z=1/[2\pi(R_F)(C_F+C_{RF})]$.

$$e_3 = (1+R_F/R_{PD}) \times e_N \times (1\ Hz/f_Z) \times \sqrt{f_P/3 - f_Z/3},$$

where C_{PD} is the device's capacitance and C_{DIFF} is the differential amplifier's capacitance.

The noise in regions e_4 and e_5 uses the higher-frequency gain of the closed-loop-gain curve with the value of C_1 being the parallel combination of the input capacitors, or $[C_{P-R1}||2C_{CM}||C_{DIFF}]$, and C_2 is the parallel combination of C_F and C_{RF}.

$$e_4 = (1+C_1/C_2) \times e_N \times \sqrt{f_{AOL} - f_P}.$$

$$e_5 = (1+C_1/C_2) \times e_N \times \sqrt{\pi \times (f_U - f_{AOL})/2}.$$

The sixth part of the noise equation, e_6, represents the noise contribution of the feedback resistor. The amplifier does not gain the contribution of noise from the feedback resistor:

$$e_6 = \sqrt{4 \times K \times T \times R_F \times (BW)},$$

where K is Boltzmann's constant, which is 1.38×10^{-23}; T is temperature in Kelvin; R_F is the feedback resistor in ohms; and BW is the bandwidth of interest.

When asking how much noise is too much noise in this photodiode-preamp circuit, consider that a 12-bit system operating with a 5V input range has an LSB of 1.22 mV. The LSB for a 16-bit system with the same input-voltage range is 76.29 µV. Both LSBs are peak-to-peak numbers, and the values in this column are root-mean-square values.

References

1. Baker, Bonnie, "Photo-sensing circuits: The eyes of the electronic world are watching," EDN, Aug 7, 2008.
2. "Noise Analysis of FET Transimpedance Amplifiers," SBOA060, Texas Instruments, February 1994.
3. Baker, Bonnie, "RMS and peak-to-peak noise trade-off," EDN, May 15, 2008.

Transimpedance-amplifier application: The pulse oximeter

Have you ever been in need of a second opinion when your sanity is at stake? The pulse oximeter may be able to provide that second opinion if your brain is oxygen-deprived. This condition could affect you if you are a pilot, hiking in the high altitude of a mountain range, or even undergoing surgery. The pulse oximeter is a noninvasive instrument that monitors SpO_2 (saturation of hemoglobin with oxygen) in your blood.

You measure the oxygen in the blood by alternating the on-times of a red LED with a 650-mm wavelength and an NIR (near-infrared) LED with a 940-mm wavelength, taking the ratio between the intensities from a photodiode, and comparing that ratio with an SpO_2 look-up table in the microcontroller.

The transimpedance amplifier appears in medical and laboratory instrumentation, position and proximity sensors, photographic analyzers, bar-code scanners, and even smoke detectors. In the medical field, you will primarily find transimpedance amplifiers in the CT (computed-tomography)-scanner front end and the pulse oximeter. **Figure 1** shows a simplified block diagram of a pulse oximeter.

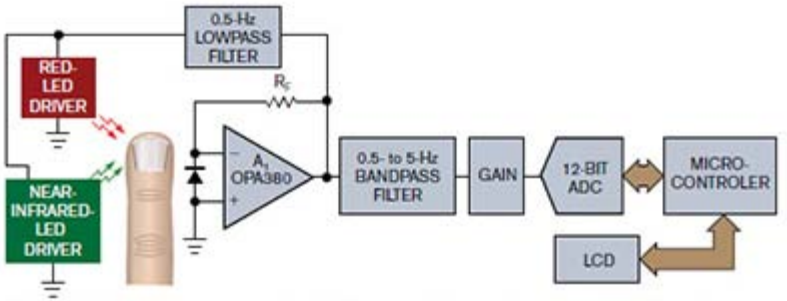


Figure 1 This pulse-oximeter circuit alternates the on-time of a red LED and a near-infrared LED to monitor oxygen saturation in the blood.

In the circuit in **Figure 1**, the red LED is on for 50 µsec, both LEDs are off for 450 µsec, the NIR LED is on for 50 µsec, and then both LEDs are off for 450 µsec. The system repeats this cycle continuously. The transimpedance amplifier, A_1, converts the photodiode current generated by the LEDs to a voltage at the output. The signal then travels through a bandpass filter and gain stage to the 12-bit ADC. The signal also travels through a lowpass filter to regulate the driver power to the LEDs. The microcontroller acquires the signals from the 12-bit ADC, computes the ratio of the red- and NIR-LED signals, and compares the results with a look-up table. The LCD shows a percentage of oxygenated hemoglobin versus nonoxygenated hemoglobin and your heart rate.

When you choose your device for the pulse-oximeter transimpedance-amplifier circuit, you need to make sure that the amplifier's input-bias current is very low or in a picoamp region at 25°C. The amplifier's input-bias current creates an output-voltage error by conducting through the high-impedance resistor, R_F, in the amplifier's feedback loop. FET- or CMOS-amplifier input devices usually meet this requirement. A second consideration is that the low-frequency voltage noise of your amplifier must be very low. When you consider the input-voltage noise of the amplifier, scrutinize the impact of the flicker noise. After the transimpedance amplifier, a bandpass filter eliminates the noise above 5 Hz. Finally, the amplifier's initial offset error and overtemperature should be in the microvolt region if you want to minimize linearity errors. It may be worthwhile to use an autozero amplifier.

A normal output for the pulse oximeter is approximately 97%±2%, ranging from 95 to 100%. The alarms on the pulse oximeter usually sound when the SpO_2 level drops below 90%. If there is a shortage of oxygen in your system, you may experience poor judgment or loss of motor function. If a pulse oximeter indicates that your oxygen levels are stable, you may want to explore other diagnostic avenues, or perhaps you just dance to the beat of a different drummer. Good luck!

References

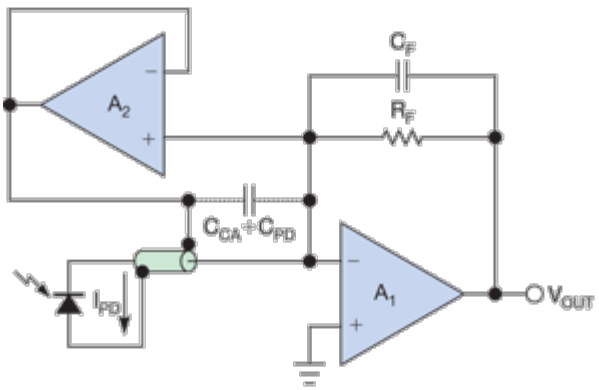
1. Medical Instruments Applications Guide, Texas Instruments, 2010.
2. Townsend, Neil, MD, "Pulse Oximetry," Medical Electronics, Michaelmas 2001.

Remote photo sensing

Photodiodes transform a basic physical occurrence, light, into an electrical form, current. Design engineers methodically convert the photodetector's current to a usable voltage, which makes the manipulation of the photodiode signal manageable. There are many ways to approach the photosensing-circuit problem, but one issue came to mind as I read the comments in the Talkback section for a recent column. A reader requested a circuit that reduces the noise impact of a photodiode with a large parasitic capacitance.

A classic photo-sensing system circuit has a photodiode, an operational amplifier, and a feedback resistor/capacitor pair at the front end. Recalling a circuit from another column, in this circuit, the photodiode, amplifier, and feedback-capacitance elements limit the bandwidth of the circuit. Yet another column details the stability of this circuit.

When sensing with a photodiode with a large parasitic capacitance or from a remote site, the input of the amplifier has a large capacitance across its input. The result of this added capacitance increases the circuit's noise gain unless you increase the amplifier's feedback capacitor. If the feedback capacitor, C_F, increases, the bandwidth of the circuit decreases.



C_{PD}: PHOTODIODE PARASITIC CAPACITANCE
C_{CA}: CABLE CAPACITANCE

Figure 1 You can use bootstrapping to eliminate diode capacitance and cable capacitance from the transimpedance-design problem.

To fix this problem, you can use a bootstrap circuit (**Figure 1**). Photodiodes with a relatively low diode capacitance do not benefit from this circuit. A unity-gain buffer, A_2, removes the cable's capacitance and the photodiode's parasitic capacitance from the input of the transimpedance amplifier, A_1.

When designing this circuit, you'll find that the type of amplifier you select for A_2 is somewhat easy. The only important performance specifications are low input capacitance, low noise, a wider bandwidth than A_1, and low output impedance.

In this design, A_2's input capacitance is the only capacitance that plays a role in the ac-transfer function of the transimpedance system. The input capacitance of the buffer replaces the summation of the input capacitance of A_1, the cable capacitance, and the parasitic capacitance of the photodiode. A good rule of thumb is to have $C_{A2}<<(C_{A1}+C_{CA}+C_{PD})$, where C_{A1} and C_{A2} represent the sum of their input differential and common-mode capacitance.

With this design, you exchange one noise problem, A_1, with another, A_2. The unity-gain buffer removes the noise effect from A_1. A good approach is to make the noise of A_2 less than or equal to that of A_1.

The difference between the input signal and the output signal in this system falls across the cable/diode capacitance. You can keep this difference low selecting A_2 with wider bandwidth than A_1 and keeping A_2's output impedance low. A_2's gain roll-off introduces an upper limit for the bandwidth improvement, making A_2's bandwidth much greater than that of A_1. This circuit requires stability optimization as you balance C_F and the input capacitance of A_2.

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Single-supply amplifier outputs don't swing rail to rail

Single-supply amplifiers do not truly swing rail to rail at the output. Near the rail, the amplifier is nonlinear. For linear operation, the output of single-supply amplifiers can come within only 50 to 300 mV of each rail (**Figure 1**).

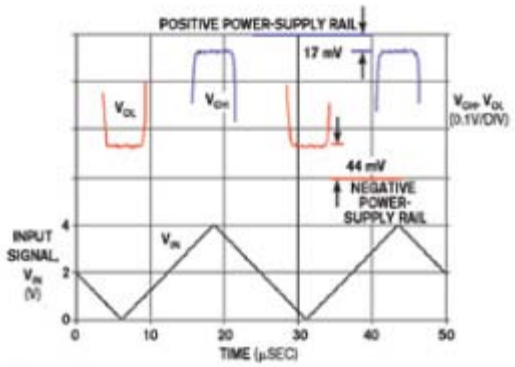

Figure 1 The lower plot illustrates the amplifier's input-voltage swing at a gain of 2V/V. The upper plot shows the amplifier's magnified output voltage.

Single-supply-amplifier, rail-to-rail-output ads can give a false sense of security. **Figure 1** shows a typical single-supply amplifier's output swing as you drive the output to the rails.

The amplifier's linearity starts to degrade long before reaching the output-swing maximums, and the amplifier output never reaches either rail.

The conditions of the dc-open-loop-gain specification define the amplifier's linear operating output range. The dc open loop gain in decibels is 20 $\log(\Delta V_{OUT}/\Delta V_{OS})$, where V_{OUT} is the output voltage and V_{OS} is the input offset voltage. When you drive the output high, V_H is the maximum voltage level at the output in the dc-open-loop-gain measurement. V_{OH} is the absolute maximum voltage level with respect to V_{DD} (drain-to-drain voltage) that the output can reach. V_L is the minimum voltage level at the output in the dc-open-loop-gain measurement, and V_{OL} is the absolute minimum voltage level that the output can reach. V_H is less than V_{OH}, and V_L is greater than V_{OL}.

From a signal-chain perspective, you can see an op amp's output limitations to swinging rail to rail when the op amp is driving an ADC. The FFT plot in **Figure 2**a shows the amplifier/ADC-combination response to a 1-kHz signal in a 5V system. The amplifier's typical closed-loop bandwidth is about 3 MHz with a typical slew rate of 2.3V/µsec. The amplifier output voltage swings from 140 mV to 4.66V. In this 5V-supply system, the headroom between the signal and rails is 140 mV. For this amplifier, the V_{OL} minimum specification is 15 mV above ground. The V_{OH} maximum specification is V_{DD}–20 mV.

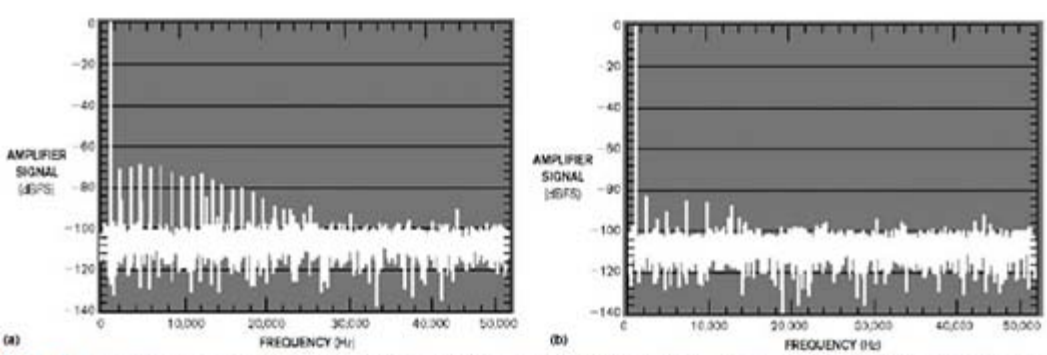

Figure 2 This 12-bit successive-approximation-register converter's maximum sampling speed is 100k samples/sec (a). Reducing the amp's output signal to 272 mV produces better results (b).

Figure 2a illustrates the nonlinearity-output-stage effects with a single-supply CMOS amplifier by showing distortion at 2, 3, and 4 kHz and so on. By reducing the amplifier's output signal to 272 mV from each rail, the data looks perfect with only the ADC distortion (**Figure 2**b).

When using a single-supply amplifier, read the fine print! Some single-supply amps have output-stage charge pumps, allowing the amplifier's output swing to go to and well beyond the power-supply rails. In every case, read your data sheet and refer to the conditions on the open-loop-gain test.

The non-negotiable single-supply operational amplifier

Fundamental analog devices that serve applications such as high-resolution delta-sigma or SAR (successive-approximation-register) converter systems are feeling the crunch from amplifiers that have difficulty with achieving good rail-to-rail input performance. The simple rail-to-rail operational amplifier must have a transistor design that spans the power supply with minimal distortion.

The trend toward designing single-supply op amps started in the 1970s with a single differential-input stage that spanned a portion of the common-mode input range. Later, designers added a second, or complementary, differential-input stage. The two stages shared, with some distortion, the rail-to-rail input operation across the complete amplifier's rail-to-rail common-mode range (**Reference 1**). Neither of these approaches produced an amplifier adequate for the high-precision systems to span the amplifier's full common-mode input range.

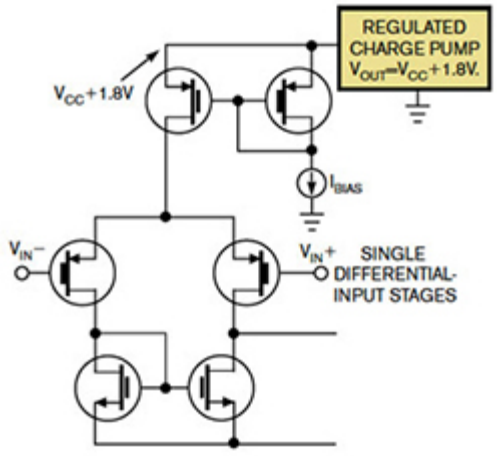

Figure 1 In this configuration, a charge pump pushes a single differential-input stage of the amplifier above the positive-power supply.

Eventually, IC designers borrowed a technology from other devices to solve this problem. They began to use the all-too-common charge pump to push a single differential-input stage of the amplifier above the positive-power supply (**Figure 1**). Amplifier designers place the switching mechanism's frequency above the amplifier's bandwidth and keep the switching noise lower than the amplifier's thermal noise floor.

The single differential-input stage with a charge pump buys you a 20- to 30-dB increase in the amplifier's CMMR (common-mode-rejection ratio). This increase has a positive effect on amplifiers in buffer configurations. You can also expect almost a tenfold decrease in the amplifier's THD (total-harmonic-distortion) performance. So, if you use an amplifier that has a charge pump in its input stage to drive high-precision SAR or delta-sigma converters, your system's performance will improve.

For example, the THD of an ADC driven by an op amp in a buffer configuration is the root-sum square of distortion contributions of the ADC and op amp. In this configuration, the system THD is:

$$THD_{SYSTEM} = 20\log\sqrt{10^{(THD_{ADC}/10)} + 10^{(THD_{OPA}/10)}},$$

where $THD_{OPA}=20\log(THD_{OPA-\%}\times 100)$ and $THD_{OPA-\%}$ is the THD specification in the operational amplifier's data sheet in units of percentage.

Using these **equations**, if an operational amplifier with a complementary input stage has a THD specification of 0.004%, with an input voltage of 4V p-p, and the 16-bit SAR ADC has a THD specification of –99 dB, the system THD is –88 dB. Alternatively, if the op amp's input stage has a charge pump with a THD specification that is 0.0004%, the system THD becomes –98 dB.

Single-supply amplifiers continue to keep pace with high-resolution converters because engineers implement innovative amplifier-circuit topologies, such as an input stage with a charge pump. The charge pump is a good stopgap; however, engineers continue to demand lower system power supplies and insist on better signal integrity.

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What does "rail to rail" input operation really mean?

A hot discussion topic with single-supply operational amplifiers is whether they are capable of rail-to-rail input or output operation. Vendors of single-supply op amps claim their amplifiers have rail-to-rail input capability, but the chip designer has to make some compromises to achieve this type of performance.

A common single-supply amplifier input topology has parallel PMOS and NMOS differential input stages, combining the advantages of those stages to achieve actual rail-to-rail input operation (**Figure 1**). When you bring V_{IN}+ toward the negative rail, the PMOS transistors are completely on, and the NMOS transistors are completely off. When you bring the input terminals to the positive rail, the NMOS transistors are in use, and the PMOS transistors are off.

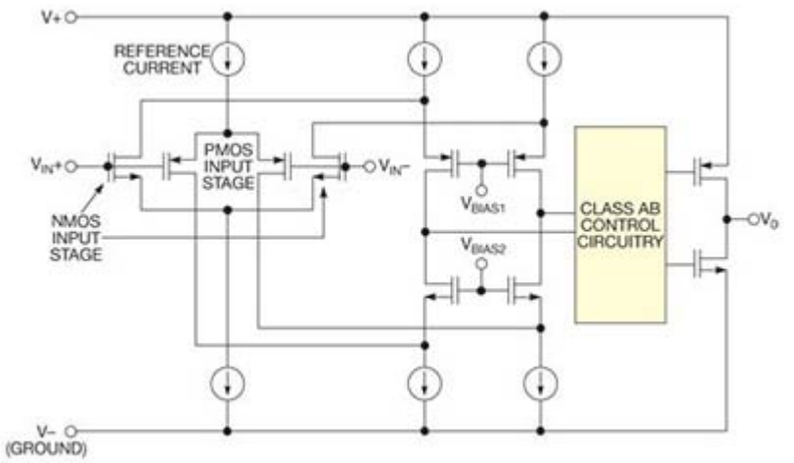

Figure 1: This composite input stage of the op amp uses PMOS and NMOS differential pairs so the input-voltage range can extend from above the positive rail to below the negative rail.

Although the precision, low-power OPA344 input stage in **Figure 1** has rail-to-rail input operation, there are performance compromises that the circuit designer must address. The design topology in **Figure 1** can have wide variations in offset voltage across the amplifier's common-mode input range. In the region near ground, the PMOS offset-error portion of the input stage is dominant. In the region near the positive power supply, the NMOS offset error dominates.

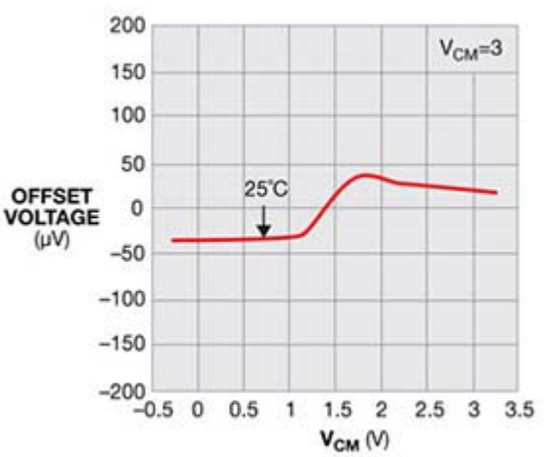

Figure 2: As the amplifier's common-mode voltage changes from ground to the positive supply, the input stage of the CMOS amplifier completely changes from its PMOS input pair to its NMOS input pair at -2V below the 3V positive supply rail.

The best way to view the input stage's behavior is to look at the offset voltage versus the common-mode input voltage (**Figure 2**). The 4.6-MHz, rail-to-rail input/output LMP7701 CMOS amplifier in **Figure 2** exhibits the offset-voltage-error crossover behavior around 1.4V. At lower common-mode input voltages, the PMOS transistors are in operation, with the NMOS transistors turned off. At approximately 1.1V, the NMOS transistors start to turn on. As the common-mode input voltage increases, the NMOS section of the circuit finally takes over, with the PMOS transistors completely off. From approximately 1.1 to 2V, both the PMOS and NMOS transistors are operating.

There are circuit-design tricks at your disposal for minimizing this input-stage crossover effect; you can read about them in "Rail-to-rail input amplifier application solutions."

Single-supply amplifier manufacturers also claim they have devices that will swing rail-to-rail on the output. With those types of amplifiers, the output cannot go all the way to the rails, but it can get close.

Next time, I'll talk about the rail-to-rail amp's output stage and its ability to achieve rail-to-rail performance.

References

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Rail-to-rail input amplifier application solutions

Many single-supply operational amplifiers are capable of rail-to-rail input operation, if they have the proper input circuitry to support this function. This article is an expansion of the blog post "What does 'rail to rail' input operation really mean?" By examining an additional input-stage topology and implementing these op amps into some common op-amp circuits, you will see what I mean.

The article discusses a composite input-stage topology for single-supply op amps. You may recall that this topology exhibited an offset-voltage, crossover distortion as the input common-mode voltage traveled across the full rail-to-rail input voltage range. Switching from one differential input stage to the other causes this distortion.

Revisiting single-supply input topologies

The CMRR (common-mode rejection ratio) specification describes changes in the amplifier's offset-voltage versus common-mode input changes. The specification conditions can subtly describe the amplifier's rail-to-rail input topology. A typical common-mode rejection specification for an amplifier with a composite input stage has two or more CMRR specifications (Table 1).

Input Voltage Range		Conditions	Min	Typ	Max	Units
Common-Mode Voltage Range	V_{CM}		-0.3		(V+) +0.3	V
Common-Mode Rejection Ratio	CMRR	$-0.3 < V_{CM} < (V+) - 1.8\ V$	80	92		dB
		$V_S = 5\ V, -0.3\ V < V_{CM} < 5.3\ V$	70	84		dB
		$V_S = 2.7\ V, -0.3\ V < V_{CM} < 3\ V$	66	80		dB

Table 1: The single-supply op-amp data sheet describes the CMRR test conditions as well as the actual specified values. These specification tables provide evidence of the characteristics of the input-stage topology, which in this case is an amplifier with a composite input stage.

In **Table 1**, the CMRR is equal to 20*log ($\Delta V_{CM}/V_{OS}$). Line 1 verifies that the amplifier has true rail-to-rail input capability. Line 2 specifies the CMRR from ground to 1.8V below the positive power-supply rail as 92 dB (typ). Note that this specification does not describe the range specified in Line 1. Line 3 specifies the CMRR across the entire input range as 70 dB (typ, V_S=5V). This disparity in specification only points out that the amplifier's input stage has a composite input topology.

There are more ways to tackle this input topology problem with the IC design. The composite input stage is one example. As a second IC-design strategy, a unique zero-crossover input topology provides superior common-mode performance over the entire input range.

In **Figure 1**, a regulated charge pump lifts the top of the differential input as well as its biasing current source to 1.8V above the power-supply voltage, V_S. This increased headroom allows for a single differential PMOS input stage to replace the composite differential input stage. A typical common-mode rejection specification for an amplifier with a charge-pump input stage has one CMRR specification. This specification encompasses the full amplifier input range.

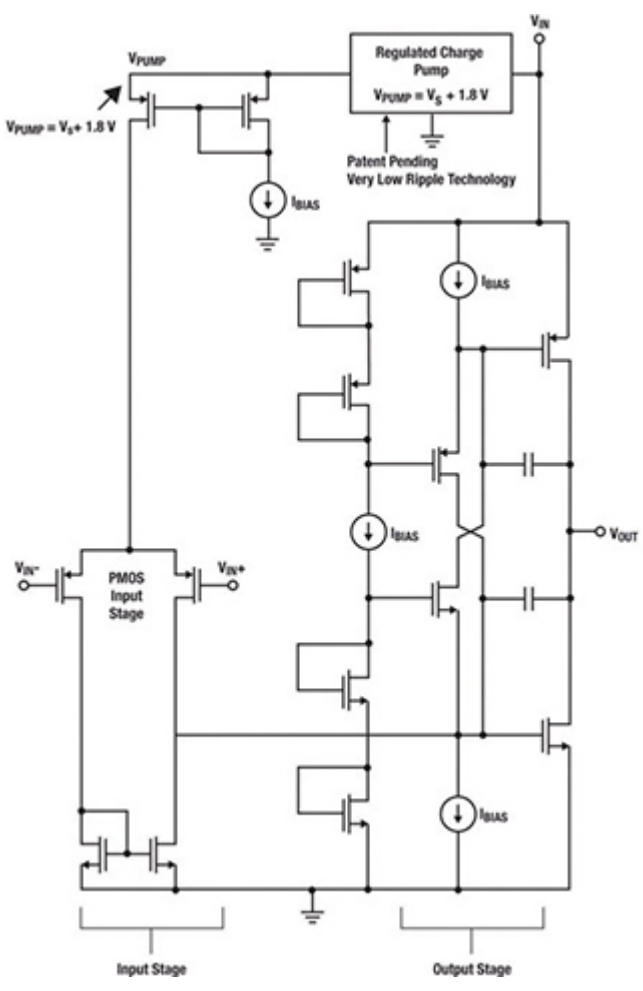

Figure 1: This single PMOS differential input stage in conjunction with a high-side charge-pump eliminates the common-mode crossover distortion found in composite input stages.

Figure 2 compares the response of the charge pump to composite amplifier inputs. The difference between these two topologies in this figure is obvious.

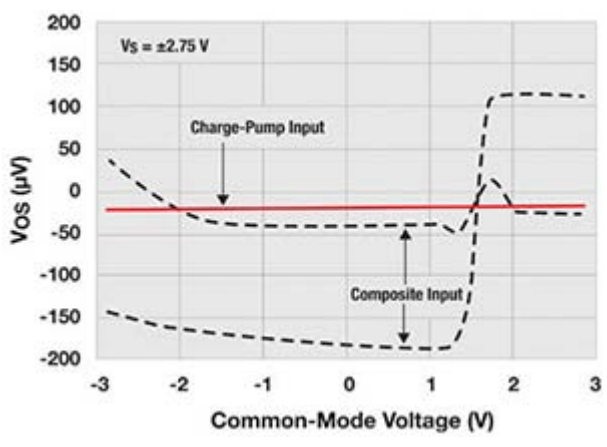

Figure 2: The op-amp offset voltage of an op amp with a charge-pump input remains constant across changes in the common-mode voltage. The offset voltage of an op amp with a composite input varies across changes in the common-mode voltage.

The op-amp topology in **Figure 1** provides superior common-mode performance over the entire input range. In fact, the input range extends at least 100 mV beyond both power-supply rails. You may think that the charge pump's output ripple voltage will become a noise problem. However, the charge-pump design can provide an output ripple voltage that is low enough so as to not produce undesirable noise or distortion at the output of the op amp.

Application solutions

Circuit designers can use rail-to-rail input op amps in virtually any op-amp configuration. To achieve optimum performance, however, circuit designers need to consider the behavior of the single-supply op-amp input stage. Let's consider the behavior of the composite and charge-pump amplifier inputs in a single-supply inverting amplifier, noninverting amplifier, and buffer circuits.

In many applications, the amplifier's common-mode input voltage can remain at a static voltage. This is true for the inverting-amplifier circuit found in **Figure 3**. The inverting-amplifier circuit gains the input signal as well as changes the signal polarity.

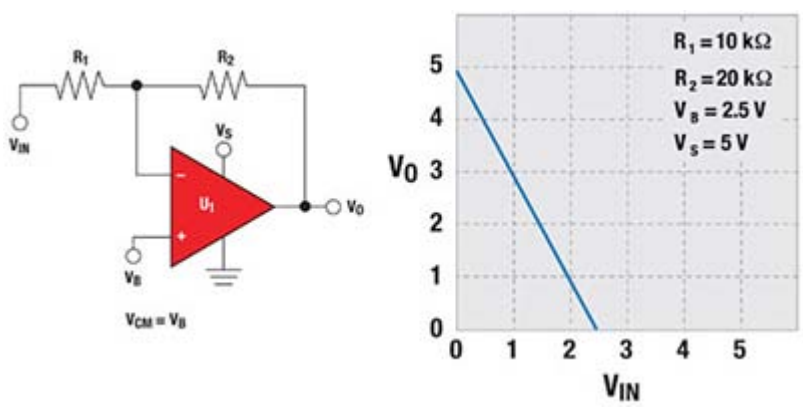

Figure 3: The inverting-amplifier circuit keeps the amplifier's common-mode voltage at a constant voltage, V_B.

The circuit requires a bias voltage, V_B, to keep the output range at V_O between the power-supply rails. When V_B establishes the common-mode voltage of the amplifier, the transfer function for this circuit is expressed as

$$V_O = V_{IN} \frac{R_2}{R_1} + V_B \frac{R_1 + R_2}{R_1}$$

The V_B voltage can be anywhere between ground and V_S, as long as the combination of the elements in this circuit (V_B, R_1, R_2, and V_{IN}) keeps the output (V_O) between V_S and ground. Since the V_B voltage is static, the amplifier's common-mode voltage remains constant. When using composite input amplifiers, choose the V_B voltage to be below or above the PMOS/NMOS transition region.

Bottom line: inverting-amplifier circuit

- **Composite input**: performs without distortion with V_B outside the PMOS/NMOS transition region
- **Charge-pump input**: performs without distortion

The noninverting amplifier's common-mode voltage (**Figure 4**) is equal to the input voltage, V_{IN}. The noninverting amplifier circuit gains the input signal with a voltage level-shift implemented with V_B.

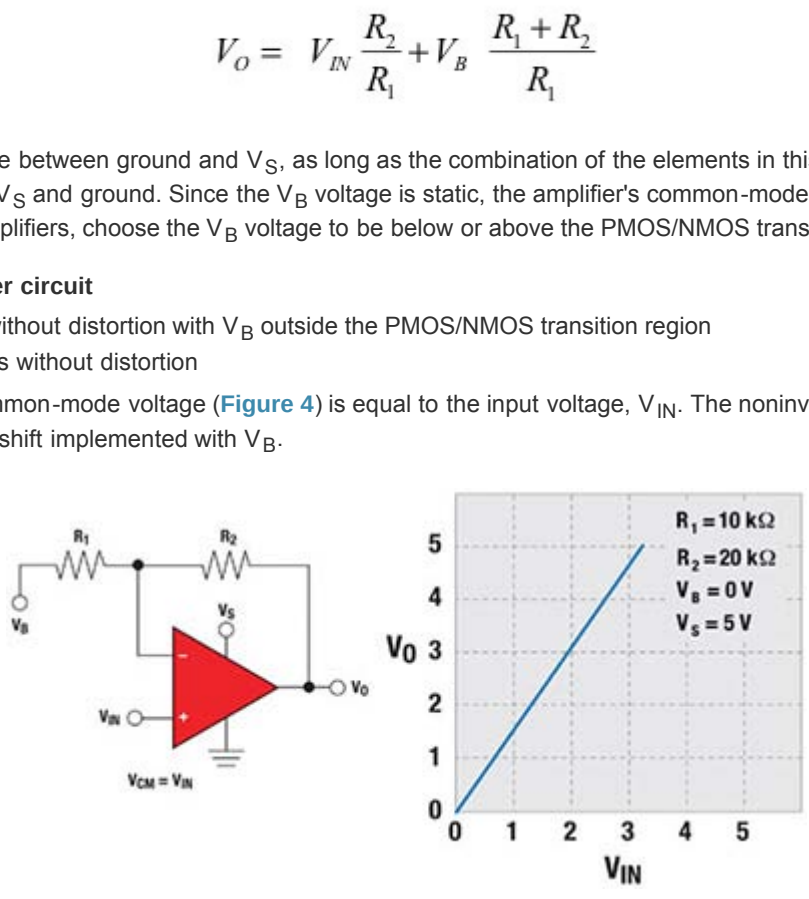

Figure 4 The noninverting gained amplifier configuration allows the amplifier's common-mode voltage to change with input signals.

For proper operation, the noninverting amplifier circuit may require a bias voltage, V_B, to keep the output range at V_O between the power-supply rails. Here V_B establishes the common-mode voltage of the amplifier. The transfer function for the circuit is expressed as

$$V_{OUT} = V_{IN} \frac{R_2 + R_1}{R_2} \quad V_B \frac{R_2}{R_1}$$

The input common-mode voltage (V_{IN}) can vary between ground and V_S, as long the voltage at V_O remains between the power-supply rails. VB can be assigned so that the input signal is not required to go across the composite input stage's crossover region. If the input signal always remains less or more than the composite input-stage's transition voltage, the circuit will not create distortion from the composite's input stage, crossover phenomena.

Bottom line: noninverting-amplifier circuit

- **Composite input**: the input signal (V_{IN}) must not travel into the transition region of the PMOS and CMOS differential input stages
- **Charge-pump input**: performs without distortion in reaction to common-mode voltage or V_{IN} changes

With a unity-gain buffer (**Figure 5**), the input signal (V_{IN}) can traverse from one rail to the other rail. In this circuit, V_{IN} establishes the amplifier's common-mode voltage. If the circuit designer uses the amplifier in a voltage follower or buffer configuration, the composite amplifier exhibits some limitations in linearity due to the input-stage topology. If the circuit designer wants a distortion-free output from this amplifier circuit, an op amp with a composite input topology may limit the input range of the buffer.

Figure 5 The input signal, V_{IN}, of the buffer circuit changes the amplifier's common-mode voltage. Composite input op amps can create distortion at the output, V_O, as V_{IN} changes.

The transfer function of the circuit in **Figure 5** is shown here:

$$V_O = V_{IN}$$

The input common-mode voltage (V_{IN}) can vary between power-supply rails. If V_{IN} travels across this entire range, the composite input amplifier produces distortion at the circuit output, V_O. If the input signal always remains less than the composite input stage's transition voltage, the circuit does not create distortion from the composite's input stage, crossover phenomena. Alternatively, an amplifier with a charge-pump input stage does not create this unwanted distortion across the entire input range.

Bottom line: buffer circuit

- **Composite input**: the op amp's input range (V_{IN}) must not travel into the transition region between the PMOS and CMOS differential input stages
- **Charge-pump input**: performs without distortion in reaction to common-mode voltage changes

Conclusion

Manufacturers use several input topologies in their designs of rail-to-rail input amplifiers. It is true that circuit designers can use rail-to-rail input amplifiers in virtually any op-amp configuration. However, if you choose to use a rail-to-rail input amplifier, it pays to understand the CMRR impact on your circuit. The composite input amplifier produces a crossover distortion, requiring special considerations in some classes of circuits. The charge-pump input amplifier does not produce this same distortion.

References

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Voltage- and current-feedback amps are almost the same

Current-feedback amplifiers have a higher slew rate than do voltage-feedback amplifiers. As such, current-feedback amps can better solve high-speed problems than their voltage-feedback counterparts. The name "current-feedback amp" carries some mystique, but, generally, the application-circuit configurations for voltage- and current-feedback amps are the same, except for a few key points.

First, the feedback resistor of a current-feedback-amp circuit must stay within a small range of values. Lower value resistors reduce the current-feedback amp's stability. The feedback resistor's higher values reduce the current-feedback amp's bandwidth. You can find the prescribed feedback-resistor value in the current-feedback amp's product data sheet. The voltage-feedback-amp's feedback-resistance value is more forgiving. This amplifier's drive capability limits the resistor's minimum value, and the overall circuit noise limits the maximum value.

Figure 1 shows a circuit that is appropriate for either a current- or a voltage-feedback amp. If the feedback resistance, R_F, equals $2R_{IN}$, where R_{IN} is the input resistance, the closed-loop gain of each channel is –2V/V. At first glance, it is easy to assume that the closed-loop bandwidth equals the gain-bandwidth product divided by each channel's gain, or |–2V/V|. Don't make this assumption!

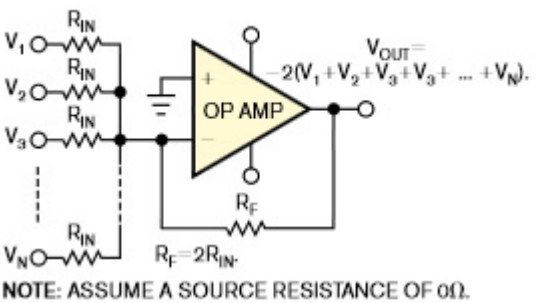

Figure 1 If you vary the number of channels in this circuit, the current-feedback amp will help keep the closed-loop bandwidth constant.

If you use a voltage- or current-feedback amp with the circuit in **Figure 1**, the noise gain is:

$$1+\frac{R_F}{R_{IN}/N}, \quad (1)$$

where N is the number of input channels. This circuit's bandwidth, with a voltage-feedback amp, equals the gain-bandwidth product divided by the noise gain. For instance, if you have a voltage-feedback amp with a gain-bandwidth product of 180 MHz and there are three input channels (N=3) at a gain of –2V/V, the circuit's closed-loop bandwidth is 25.7 MHz. Additional channels reduce the closed-loop bandwidth, even though the input signals continue to see a gain of –2V/V.

If you use a current-feedback amp with the circuit in **Figure 1**, the amplifier's closed-loop bandwidth depends less on the closed-loop gain and the number of input channels. If you design this circuit with such an amp, you would first pick the optimum feedback resistor, per the manufacturer's specification and the circuit's noise gain. You would then select the appropriate value for R_{IN}. From this point, if you add channels to the circuit, a small variation in the signal bandwidth and gain peaking in circuit may occur. If that scenario is a concern, go back and refine your feedback-resistor selection. For both current- and voltage-feedback amps, the noise gain always equals the result of **Equation 1**, but you can reduce the feedback-resistor value with the current-feedback-amp circuit and get an *increase* in circuit bandwidth.

Chapter 2: INAs and PGAs

Understanding CMR and instrumentation amplifiers

The three-op-amp instrumentation amplifier in **Figure 1** is seemingly a simple configuration in that it uses a basic, decades-old operational amplifier to gain a differential input signal. The op amp's input offset-voltage error is easy to understand. The definition of an op amp's open-loop gain has not changed. The simple idea of an op amp's CMR (common-mode rejection) has been around since the beginning of op-amp time. So what is the hang-up?

Equation 1 yields the common CMR for a single op amp and instrumentation amplifier:

$$CMR = 20\log\frac{G\times\Delta V_{CM}}{\Delta V_{OUT}},$$

Equation 1

where G is the system gain, ΔV_{CM} is the changing common-mode voltage that you apply equally to the system's input terminals with respect to ground, and ΔV_{OUT} is the change in the system's output voltage with respect to the changing V_{CM} values.

With CMR, the inner workings of the op amp are straightforward; the change of offset voltage is the only concern. Two factors influence an instrumentation amplifier's CMR. The first and most dominant factor is the balance of the resistor ratios across A_3. For instance, if R_1 equals R_3 and R_2 equals R_4, the CMR of the three-op-amp instrumentation amplifier is ideally infinite.

At a real-world level, however, the relationship of R_1, R_2, R_3, and R_4 to the instrumentation amplifier's CMR–specifically, matching the R_1-to-R_2 ratio to the R_3-to-R_4 ratio–is critical. These four resistors combine with A_3 to subtract and gain the signals from the outputs of A_1 and A_2. A mismatch be-tween the resistor ratios creates an error at the output of A_3. **Equation 2** gives the contribution to the CMR error with respect to the relationship of these resistors:

$$CMR_{A3} = 20\log\left[\frac{100\times(1+R_2/R_1)}{\%ERROR}\right].$$

Equation 2

For instance, if R_1, R_2, R_3, and R_4 are approximately the same value and the ratio of R_3 to R_4 is 1.001 of R_1/R_2, this 0.1% mismatch will cause a degradation of the instrumentation amplifier's CMR from ideal to a 66-dB level. At a gain of one, CMR_{A3} is equivalent to the CMR of the entire instrumentation amplifier.

As **Equation 1** states, the instrumentation amplifier's CMR increases as the system's gain increases–a nice feature. **Equation 1** might motivate an instrumentation-amplifier designer to ensure that there is plenty of gain available, but A_1 and A_2's open-loop gain error places a limit on this strategy. An amplifier's open-loop gain is $20\log(\Delta V_{OUT}/\Delta V_{OS})$, where V_{OS} is the offset voltage. As the gain of A_1 and A_2 increases, the offset errors from the amplifier's open-loop gain also increase. The changes in output swing of A_1 and A_2 typically span the supply rails. At higher instrumentation-amplifier gains, the open-loop gain error of the op amps dominates. These errors degrade the CMR of the instrumentation amplifier at higher gains. Consequently, the instrumentation amplifier's CMR performance values tend to reach a maximum value at higher gains.

So, from the CMR perspective, instrumentation amplifiers are systems in which various parts contribute to the CMR error at different system gains. This situation is not so mysterious when you think about the inside of this device. As you separate the parts, the picture becomes clear.

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3. Amplifiers and Linear, Texas Instruments.

Common-mode range can bite hard

My last column provided a glimpse inside the CMR (common-mode rejection) of a three-op-amp INA (instrumentation amplifier) and revealed the main contributors to total CMR error (see "Understanding CMR and instrumentation amplifiers," *EDN*, Nov 26, 2009, pg 14). This story goes deeper, however, if you look at the common-mode range of the same device. Of all the performance characteristics of an INA, the most misunderstood is the common-mode-range requirement. So how do designers calculate the INA's common-mode range? Consider the exposure to an input/gain-overload condition on the INA as a possibility.

Three basic kinds of nodes in the INA can cause input/gain-overload problems (**Figure 1**). Pay attention to the voltage levels of the INA's V_{IN+} and V_{IN-} input pins, the V_{OA1} and V_{OA2} output levels of A_1 and A_2, and the V_{OUT} output-swing capability of A_3. As you work with these concepts, you may notice that an input signal into an INA can produce an incorrect output signal that is nevertheless within the device's normal output range.

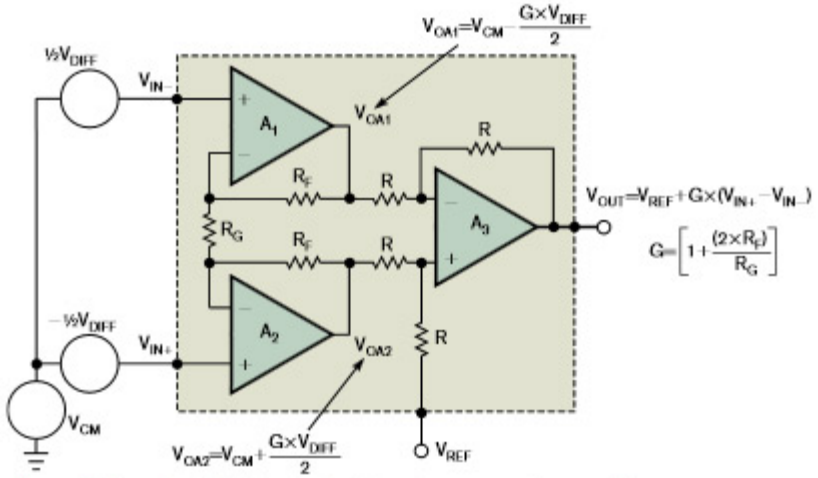

Figure 1 Three basic kinds of nodes in an instrumentation amplifier can cause input/gain-overload problems.

The applied input voltages to the INA are equivalent to the common-mode input voltage plus or minus the differential input signal. The input stages of A_1 and A_2 limit the range of these two input voltages. The maximum and minimum input-voltage limits vary from device to device.

The input voltages at V_{IN+} and V_{IN-} and the gain of A_1 and A_2 cause the internal output voltages to increase or decrease. Note that the A_1 and A_2 stages do not gain the input common-mode voltage, V_{CM}. An input/gain-overload condition can occur if A_1's output voltage, A_2's output voltage, or both violate the internal output-swing restrictions. This condition is impossible to directly measure. You must be aware of the limitations of V_{OA1} and V_{OA2} and then calculate whether your design is at risk using the equations in **Figure 1**.

An example of this type of input/gain-overload condition occurs when the in-range voltages on the INA's inputs drive A_1, A_2, or both to their positive or negative output-swing limit. In this condition, A_3 measures an erroneous difference voltage. This erroneous voltage plus the voltage reference to the INA is incorrect and may be inside the output range of A_3.

The final place to look for an input/gain-overload condition is at the output, V_{OUT}, of the INA. The A_3 output restrictions are similar to those of any other amplifier. For instance, in a single-supply environment, the output swing never spans all the way to the rails.

The common-mode behavior of the three-op-amp INA may surprise you if you ignore the nuances of the internal A_1 and A_2 output stages. All of the internal amplifier's output voltages relate to the linear common-mode input range of the complete INA. Most product data sheets provide illustrations of the effects of input/gain-overload conditions. You can now use those graphs to your advantage.

Instrumentation amplifier input-circuit strategies

Many industrial and medical applications use instrumentation amplifiers to condition small signals in the presence of large common-mode voltages. INAs have complete closed-loop operational amplifiers with feedback components included. Under normal conditions, an INA is easy to use, as long as you pay attention to the input stage and the output of the first stage. The quick and inexpensive solutions described here can help you avoid the INA circuit's input-stage pitfalls.

In a classic, three-op-amp INA (**Figure 1**), the input stage has two op amps in an adjustable-gain configuration and provides high input impedance on both the inverting (V_{IN-}) and noninverting (V_{IN+}) inputs. The output stage has four matched resistors around a single op amp. When the circuit designer exercises proper precautions with the input pins, this configuration rejects external common-mode voltage and noise. The output stage has a reference voltage that level-shifts the output with respect to ground. The level shift is convenient in single-supply applications. As with many INAs, you can program the gain found in **Figure 1** with a single resistor, R_G.

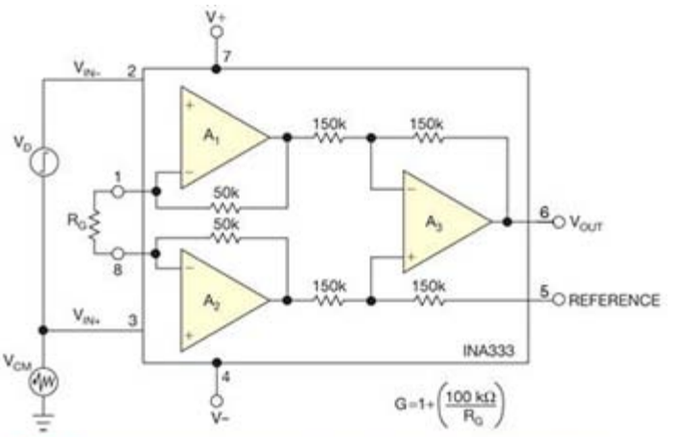

Figure 1 In a classic, three-op-amp INA topology with input sources that define V_{CM} and V_D, the input stage has two op amps in an adjustable-gain configuration and provides high input impedance on both V_{IN-} and V_{IN+}.

Depending on the INA's silicon process, V_{IN+} and V_{IN-} connect to a bipolar transistor base, FET gate, or CMOS gate. All inputs to the INA require a current-return path to ground and a bias-voltage reference. Without the current-return path and the bias-voltage reference, the INA input stage saturates or floats to an undesirable voltage. Either condition creates an invalid output voltage.

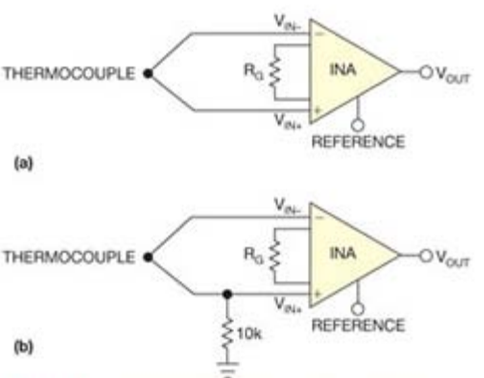

Figure 2 An incorrect thermocouple connection to the INA produces erroneous outputs (a). A correct connection to the INA's input involves biasing the input stages to ground through a 10-kΩ resistor (b).

The floating thermocouple circuit in **Figure 2a** does not provide a current path to ground or a bias-voltage reference for the INA's input pins. Thus, the input-current leakages are not dissipated, and the two inputs can float to any undefined voltage. That situation, in turn, causes the INA's output to change to an invalid output voltage, usually in the middle of the INA's output range. The invalid voltage can appear to be legitimate, making it difficult to detect the correctness of the INA input implementation. **Figure 2**b illustrates a correct thermocouple connection to an INA; both inputs have a path to ground–in this case, through a 10-kΩ resistor, biased to a voltage within the INA's input range, or ground.

Circuit designers often misapply a thermocouple or even a two-wire microphone to the INA's input circuit; the problem arises when the INA inputs are connected without proper consideration to current paths or biasing. Heed those considerations for the INA's input stage, and you can be confident that the INA's output voltage is representative of the thermocouple's voltage.

But wait–there may be a problem with the output values of A_1 and A_2 (**Figure 1**). How would you solve this problem? Comment below. I'd really like to hear from you!

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Wringing out thermistor nonlinearities

Thermistor-temperature-sensing devices present a design challenge if you intend to use such a device over its entire temperature range. Typically, the thermistor is a high-impedance, resistive device that eases one of the interface issues as you convert the thermistor resistance to voltage. The more difficult interface challenge is to capture the nonlinear behavior of the thermistor in a digital representation with a linear ADC.

The term "thermistor" originates from the descriptor "thermally sensitive resistor." The two basic types of thermistors are negative- and positive-temperature-coefficient devices. The negative-temperature-coef ficient thermistor best suits precision temperature measurements. You can determine the surrounding thermistor temperature by using the Steinhart-Hart equation: $T=1/(A_0+A_1(\ln R_T)+A_3(\ln R_T^3))$. In this equation, T is the temperature in degrees Kelvin; R_T is the thermistor resistance at temperature T; and A_0, A_1, and A_3 are constants that the thermistor manufacturer provides.

The thermistor-resistance change over temperature is nonlinear, as the Steinhart-Hart equation describes. When measuring temperature, drive a reference current through the thermistor to create an equivalent voltage. This equivalent voltage has a nonlinear response. You can try to compensate for the thermistor's nonlinear response with a look-up table in your microcontroller. Even though you can run this type of algorithm in your microcontroller firmware, you need a high-resolution converter to capture data during temperature extremes.

Alternatively, you can use hardware-linearization techniques before digitization and a lower resolution ADC. One technique is to place a resistor, R_{SER}, in series with the thermistor, R_{THERM}, and a voltage reference or the power supply (**Figure 1**). Setting the PGA (programmable-gain amplifier) at a gain of 1V/V, a 10-bit ADC in this circuit can sense a limited temperature range (approximately ±25°C).

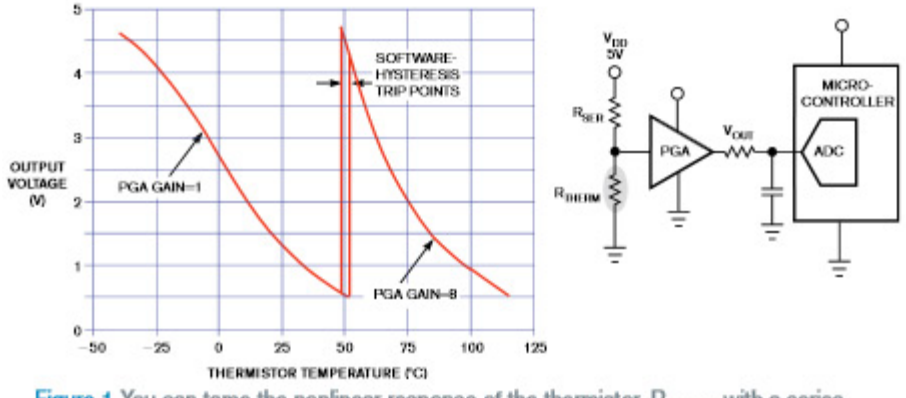

Figure 1 You can tame the nonlinear response of the thermistor, R_{THERM}, with a series resistor, R_{SER}; a PGA; and a microcontroller.

In **Figure 1**, note that resolution is lost at high temperatures. Increasing the PGA's gain at these temperatures brings the output signal of the PGA back into a range at which the ADC can reliably provide conversions that identify the thermistor temperature.

The microcontroller firmware's temperature-sensing algorithm reads the 10-bit-ADC digital value and passes it to a PGA hysteresis-software routine. The PGA hysteresis routine checks the PGA gain setting and compares the ADC digital value with the trip points that **Figure 1** indicates. If the ADC output is beyond a trip-point value, the microcontroller sets the PGA gain to the next higher or lower gain setting. If necessary, the microcontroller can again acquire a new ADC value. The PGA gain and ADC value then pass to a microcontroller piecewise linear-interpolation routine.

Obtaining data from a nonlinear thermistor sometimes can seem like an impossible task. You can combine a series resistor, a microcontroller, a 10-bit ADC, and a PGA to overcome the measurement difficulties of a nonlinear thermistor across a temperature range greater than ±25°C.

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A good holiday-season project

Which of the bulbs on a Christmas tree is the brightest? If you had the time and desire to answer this question, you could use a single photodiode to determine the brightness of your bulbs. Finding that brightest bulb among the many and the background light would be a laborious task, however, unless you expanded your design task to using two photodiodes. The two photodiodes let you find a light's position by monitoring the difference between their output signals.

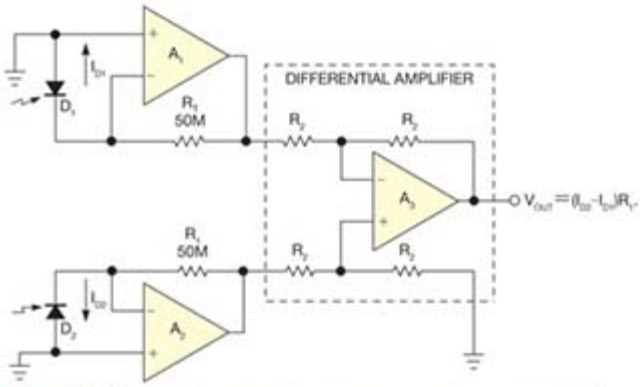

Figure 1 Differential inputs reduce common-mode errors and take the difference of the two photodiodes' signals.

If you use three op amps in a differential-photodiode-amp configuration, you will see greater accuracy in proximity and difference (**Figure 1**).

The configurations of A_1 and A_2 act as traditional current-to-voltage converters or transimpedance amps. A_3 and R_2 form a difference amp, subtracting the output voltages of A_1 and A_2. In this circuit, the incident light on the photodiode causes current to flow through the diode from cathode to anode. Because the inverting input of A_1 and A_2 has high impedance, the photodiode's currents flow through the R_1 feedback resistors. The voltage at the inverting input of the amp tracks the voltage at the amp's noninverting input.

Consequently, the amp's outputs change in voltage along with the IR drop across the R_1 resistors. The output voltages of A_1 and A_2 contain both difference and common-mode signals. A_3 rejects the common-mode signal and delivers the differential-voltage signal to the circuit output at V_{OUT}.

The key performance parameters for A_1 and A_2 are input capacitance, bias current, offset, noise, and temperature drift. The goal is to select amps in which these parameters are as low as possible. A_1 and A_2 require low-inputcurrent CMOS or FET op amps.

You can implement a differential amp discretely or with an off-the-shelf product. As long as the resistors surrounding A_3 are equal, the dc-transfer function of this circuit is 1V/V.

If the resistors around A_3 are not equal, a noticeable gain error can occur between the two input signals. You can easily compensate for this type of error by replacing any of the four resistors with a potentiometer. More important, however, this type of mismatch can introduce nonlinearities in the system when the common-mode voltage of the two inputs changes. You define the common-mode voltage of the input signals as $(V_{A1OUT}+V_{A2OUT})/2$. Ideally, the differential amp rejects common-mode-voltage changes. The calculated CMR (common-mode-rejection) error due to resistor mismatches is $100\times(1+R_2/R_1)$/(% of mismatch error).

An equal illumination on the two photodiodes makes the output voltage 0V. D_1 and D_2 respond linearly to illumination intensity, which makes the magnitude of the output voltage a direct measurement of the difference between the direct light impinging on D_1 and D_2.

A single photodiode provides some measure of a light's intensity through the magnitude of the diode's output signal. However, background-light conditions can influence this magnitude, requiring calibrated and impractical measurement conditions. Adding a matched photodiode and monitoring the difference between the two diode outputs removes the equal offsets the two diodes produce. Background light adds only an offset to the photodiode's outputs, and the differential amp removes this effect.

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About the author

Bonnie Baker is a Senior Applications Engineer with the WEBENCH® team for Texas Instruments and has been involved with analog and digital designs and systems for over 30 years. In addition to her fascination with circuit design, Bonnie has a drive to share her knowledge and experience. She has written hundreds of articles, design and application notes, conference papers, articles, including a monthly column in EDN magazine and on edn.com called "Baker's Best." Additionally, Bonnie has authored a book: "A Baker's Dozen: Real Analog Solutions for Digital Designers." Check out her latest blog, On Board with Bonnie, where she navigates the ins and outs of signal chain designs. where she navigates the ins and outs of signal chain designs. You can reach Bonnie at ti_bonniebaker@list.ti.com.

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