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Gain-of-two sample-and-hold amplifier uses no external resistors

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When you need to simultaneously sample a signal and amplify the signal level, you can cascade a common gain-of-one sample-and-hold amplifier and an amplifier with a voltage gain of one. With some exceptions, such an amplifier has two external resistors (**Reference 1**). These resistors dissipate power even at the steady state of the sample-and-hold amplifier. In monolithic ICs, power dissipation and the consequent generation of heat from resistors are not the only items in the list of the drawbacks of external resistors. Integrating precise resistors within a silicon chip requires more processing steps, because such resistors are thin-film NiCr (nickel-chromium) or SiCr (silicon-chromium) elements. Manufacturers laser-trim these resistors to a tight tolerance value, contributing to the cost of an IC. Because these resistors occupy more chip area than standard signal-processing transistors,

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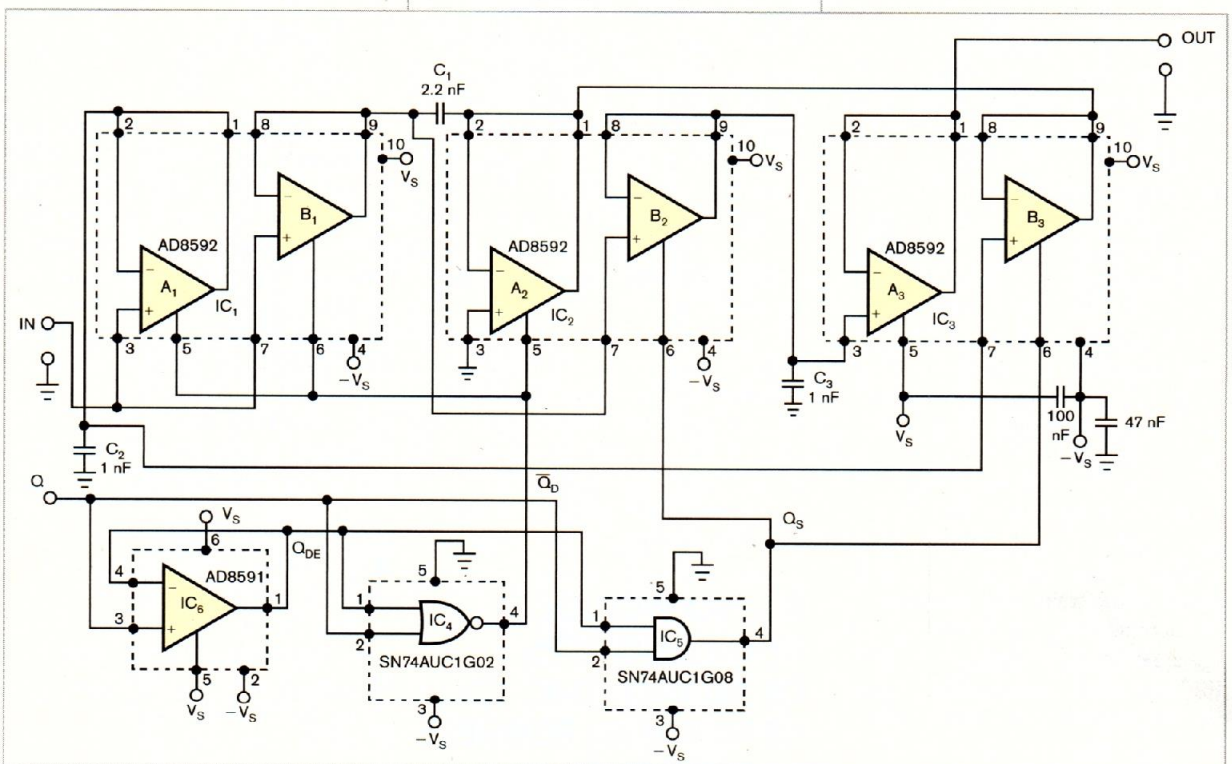

Figure 1 This sample-and-hold amplifier achieves a voltage gain of two by simultaneously tracking the input voltage on capacitors C_1 and C_2, "stacking" these capacitors within the sample interval, and storing the value of the stack's voltage in capacitor C_3.

the chip must be larger, further increasing the final cost. It's no wonder that designers of monolithic ICs as much as possible avoid using precision resistors.

If the required voltage-gain of a sample-and-hold amplifier is an integer, which it is in most cases, you can use an alternative way of increasing the magnitude of the output signal. For a voltage gain, G, the circuit can simultaneously track input voltage, V_{IN}, on temporarily ground-referenced tracking capacitors. Subsequently, an interruption occurs in tracking and cancels the ground referencing of G−1 of these capacitors. Meanwhile, the tracking capacitors stack on top of each other. The voltage on the stack is the sum of voltages of all of these capacitors, and it thus has the value of GV_{IN}. Upon the sample command, the constant voltage of GV_{IN} gets stored in the G+1 ground-referenced storing capacitor.

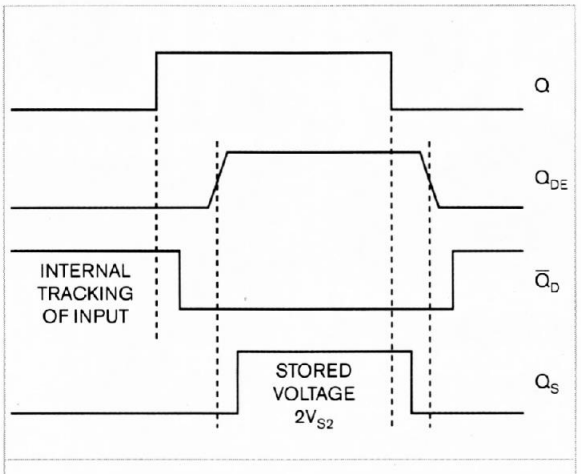

Figure 2 The external-control-logic signal, Q, splits into two quasicomplementary signals, Q_S and $\overline{Q}_D$, to avoid any internal cross-conduction in the amplifier.

Figure 1 shows an example of a sample-and-hold amplifier with a voltage gain of two. Voltage followers control the potentials on capacitors C_1, C_2, and C_3 using their shutdown function. The design uses Analog Devices' (www.analog.com) AD8592 dual op amps because their output-leakage current in shutdown mode can be lower than 10 pA (**Reference 2**). You can follow the operation of the sample-and-hold amplifier with the timing diagram (**Figure 2**). The external logic-control signal, Q_S, is at a low level, and the C_1 and C_2 capacitors simultaneously track the voltage at its input. The shutdown inputs of followers A_1, B_1, and A_2 are tied together. At $\overline{Q}_D$=high, they are enabled, so the input voltage appears at the outputs of A_1 and B_1, and no voltage appears at the output of A_2. After the high-to-low transition of $\overline{Q}_D$, a dead slot follows with each of the controlled followers turning off. At Q=high, B_3 and B_2 turn on. Thus, the voltage in C_2 appears at the output of B_3. The potential of the input voltage occurs, therefore, at the lower node of C_1 (Pin 2 of IC_2). Because C_1's voltage has the same value as the input voltage and the output voltage, the B_2 follower is $2V_{IN}$. Capacitor C_3 thus charges to the voltage of $2V_{IN}$. After the high-to-low transition of Q_S, another dead slot follows to prevent any cross-conduction in the circuit. At the next high-to-low transition of Q_S, the process repeats.

The A_3 follower serves as an impedance converter, outputting the voltage in C_3. The single NOR and AND gates, together with op amp IC_6 functioning as a delay line, modify the single external-logic-control signal to create the properly timed internal logic signals, $\overline{Q}_D$ and Q_S.

For a noise analysis, assume that the noise characteristics of each of the followers are the same—namely, the standard deviation, σ_A, of the random component of the output voltage of a single follower. At the end of the tracking interval, both C_1 and C_2 charge to the input voltage. The standard deviation of the V_{C2} voltage is σ_A only for the A_1 follower. The standard deviation of V_{C1} voltage is, however, $\sqrt{2}\sigma_A$, because C_1 charges through two series-configured followers, B_1 and A_2. The standard deviation of $V_{C1}+V_{C2}$ voltage thus has the value of $\sqrt{3}\sigma_A$. The voltage of $V_{C1}+V_{C2}$ applies to C_3 through two followers in a cascade, B_3 and B_2, within the sample interval. Further, the V_{C3} voltage applies to the output through the A_3 follower. Because all of the noise sources are mutually independent and because they all effectively act in series, the standard deviation of the output voltage is $\sigma_{OUT}=\sqrt{6}\sigma_A$. Increasing the integer gain to the value of G yields $\sqrt{3G}\sigma_A$. You now pose an RSNR (relative signal-to-noise ratio) as gain, G, over a relative increment of noise at the output, yielding:

$$RSNR = \frac{G}{\frac{\sigma_{OUT}}{\sigma_A}} = \sqrt{\frac{G}{3}}.$$

For the sample-and-hold amplifier in **Figure 1**, the RSNR equals 0.8165, meaning that the noise characteristics of the circuit are slightly worse than those of a single follower. For a gain of three, the RSNR has the value of one, and, starting from a gain of four, at which the RSNR is 1.155, it gradually rises with increasing gain. The conclusion is that, for voltage gains of four or higher, the noise characteristics of the sample-and-hold amplifier are better than those of a single follower. EDN

IT'S NO WONDER THAT DESIGNERS OF MONOLITHIC ICs AS MUCH AS POSSIBLE AVOID USING PRECISION RESISTORS.

REFERENCES

1 Štofka Marián, "Gain-of-two instrumentation amplifier uses no external resistors," *EDN*, Feb 15, 2007, pg 81, www.edn.com/article/CA6413786.

2 "AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ±250 mA Output Current and a Power-Saving Shutdown Mode," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.