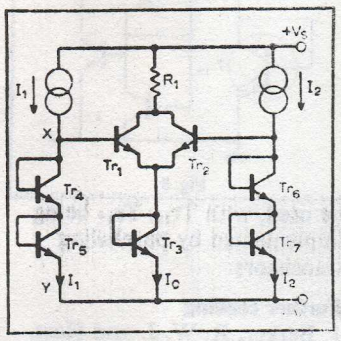
Root-law array



Typical data
Tr_1-Tr_3 3/5 of CA3086
Tr_4-Tr_7 4/5 of CA3086
$+V_S$ $\pm 5V$ R_1 33kΩ
For graphs, currents I_1 and I_2 are derived from calibrated current sources.
$I_O=\sqrt{I_1^2+I_2^2}$. Percentage error shown in graphs.

Circuit description
This circuit is a special case of a general root law circuit[1], using bipolar transistor-array packages. The performance depends on the fairly precise relationship which exists between the collector current I_C and the V_{BE} of a transistor. Assuming that the common-base current gain $\alpha=1$, then $I_C=k \exp V_{BE}/V\varphi$, where $V\varphi$ is the thermal potential. As $V_{BE}=V\varphi \log I_C/k$, then in the path XY, $V_X=2V\varphi \log I_1/k$ because there are two diodes in series. There is only one diode in the Tr_3 path and hence $V_E=V\varphi \log I_O/k$. I_O can be written in terms of the base-emitter voltage of Tr_1, giving

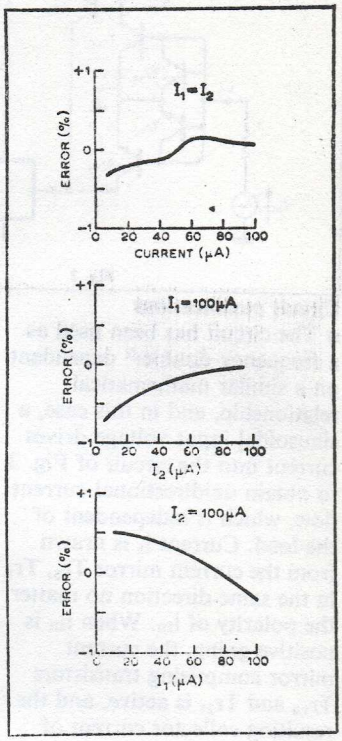
$$I_O=k\sum_1^m \exp (V_X-V_E)/V\varphi,$$

where m is the number of paths like XY. Hence by substituting for $V_X/V\varphi$ and $V_E/V\varphi$,

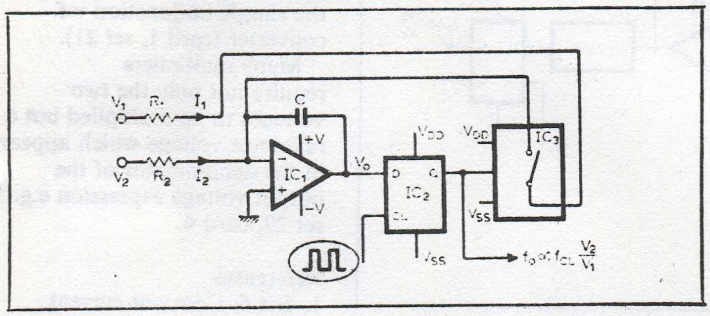
$$I_O=\sum_1^m k\,(I_1/k)^2 : (k/I_O)$$

$$=\sum_1^m I_1^2/I_O,$$

giving $I_O=\left[\sum_1^m (I_1)^2\right]^{\frac{1}{2}}$. Above, $m=2$, $I_1=I_2$ and $I_O=(I_1^2+I_2^2)^{\frac{1}{2}}$. Current flow directions of I_1 and I_2 should be as shown. If these currents are to be derived from an alternating voltage source, then circuits must be provided to ensure the above polarities are maintained.



Voltage divider



Typical performance
IC_1 741 op-amp $\pm 7.5V$ supplies
IC_2 ½ of CD4013, D-type flip-flop
IC_3 ¼ of CD4016 f.e.t. switch
V_{DD} +7.5V, V_{SS} −7.5V
Clock pulses 3V pk-pk square wave, mean value zero, frequency 10kHz.
V_2 −7.5V, V_1 positive voltage
R_2 1MΩ, R_1 100kΩ
C 2.2nF

Circuit description
Voltage V_2 is a negative voltage which will cause the integrator IC_1 to ramp positively. The slope of this is slow since R_2 is large. When I_1 is permitted to flow to the summing junction (f.e.t. switch of IC_3 closed), the op-amp will ramp downwards provided $I_1>I_2$. In ramping downwards Vo will go below the threshold level of the D-type flip-flop IC_2 and on the occurrence of the next negative going edge of the clock Q will go low, the switch will open; I_1 is thus cut-off and the op-amp will begin to ramp positively again. This will continue until D is high on the trailing edge of a clock pulse when I_1 will again be switched in. The trace above shows a typical Vo (IC_1 output). The lower level of this waveform varied somewhat (from −2V for a large V_1 to −0.25V for a small V_1). The slope of the positive ramp is, of course, constant for constant V_2 but as V_1 is varied the negative-going slope varies.

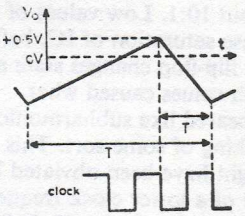
Clearly in a complete period T the charge put in by V_2 is cancelled by the charge withdrawn by V_1 as the starting and finishing voltages are the same.

i.e. $I_2T=I_1T'$

$$\therefore \frac{1}{T}=\frac{I_2}{I_1T}=\frac{V_2}{V_1}\frac{R_1}{R_2}\cdot\frac{1}{T'}$$

i.e. $$f_o=\frac{V_2}{R_2}\frac{R_1}{V_1}\cdot f_{CL}\cdot\frac{1}{V_1}$$

Hence, if R_1, R_2, and the clock frequency are constant we obtain a frequency proportional to V_2/V_1.



We fixed V_2 at −7.5V for convenience and varied V_1. For V_1 in the range 1.5V to 6.5V the frequency f_o varied from 865Hz to 3472Hz, the product V_1f_o remaining constant within 0.2% proving the division to be accurate.

Note that T′ need not be one clock period as shown but will be an integral multiple of the clock period. Furthermore, in our description we have implied that the switching level of the D-type flip-flop is zero volts and this need not be so.

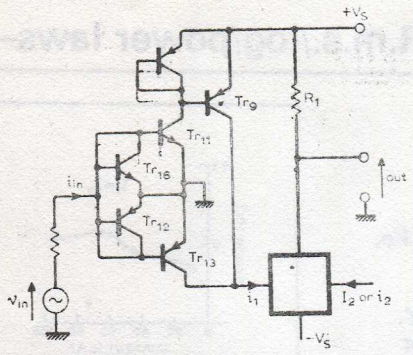


Fig. 2

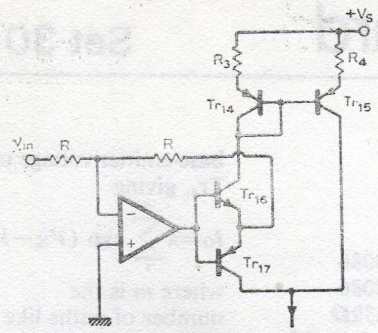


Fig. 3

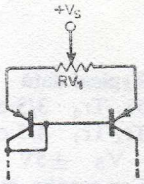


Fig. 4

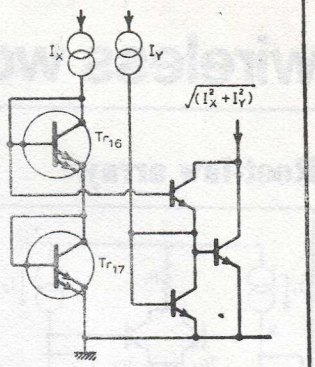


Fig. 5

Circuit modifications

● The circuit has been used as a frequency doubler[2] dependent on a similar mathematical relationship, and in this case, a sinusoidal input voltage drives current into the circuit of Fig. 2 to obtain unidirectional current flow, which is independent of the load. Current i_1 is drawn from the current mirror Tr_8, Tr_9 in the same direction no matter the polarity of i_{in}. When i_{in} is positive-going, the current mirror comprising transistors Tr_{10} and Tr_{11} is active, and the resulting collector current of Tr_{11} is mirrored by Tr_8, Tr_9. When therefore i_{in} is negative-going, an equivalent current is delivered by current mirror Tr_{12}, Tr_{13}. P-n-p transistors are required for those current mirrors and are obtained in the CA3084 i.c. A voltage output is available via R_1.

● An alternative arrangement for obtaining unidirectional current is shown in Fig. 3 using an inverting amplifier, and a complementary pair in the feedback loop. This avoids the crossover distortion that may exist in the Fig. 1 arrangement due to the finite V_{BE} drops of transistors Tr_{10}, Tr_{12}, though if $v_{in} \gg 0.6V$ this effect might be acceptable. The resistors R_3 and R_4 must be closely matched to optimise the current mirror action. RV_1 of Fig. 4 replaces R_3, R_4 and allows an alternative manual adjustment to match the collector currents.

● Another arrangement using the transconductance multiplier[4] concept is shown in Fig. 5. While this may be a configuration more likely met in a i.c. multiplier, transistor-array packages could be used, with Tr_{16}, Tr_{17} being implemented by paralleling transistors.

Further reading

1. Barker, R. W. J. and Hart, B. L., *Electronics Letters* vol. 10, 1974, pp. 439/40.
2. Barker, R. W. J., *Electronics Letters* vol. 11, 1975, pp. 106/7.
3. Barker, R. W. J. and Hart, B. L. *Journal of Physics E.* vol. 8, 1975, pp. 721/2.
4. Gilbert, B. *Electronics Letters* vol. 11, 1975, pp. 14-6.

Related circuits

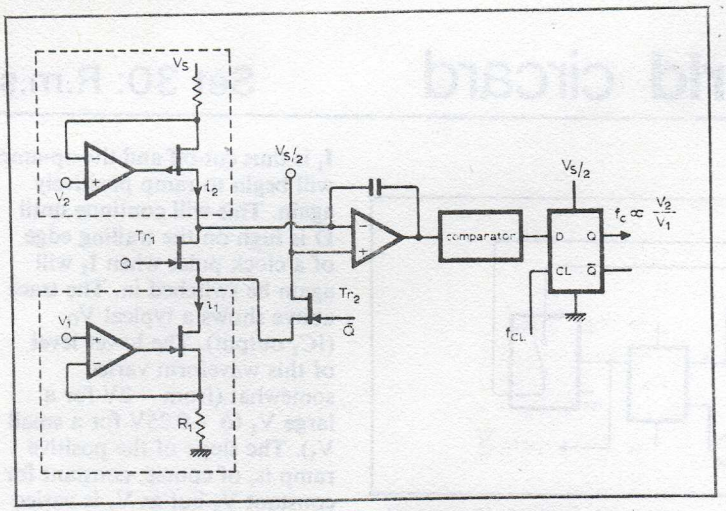
Set 30, cards 10, 5.

Component changes

With the values of R_1 and R_2 quoted, C, which does not appear in the expression for f_o, can be varied over a range of about 10:1. Low values of C cause saturation of IC_1 before the flip-flop changes state and high values caused what appeared like subharmonic locking of some sort. This might have been obviated by use of a lower clock frequency.

Changing R_1 to 10kΩ, R_2 to 1MΩ and C to 22nF made little difference to the results. One would expect R_2 max to be of the order of 1MΩ to prevent op amp input currents affecting the operation although since this is a constant effect it should not seriously affect the frequency of oscillation. The lower limit to R_1 is set by the fact that the 'on' resistance of the f.e.t. switch is approximately 300Ω i.e. $R_1 \gg 300\Omega$.

The max. V_2 is not seriously limited but V_1 is limited to be less than V_{DD} – the positive supply of the c.m.o.s. f.e.t. switch IC_3.



Circuit modifications

● In essence we have been supplying voltage-controlled currents I_2 and I_1 to the integrator. There are several ways of doing this (e.g. ref. 1). One method is as shown above centre in which the two dotted sections are accurate voltage to current converters, i_1 for example being V_1/R_1. This circuit is very similar to the one shown overleaf with the addition of an unessential comparator but has the disadvantage that V_2 is referred to V_s. This can be modified so that V_2 is referred to ground (refs 2, 3).

Note that f_o is proportional to the ratio of two voltages, the numerator one in our case being fixed. Many v-f converters operate on the same principle but keep the denominator term fixed. Such v-f converters therefore can be converted to act as divider circuits. In fact the circuit shown overleaf is identical to the delta-sigma voltage-to-frequency converter on card 3, set 21.

● Another such v-f converter is the simple unijunction v-f converter (card 1, set 21).

Many multipliers require not only the two voltages to be multiplied but a reference voltage which appears in the denominator of the output voltage expression e.g. set 29, card 4.

References

1. Set 6, Constant-current circuits, card 1.
2. Ljung, E. Accurate wide range analog multiplier, *Electronic Engineering*, July 1975.
3. Alusten, B. and Ljung, E. Accurate voltage dividing circuit, *Int. J. Electronics*, vol. 39, pp. 353-6, 1975.

Related circuits

Set 21, card 3
Set 29, card 4

wireless world circard

Set 30: R.m.s./log/power laws—3

Ramp to sinewave converter

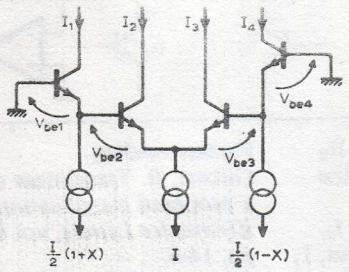


Fig. 1

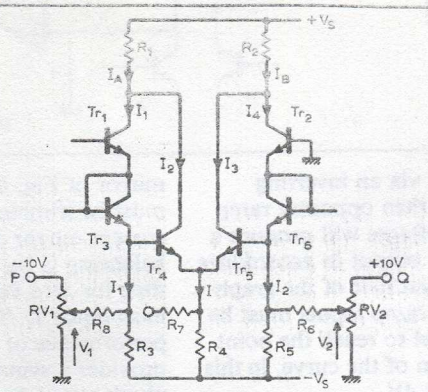
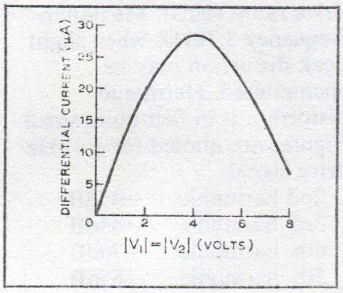


Fig. 2

Typical data
Tr_1, Tr_2 2/5 of CA3086
Tr_3–Tr_6 4/5 of CA3086
V_S ±10V
R_1, R_2 47kΩ, R_3–R_8 100kΩ
RV_1, RV_2 10kΩ
Above values are chosen to simulate the current-source relationships indicated in Fig. 1 and provide the d.c. characteristic shown in the graph



Circuit description
The circuit is based on the transconductance circuit of Fig. 1. Currents I, $(1+X)I/2$, $(1-X)I/2$, are controlled current sources, and the values are chosen to have a specific relationship. It is assumed that all the transistors are matched (Tr_1, Tr_2 must be on the same chip, and also Tr_3–Tr_6).

Summation of the base-emitter voltages in Fig. 1 gives

$$V_{BE_1}+V_{BE_2}-V_{BE_3}-V_{BE_4}=0.$$

Because the collector currents are of the form $I_C=I_S \exp qV_{BE}/kT$ then by substitution

$$(kT/q)\times\left[\log\frac{I_1}{I_S}+\log\frac{I_2}{I_S}-\log\frac{I_3}{I_S}-\log\frac{I_4}{I_S}\right]=0$$

and hence $I_1 I_2=I_3 I_4$. Hence any one current can be chosen to be a dependent output current. In Fig. 2, an extra diode in each branch means an additional V_{BE} drop must be considered, and the current relationship is then

$$I_1^2 I_2=I_3 I_4^2$$

With $I_1=(1+X)I/2$, $I=I_3+I_4$, $I_4=(1-X)I/2$ it is easily shown that

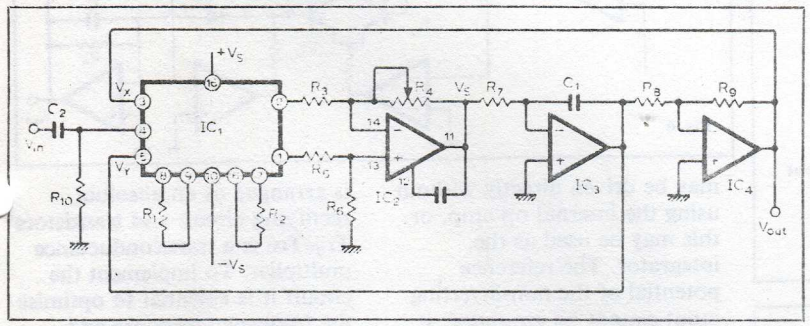
$$I_A=I_1+I/(I_1/I_4)^2+1$$

and $I_B=I_4+I/(I_4/I_1)^2+1$.

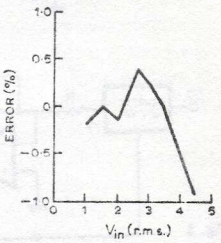
wireless world circard

Set 30: R.m.s./log/power laws—4

r.m.s. to d.c. converter



Typical data
IC_1 XR2308 V_S ±10V
IC_2 (included in IC_1)
IC_3, IC_4 SN741, R_{10}, R_7 47kΩ
R_1, R_2 22kΩ, R_8, R_9 10kΩ±0.1%
R_3, R_5 56kΩ, R_6 100kΩ
RV_4 100kΩ potentiometer
V_{in} 1-5V r.m.s. C_1, C_2 1μF
frequency 1kHz
V_{out} 1-5V d.c.



Circuit description
This circuit is based on an approach implemented in ref. 1, via an argument based on the explicit (Fig. 1) and implicit methods of establishing the r.m.s. value of a signal (Fig. 2). Notice that the squarer divider would require a device that would give an XY/Z output for X, Y, Z inputs (type AD433J). In each case, the integrator filters the fluctuating d.c. signal.

The arrangement above is based on a i.c. multiplier. IC_2 is connected as a subtractor to provide a single-ended output from the differential output currents of the multiplier section of the i.c. This is then proportional to the product $(V_{in}-V_{out})(V_{in}+V_{out})$ i.e. $(V_{in}^2-V_{out}^2)$. Under steady-state conditions, the d.c. feedback via V_X and V_U will force the mean value of this voltage, V_S, to be zero, any a.c. components being filtered by IC_3. Hence $V_{out}=(V_{in}^2)^{1/2}$ Initial setting up of the circuit to obtain the output equal to the input requires adjustment of R_4 which may shift the output zero level for $V_{in}=0$. Zero adjustment is obtained via the circuit of Fig. 3, though further adjustment of R_4 may be necessary, etc. The inverting-gain amplifier must be precisely −1, either by trimming or using accurate values of R_8, R_9.

Circuit modifications
- If pins 1 and 2, 3 and 5 are reversed, a negative d.c. output can be obtained without loss of accuracy.
- If terminals 1 and 2 (see Fig. 4) are connected to a current mirror comprising transistors Tr_1 and Tr_2, then the integrator

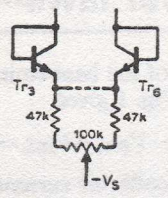


Fig. 3

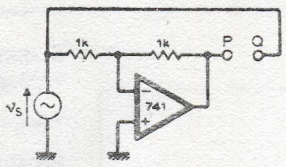


Fig. 4

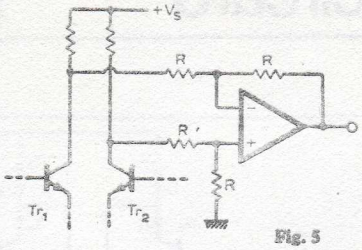


Fig. 5

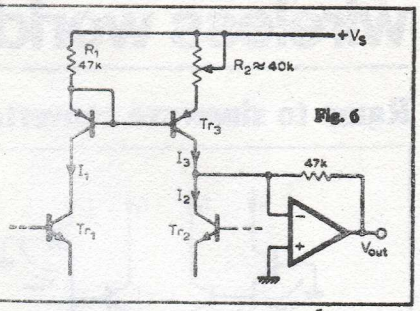


Fig. 6

Hence the differential current

$$I_A - I_B = IX\frac{(1-X^2)}{(1+X^2)}$$

With $-1<X<1$, this difference-current is claimed to approximate a sine-function within ±0.4% full-scale. Over the range of control voltages used above ($V_1=V_2=0$ to 10V) the differential current is acceptably sinusoidal over half the range.

Circuit modifications

- Fig 3 permits zero-setting of the differential current when factor $X=0$.
- If terminals P and Q of Fig. 2 are driven from a ramp-function generator, via an inverting amplifier, then opposing ramp control voltages will produce a sinusoidal output in accordance with the first half of the graph over. The ramp inputs must be such a level to reach the point of inflexion of the curve, in this case about 4V.
- To obtain a single-ended voltage output from a differential current-input, a subtracting circuit such as Fig. 5 can be used, but in this case, matching of resistors R is necessary.
- An alternative differential current-to-voltage converter is achieved using the current mirror of Fig. 6. Resistor R_2 must be trimmed to optimise current-mirror action. If balancing is such that $I_1=I_2$, then for zero voltage output, I_3 must equal I_1. Typical performance of this circuit provides a symmetrical 5.8V pk-pk cisoidal output for a 4V drive ramp signal. Maximum frequency 3.5kHz, when slight peak distortion may be encountered. Harmonic distortion is in fact quite small. Figures are quoted for a 1kHz drive signal.

2nd harmonic	−45dB
3rd harmonic	−43dB
4th harmonic	−70dB
5th harmonic	−65dB

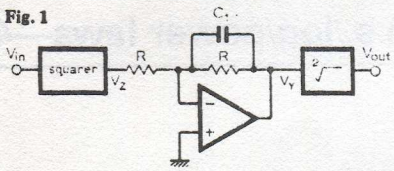
Further reading

Gilbert, B. Translinear circuits: a proposed classification, *Electronics Letters*, vol 11, pp. 14-6.
Errata to above: *Electronics Letters*, vol. 11, p. 136.

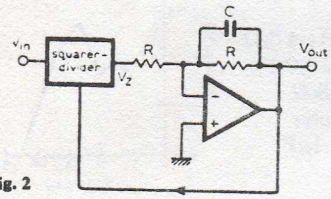
Related circuit

Set 29, card 8.

Fig. 1



$$V_Z=V_{in}^2 \quad V_Y=\overline{V_{in}^2}$$
$$V_{out}=(\overline{V_{in}^2})^{1/2}$$



$$V_Z=V_{in}^2/V_{out}$$
$$\text{and } V_{out}=\overline{V_Z}=\overline{V_{in}^2}/V_{out}$$
$$V_{out}=(\overline{V_{in}^2})^{1/2}$$

Fig. 2

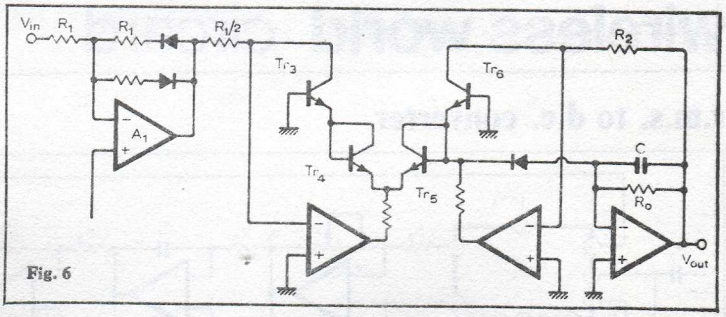


Fig. 6

Fig. 4

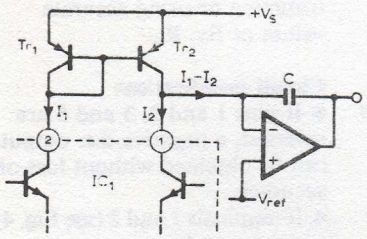


Fig. 5

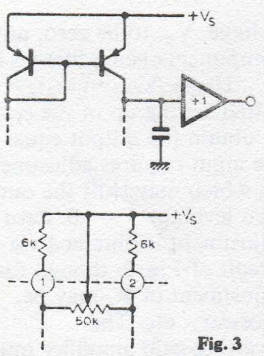


Fig. 3

may be driven directly without using the internal op amp, or this may be used as the integrator. The reference potential of the non-inverting input cannot be grounded, it must be maintained fairly positive to ensure it's within the range of potential of terminal 1.

- Another possibility is shown in Fig. 5, where because the current mirror is a current source, the capacitor can be connected directly and the output derived from a unity gain non-inverting amplifier. Fig. 6 (ref. 2) is an example of the implicit method of conversion, where A_1 amplifier is arranged as an absolute rectifying circuit and transistors Tr_3–Tr6 is a transconductance multiplier. To implement the circuit it is essential to optimise the frequency response and compensate for the limitations of the op-amps and transistors and some design guidance is given in the reference.

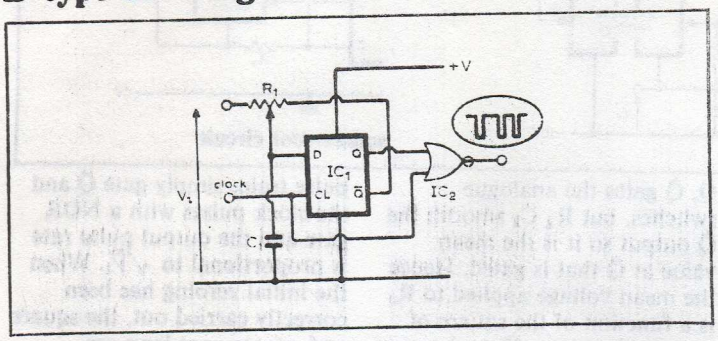
Further Reading

Gilbert, B. RMS-DC Conversion, *Electronic Letters*, vol. 11, 1975, p. 18.
Handler, H. True r.m.s. voltage conversion, *Electronic Design*, vol. 4, 1974, pp. 66-72.

Related circuits

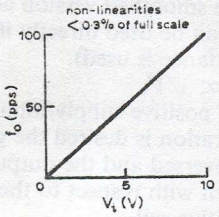
Set 30, cards 9, 3.

D-type delta-sigma converter



Typical performance

IC	½ of CD4013AE
IC_2	¼ of CD4001AE
Supply	+10V
	100kΩ pot
C_1	10nF
Clock freq.	100kHz
V_i	0-10V
f_o	$\propto V_i$
Note	$\frac{f_o}{f_{clock}} \approx \frac{V_i}{V_s}$

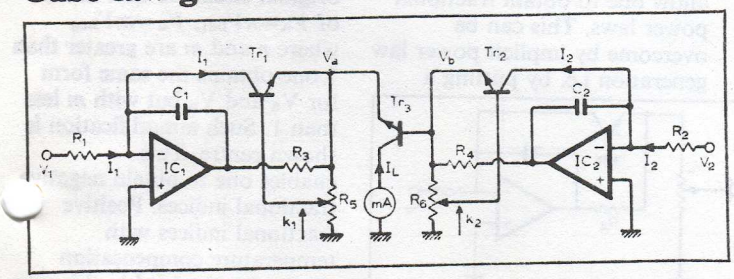


Circuit description

The delta-sigma modulator is a powerful tool in the processing of signals. Conceptually it requires a number of different sections: a D-type flip-flop; an analogue gate; a reference voltage; a comparator; an integrator. Previous designs have combined the functions of gate, reference and comparator into the flip-flop itself, using the facts that (i) the threshold level of the flip-flop is sharply defined, obviating the need for a comparator in simple applications (ii) the gate/reference section is only required to define the feedback during the pulse on-state. This is achieved for a stable supply voltage by direct feedback from the Q output since c.m.o.s. outputs switch virtually to supply levels.

This leaves the op-amp integrator as the only analogue element in the system. If the feedback is taken from the $\bar{Q}$ output to the D-input with a capacitor to ground then a virtual-earth action is achieved without the need for an operational amplifier. This remarkable simplification has one drawback—the virtual earth has an offset voltage equal to the threshold voltage of the D-type flip-flop. This varies from device to device but is (i) a relatively fixed fraction of the supply (ii) varies little with temperature. Without any precautions, and setting R_1 to its centre value, the output pulse rate has an average value that is a linear function of V_i (typically to much better than 1%). It is possible to remove the offset by the configuration shown. If the clock pulse together with the Q output is fed to a NOR gate, then when the input voltage is low the D-input will tend to drop. Once below the threshold the clock

Cube-law generator



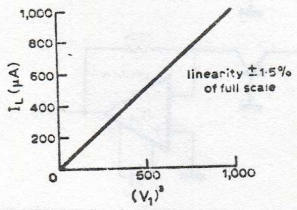
Components

R_1, R_2	10kΩ
R_3, R_4	220Ω
R_5, R_6	1kΩ
C_1	100pF, C_2 1nF

IC_1, IC_2	741
V_S	±10V
Tr_1, Tr_2, Tr_3	1/5 of CA3086
k_1	0.667 k_2 0.5

Performance

With V_1 at 10V, V_2 was adjusted so that I_L=1mA, achieved with V_2=8.65V. V_1 was then varied and produced the graph of I_L versus V_1^3 shown.



Circuit description

In the following equations the subscripts 1, 2, 3 refer to transistors Tr_1, Tr_2 and Tr_3 respectively

$V_{be1}=k_1V_a-V_a=(k_1-1)V_a$

$\therefore\ V_a=-V_{be}/(1-k_1)$

Similarly $V_b=-V_{be2}/(1-k_2)$.

Writing $1/(1-k_1)$ as n and $1(1-k_2)$ as m one obtains

$V_{be3}=V_b-V_a=nV_{be1}-mV_{be2}$

In general, $V_{be}=(kT/q)\log I/I_s$, which results in

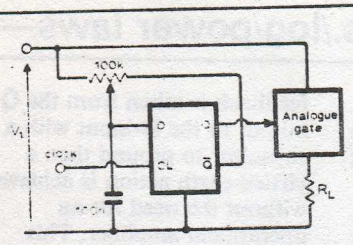
$$I_L=I_S\frac{V_1^n}{V_2^m}\cdot\frac{R_2^m}{R_1^n}\cdot\frac{1}{I_S^{n-m}}$$

As I_S is temperature dependent one can achieve some temperature compensation by maintaining $(n\text{-}m)=1$. Temperature dependence due to the kT/q terms is eliminated if all the transistors are at the same temperature.

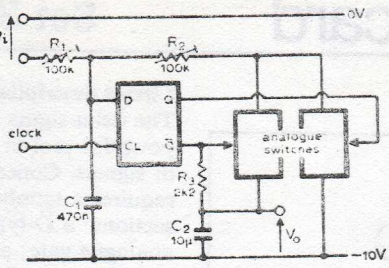
Components R_3, R_4, C_1 and C_2 do not enter into this analysis. They are used to reduce the loop gain round the i.cs so that instability, which is always a problem with these circuits, does not occur. Previous experience suggested that both C_1 and C_2 should be 100pF but on this occasion for reasons unknown this was not so.

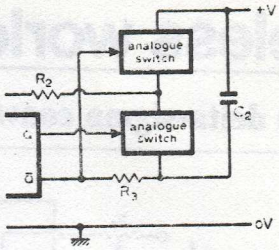
Note that the transistors used obey the log law most closely at currents below 1mA. This constrains R_1 and R_2 to be dependent in large measure on the values of V_1 and V_2. Furthermore, the op amp input currents will have an appreciable effect if I_1 and/or I_2 are less than 1μA.

Note also that for cube law generation $V_a=3V_{be}$ and $V_b=2V_{be}$. As V_a is the larger we examine its effect on the op-amp output current. If $V_a=3V_{be}$ (i.e. about 2V) then the op-amp must deliver I_1 to Tr_1 and current ($=V_a/R_5$) to R_5. Hence to avoid current saturation R_5 has to be large (e.g. R_5=100Ω is too low). On the other hand, if R_5 is a potentiometer one



squaring circuit





square-root circuit

pulses keep $\bar{Q}$ high raising the D-input again. The $\bar{Q}$ output will need to be high most of the time. This implies that Q is only high occasionally and few pulses are obtained at the output—a direct representation of the low input voltage assumed. Set V_i to zero and adjust R_1 until the output pulses are just barely inhibited. The setting is generally close to the centre-tap because the threshold is around $V/2$. This zero-setting varies the slope of the characteristic so that sensitivity controls must be adjusted after zero-setting.

Circuit modifications

- The basic circuit is a tool that can be used to implement square, square-root and multiplier functions.
- **Squaring circuit.** The flip-flop is set up for $f_o = kV_i$ as above. V_i is also applied via an analogue gate to the load. Hence the mean load voltage is proportional to $(V_i)^2$—the voltage of magnitude V_i is applied to the load for a fraction of the time proportional to V_i. In this mode the output pulses are not used directly and the NOR gate is not needed—unless transmission of the original variable V_i in serial form is desired.
- **Square root circuit.** This is achieved by the implicit method. Q, $\bar{Q}$ gates the analogue switches, but R_3 C_2 smooth the $\bar{Q}$ output so it is the mean value at $\bar{Q}$ that is gated. Hence the mean voltage applied to R_2 is a function of the square of the mean output. If the input is applied with respect to the ground the output is obtained from $\bar{Q}$ to the negative line. (The smoothed version across C_2 can be used directly if a high resistance is used). $V_o \propto \sqrt{V_i}$.
- If positive supply/input operation is desired the gating is reversed and the output taken with respect to the positive rail.
- If the output is required as a pulse train, simply gate $\bar{Q}$ and the clock pulses with a NOR gate and the output pulse rate is proportional to $\sqrt{V_i}$. When the initial zeroing has been correctly carried out, the square and square-root laws are followed with errors of <1% of full-scale. As noted earlier the scaling factor is affected by the zero-setting.

Related circuits

Set 30, cards 1, 10
Set 29, card 3

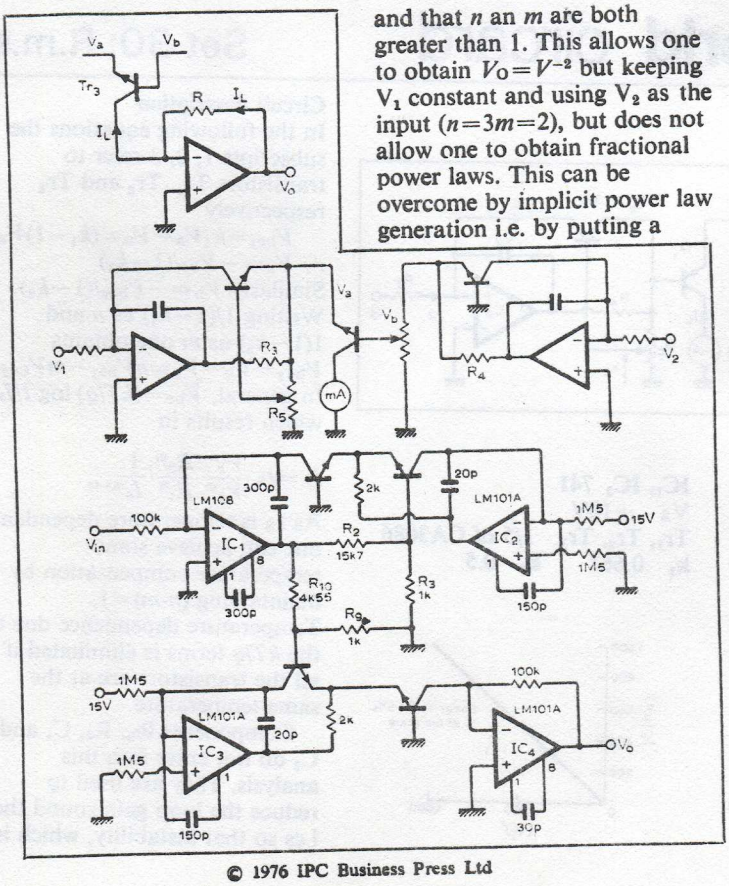
requires that the transistor base current is negligible compared with the current through R_5, otherwise the voltage on the pot. arm will not be $k_1 V_a$. This indicates the need for a low value of R_5. If the current gain of the transistors is taken as 50 then the value of 1kΩ for R_5 is about the maximum useful.

Accuracy and range of circuits such as this is much affected by operational amplifier offset voltage, bias current and offset current. Op-amps such as the LM108 or a f.e.t. input stage op-amp such as the CA3130 are preferable to 741s.

Circuit modifications

- If one requires a voltage output rather than a current output then the modification above will suffice. V_O is given by $V_O = I_L.R$ where I_L is the current in Tr_3.

The circuit is described as a cube generator, but from the expression for I_L it is clear that any power law can be generated, with the provisos that n-m=1 for temperature compensation,



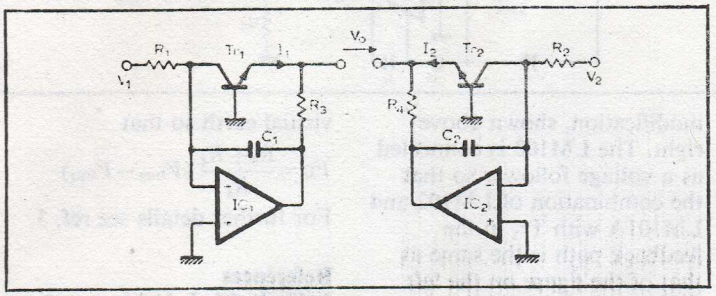
and that n an m are both greater than 1. This allows one to obtain $V_O = V^{-2}$ but keeping V_1 constant and using V_2 as the input (n=3m=2), but does not allow one to obtain fractional power laws. This can be overcome by implicit power law generation i.e. by putting a power law device $y = x^k$, (y output, x input), in the feedback path of an op-amp so that $V_O = V_{in}^{1/k}$. A partial alternative is to modify the original circuit so that instead of $V_a = nV_{be1}$, $V_b = mV_{be2}$ where n and m are greater than 1 one obtains the same form for V_a and V_b but with m less than 1. Such a modification is shown centre. This enables one to obtain negative fractional indices. Positive fractional indices with temperature compensation cannot be obtained in this way.

The circuit shown bottom is a cube law generator (Ref. 1). More generally $V_O = V_{in}^a$, where $a = 16.7R_9/(R_9 + R_{10})$ so that one can obtain any positive power law. Like the original circuit two transistors are fed from potentiometers (R_2-R_3, R_{10}-R_9). The circuit is very similar to the multiplier in ref. 2.

References

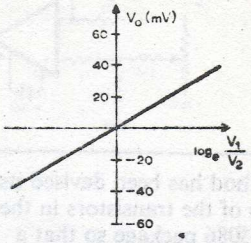
1. National Semiconductor application notes AN30.
2. Set 29, card 4
Set 30, card 7

Logarithmic amplifier



Components
R_1, R_2 10kΩ
R_3, R_4 2.2kΩ
C_1, C_2 100pF
IC_1, IC_2 741 ±7.5V supplies
Tr_1, Tr_2 1/5 of CA3086

Performance
With V_2 set at 0.25V the graph shown was obtained. Origin corresponds to V_1=0.25V, slope is 17.8mV/octave and



range of V_1 two decades, from 0.03V to 4.0V. Linearity better than 1%.

Circuit description
The following equations can immediately be given

$$V_O = V_{be1} - V_{be2}$$

$$V_{be1} = \frac{kT}{q}\log_e\frac{I_1}{I_S}, V_{be2} = \frac{kT}{q}\log_e\frac{I_2}{I_S}$$

$$I_1 = \frac{V_1}{R_1}, I_2 = \frac{V_2}{R_2}$$

Hence $V_O = \frac{kT}{q}\log_e\frac{V_1}{V_2}$

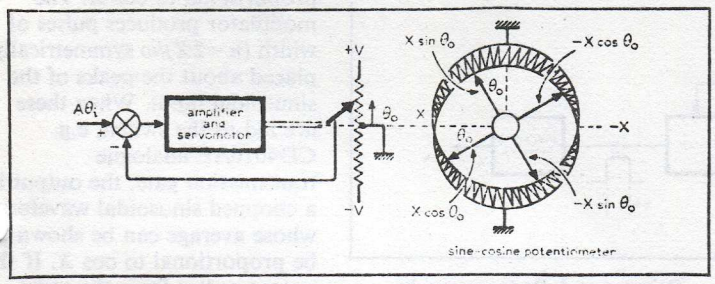
i.e. if V_2 is held constant then V_O is proportional to the log of V_1. At room temperatures $kT/q \approx 26$mV and for any octave change in V_1/V_2, V_O will change by approximately 18mV.

Inclusion of R_3 and C_1 around IC_1 and of R_4 and C_2 around IC_2 prevents oscillation of the amplifiers. Considering IC_1, we have a loop gain and the gain of the feedback path. The transistor Tr_1 is in common-base mode and hence has a voltage gain g_mR_1, R_1 being the load on Tr_1 and is by superposition connected to ground. The loop gain can be very high. Resistor R_3 reduces the proportion of the output voltage fed to Tr_1 and hence reduces the gain. Likewise, high frequency gains are reduced to zero by the inclusion of C_1 across the amplifier.

Despite these safeguards the circuit does have a tendency to oscillate and care must be taken with wiring. Note that the transistor is linearly related to the current so the problem is increased for high current levels. Further, at high current levels bulk resistance effects in the transistor come into play and destroy the simple logarithmic relationship. It is, therefore, important to keep V_1/R_1 and V_2/R_2 to levels which the transistors will accept.

Circuit modifications
Methods of temperature compensation using transistor arrays have recently been reported, refs. 1, 2. A simpler

Resolvers

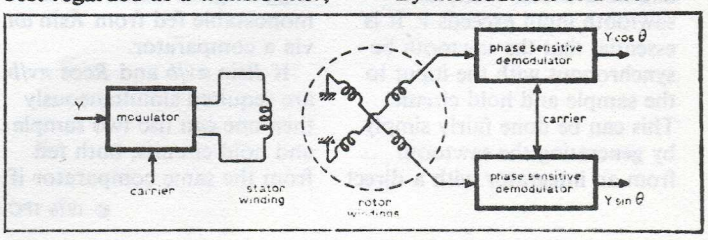


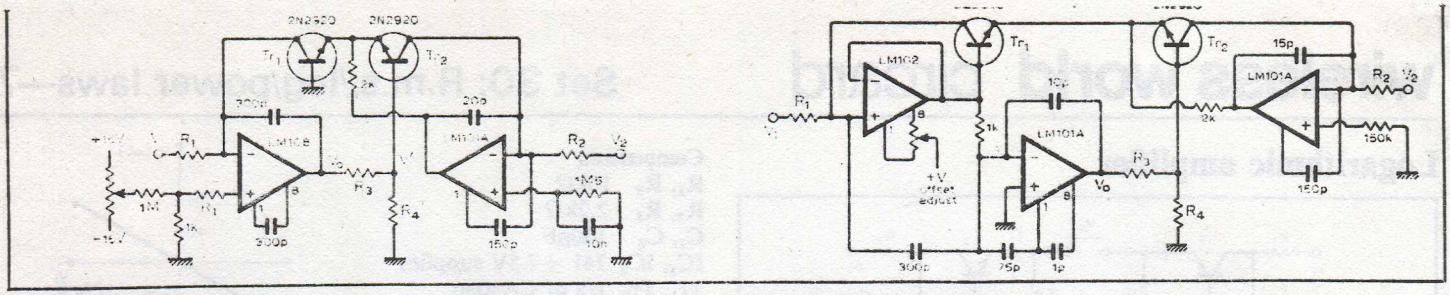
A resolver is a device which with input v produces an output proportional to sin v or cos v: frequently both outputs are available giving $a = R\sin v$ and $b = R\cos v$ i.e. the vector R/v is resolved into its two rectangular components. These devices are used widely in navigation and range instrumentation, where high bandwidth is not required. The circuit above left consists of a simple servomechanism which will rotate through θ_o degrees in response to some input. If $A = 1$ then $\theta_o = \theta_i$ in the steady state in response to a step.

In addition to the normal feedback potentiometer there is also attached to the shaft a sine-cosine potentiometer generally wound through 360° and having four slider arms as shown. The shaft of this potentiometer will rotate through the same angle as the output shaft. Such arrangements suffer from all the usual disadvantages of potentiometers, wear, resolution, accuracy, etc. By using a gear box between motor shaft and sine-cosine potentiometer shaft one can improve the accuracy and resolution to less than 0.5% (static). Use of a gear box requires scaling of the input to suit. Dynamic accuracy depends largely on the servomotor.

In the induction resolver (below) the sine-cosine potentiometer is replaced by an induction machine shown, having a stator winding and two mutually perpendicular rotor windings. The device is best regarded as a transformer, the output voltages being generated in the rotor windings by induction. The angle θ shown in the output expression is the angle between the axes and is obtained by the servo arrangement shown left or by any other equivalent. The carrier frequency is usually 460Hz. Induction resolvers have the considerable advantage of being relatively maintenance-free since there are no rubbing contacts, apart from slip rings. The main problem is the production of an accurate modulation/demodulation system.

By the addition of a second





method has been devised using two of the transistors in the CA3086 package so that a controlled temperature can be achieved in this package at the same time as using two of the remainder for the logarithmic amplifier. Details will appear in a future set. The circuit shown above acts in a manner very similar to the basic circuit overleaf. It is easy to show that

$$V_O = \frac{R_3 + R_4}{R_4}(V_{be2} - V_{be1})$$

from which

$$V_O = \frac{-kT}{q}\left(\frac{R_3 + R_4}{R_4}\right)\log_e\left(\frac{V_1 R_2}{R_1 V_2}\right)$$

Note that V_O is now referred to ground potential. Further, if $R_3 \gg R_4$, and if R_4 is a temperature-controlled resistor, then compensation is possible. As T is in Kelvins, V_O will change by 0.33% per deg. C.

This circuit with the bias and compensation networks shown is described in some detail in ref. 3. It is claimed to have a dynamic range of 100dB. The circuit is slow, the output typically taking several milliseconds to settle within 1% of final value. The LM108 does not have great bandwidth but does have a low input current, making it suitable as an input stage. To speed up the system by replacing the LM108 by an LM101 requires some modification, shown above right. The LM102 is connected as a voltage follower so that the combination of LM102 and LM101A with Tr_1 in the feedback path is the same as that of the figure on the left expect that the LM102 effectively diode connects Tr_1. This reduces the dynamic range (80dB is possible) but allows feedforward compensation on the LM101A, thereby increasing the speed of response by about two orders of magnitude. Very little current will flow through the 1kΩ resistor between the output of the LM102 and the LM101A and the input terminal of that LM101A is a virtual earth so that

$$V_Q = \frac{R_3 + R_4}{R_4}(V_{be2} - V_{be1})$$

For further details see ref. 3.

References

1. Shah, M. J. Using transistor arrays for temperature compensation, *Electronics*, April 12, 1973, p. 103.
2. Shah, M. J. Self-regulating temperature stabilised reference, EDN, May 20, 1974, pp. 74-6.
3. National Semiconductor application notes AN30.

Related circuits

Set 29, card 4
Set 30, card 6

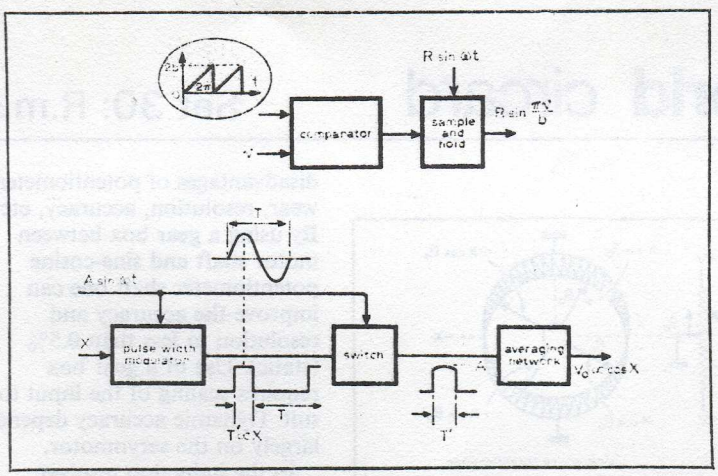
stator winding with input X, perpendicular to that shown one can obtain outputs

$U = -X\sin\theta + Y\cos\theta$
$V = X\cos\theta + Y\sin\theta$

which enable one to perform co-ordinate transformations.

Electronic resolvers are not so common as the electromechanical types. The most common type is that using a diode function generator as described in the quarter squares multiplier card (set 29, card 1). The cost of such a resolver depends on the range of input being considered, the simplest being that corresponding to 0°→90°.

The diagram above (top) shows a different approach which conceptually is very simple. A comparator is arranged to trigger a sample and hold circuit when its sawtooth input exceeds *v*. It is essential that the sawtooth be synchronous with the input to the sample and hold circuit. This can be done fairly simply by generating the sawtooth from an integrator with a direct input voltage. This produces a ramp output voltage which has to be reduced to zero every 2π radians. This can be done by inserting a f.e.t. in parallel with the feedback capacitor and triggering the f.e.t. from a monostable fed from $R\sin\omega t$ via a comparator.



If $R\sin\pi v/b$ and $R\cos\pi v/b$ are required simultaneously then one can use two sample and hold circuits, both fed from the same comparator if $R\sin\omega t$ and $R\cos\omega t$ can be generated simultaneously. Both of these signals are generated in the two integrator loop (set 26, cards 6 and 7).

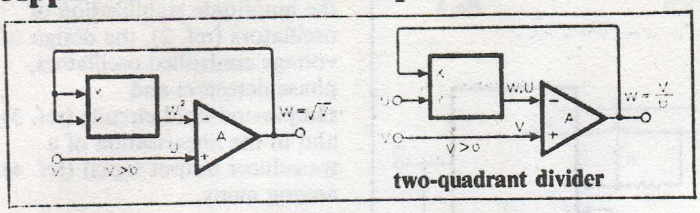
If only one signal source is available then use two sample and holds, each fed with $R\sin\omega t$, but triggered from different comparators, one fed from the sawtooth ramping from 0 to $2b$, the other ramping from $-b/2$ to $+3b/2$. In the last case the bias voltage must be able to go negative to obtain angles in the fourth quadrant.

Other electronic methods use pulse width modulation and averaging circuits. Such a scheme is the one shown left which produces an output proportional to cos *X*. The modulator produces pulses of width $(\pi - 2X)/\omega$ symmetrically placed about the peaks of the sinusoidal input. When these are fed to the switch, e.g. CD4016AE analogue transmission gate, the output is a chopped sinusoidal waveform whose average can be shown to be proportional to cos *X*. If the output pulses from the pulse width modulator are centred about the zero-crossings of the sinusoid, the output will be proportional to sin *X*.

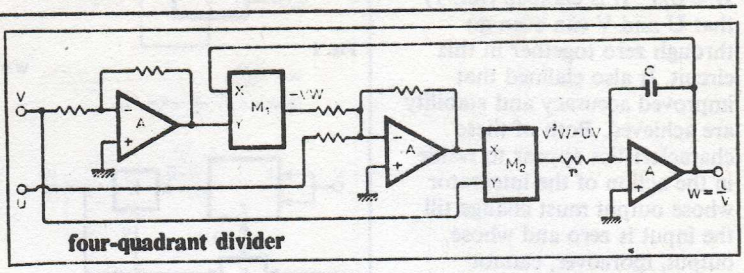
Reference

Schmid, H. Integrated circuits replace the electromechanical resolver, *Electronics*, Jan. 1966.

Applications of i.c. multipliers



two-quadrant divider



four-quadrant divider

Many multiplier modules are now available on the market (e.g. MC1594L, XR2308, AD433J). The reduced cost and improved capability and accuracy of them has produced an increasing usage; unfortunately the existence of different types has produced confusion to the uninitiated. There are at least three distinct types: those having two inputs X and Y, the output being KXY, with K a scale factor; those which have two differential inputs X and Y, the output being KXY; those having three inputs X, Y and Z the output being KXY/Z—this last one is obviously a combined multiplier/divider. Adding to the confusion is the apparently magical way in which some functions are generated. It is easy to see that the final answer is correct but there is never a logical thought process shown by which the answer was arrived at.

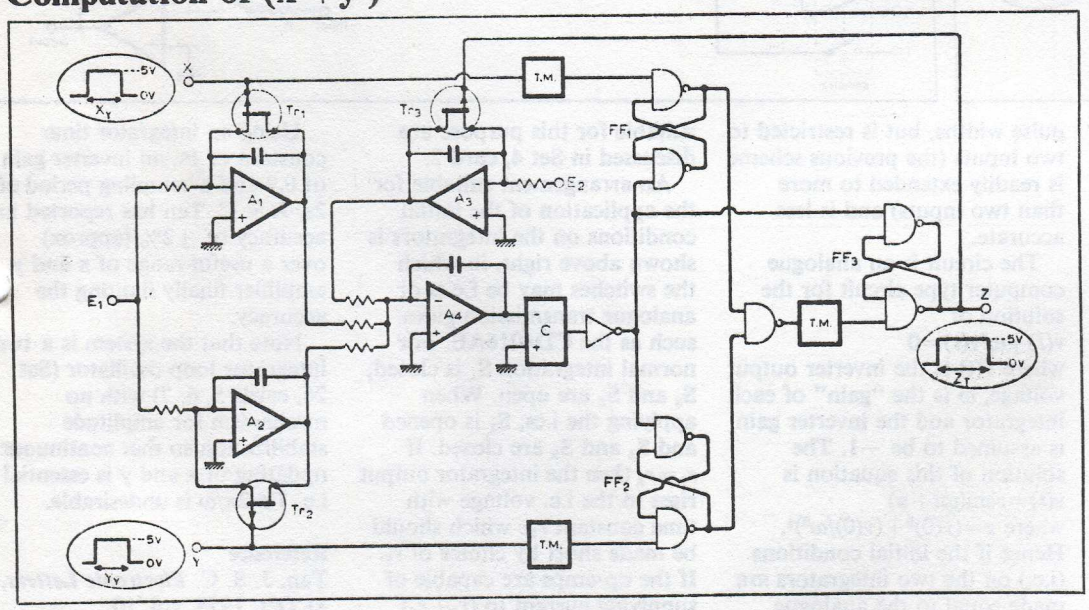
Many of the uses of multipliers involve the implicit solution of some equation. This means that the output is fed back in some manner, thereby affecting itself. All of the circuits in this card involve an implicit solution.

Above left is shown a circuit for the generation of $\sqrt{V}$. The output W is fed to a multiplier with both input terminals connected together to form a squarer. This squarer is in the feedback path of an op-amp A. As the differential input voltage of the op-amp must be zero, $V-W^2=0$ i.e. $W=\sqrt{V}$. Note that V must be positive, as otherwise negative feedback round the loop is lost and latch-up will occur.

Above centre is a multiplier connected in the feedback path of an op-amp to provide an overall division function. Polarity inversion through the multiplier must be avoided to prevent positive feedback and this restricts U to being positive. On the other hand V can be either positive or negative so that in the U-V plane one is allowed to operate in the two quadrants for which U is positive. It is clearly impossible for U to be zero but additionally if U is very small one obtains a very small feedback signal so that offset voltages and currents can cause latch up.

Above right is a four-quadrant divider in which the output of M_2 is V^2W-UV. If the inputs are d.c. then in the steady state the integrator

Computation of $(x^2+y^2)^{\frac{1}{2}}$



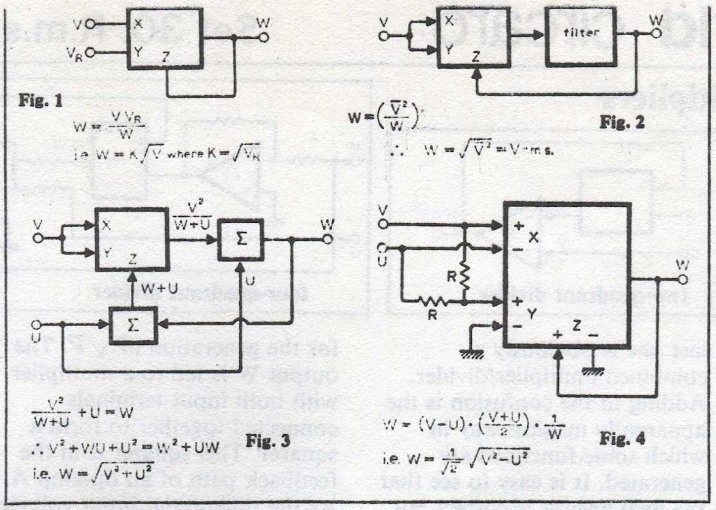
Analogue information x and y is contained in the input pulse widths x_T and y_T respectively.

On the occurrence of the pulse x, the f.e.t. switch Tr_1 opened and integrator A_1, fed from the d.c. signal E, ramps down and integrator A_4 rises in a parabolic manner to a voltage Ax_T^2, when the signal y is applied A_2 ramps giving an additional component By_T^2 to the output of A_4. y may appear before, during or after x. Whatever the case, the output of A_4 rises to $Ax_T^2+By_T^2$. At the end of this operation the R-S flip flops FF_1 and FF_2 combine with FF_3 to open switch Tr_3 allowing E_2 (negative) to integrate via A_3 and feed A_4. This causes the output of A_4 to fall. When this

Performance data
All resistors 50kΩ,
capacitors 10nF
Tr_1–Tr_3 1H5012
C (comparator) SN72810
All logic SN7400
T.M. ≡ trailing edge triggered monostable (see figure above)
$z_T=(x_T^2+y_T^2)^{\frac{1}{2}}$ within ±1%
for x_T in range 0 to 2ms
and y_T in range 0 to 1ms
E_1 +1.0V, E_2 −1.0V

implying $V^2W-UV=0$ i.e. $W=U/V$. It is claimed (ref. 1) that U and V can even go through zero together in this circuit. It also claimed that improved accuracy and stability are achieved. Both of these characteristics appear to reside in the action of the integrator whose output must change till the input is zero and whose output, moreover, cannot change rapidly.

Turning now to the more complex multipliers, note the circuit simplicity of Figs. 1 to 4. Fig. 1 shows a square rooting circuit, Fig. 2 an r.m.s. to d.c. converter (compare card 4) and Figs. 3 and 4 show vector sum and vector differencing circuits. Note the vector sum relationship can also be obtained by mechanising the relationship $V^2/(W-U)-U=W$. The apparent simplicity vaporizes to an extent when one examines the actual implementations recommended by the module manufacturers. The modules are liberally surrounded by assorted external components the aim of which is to minimize errors. Fortunately these recommendations are fairly specific since the questions of errors and bandwidth are difficult for multipliers alone; when combined in complex circuits the analysis really is awkward.

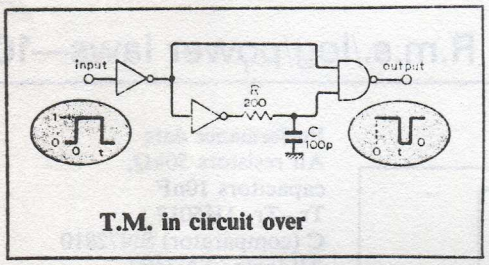


Another point which must be mentioned is that of scaling: it is always necessary to ensure that the design of a circuit is such that the multipliers do not saturate. This may seem obvious but with as many as six inputs, possible with the module of Fig. 4, it is all too easy to overlook this aspect or even to make a simple miscalculation.

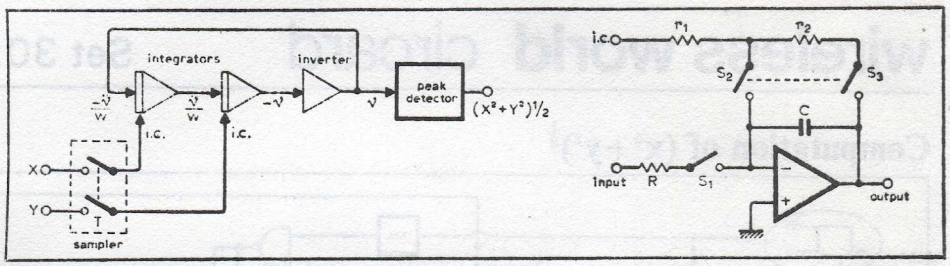
intended only as a representative sample of some things that are possible with multipliers. Other applications will be found in the amplitude stabilization of oscillators (ref. 2), the design of voltage controlled oscillators, phase detectors and sample-and-hold circuits (ref. 3) and in the linearisation of a transducer output signal (ref. 4) among many.

References

1. Korn and Korn, Electronic analog and hybrid computers, 2nd edition, McGraw-Hill.
2. Vannerson and Smith, Fast amplitude stabilisation of an R-C oscillator, *IEEE J. Solid State Circuits*, vol. SC9, No. 4, Aug. 1974.
3. Ryan, C. R. Applications of a four quadrant multiplier, *IEEE J. Solid State Circuits*, Feb. 1970, pp. 45-8.
4. Trofimenkoff and Smallwood, Analog multiplier circuit linearises transducer output, *IEEE Trans.* vol. IM23, no. 3, Sept. 1974.



T.M. in circuit over



fall reaches zero, the comparator C changes state and becomes high causing FF_3 to become low and switching off Tr_3. The time for which E_2 is applied is

$$z_T=\left(\frac{Ax_T^2}{C}+\frac{By_T^2}{C}\right)^{\frac{1}{2}}$$

With the circuit elements chosen, $A/C=B/C=1$, giving the required relationship.

Reference

Ikeda, H. *Electronics Letters*, 30 Oct. 1975, vol. 11.

Related circuits

Set 19, card 4
Set 15, cards 4, 6
Set 30, card 1

Alternative circuit

This circuit (middle) has the advantage that the inputs can be simple voltages, rather than pulse widths, but is restricted to two inputs (the previous scheme is readily extended to more than two inputs) and is less accurate.

The circuit is an analogue computer type circuit for the solution of

$v(t)+\omega^2 v(t)=0$

where $v(t)$ is the inverter output voltage, ω is the "gain" of each integrator and the inverter gain is assumed to be -1. The solution of this equation is

$v(t)=z\sin(\omega t+\varphi)$

where $z=(v(0)^2+(v(0)/\omega^2)^{\frac{1}{2}}$. Hence if the initial conditions (i.c.) on the two integrators are made equal to the analogue voltages x and y, the resulting oscillation has a peak value $(x^2+y^2)^{\frac{1}{2}}$. Peak detectors suitable for this purpose are discussed in Set 4, card 2.

An arrangement suitable for the application of the initial conditions on the integrators is shown above right, in which the switches may be f.e.ts or analogue transmission gates such as the CD4016AE. For normal integration S_1 is closed, S_2 and S_3 are open. When applying the i.cs, S_1 is opened and S_2 and S_3 are closed. If $r_1=r_3$ then the integrator output rises to the i.c. voltage with time constant r_3c which should be made short by choice of r_2. If the op-amps are capable of supplying current to (r_1+r_2) and to the following integrator/inverter then S_3 may be dispensed with.

Using an integrator time constant of 1s, an inverter gain of 0.9 and a sampling period of 2s, J. S. C. Tan has reported an accuracy of $\pm 2\%$ (approx) over a useful range of x and y, amplifier finally limiting the accuracy.

Note that the system is a two integrator loop oscillator (Set 26, cards 5, 6, 7) with no mechanism for amplitude stabilization so that continuous updating of x and y is essential i.e. $T \gg 2\pi/\omega$ is undesirable.

Reference

Tan, J. S. C. *Electronic Letters*, 31 Oct. 1974, vol. 10.

Related circuit

Set 30, cards 1, 5.