Power Gain Stages for Monolithic Amplifiers

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Most monolithic amplifiers cannot supply more than a few hundred milliwatts of output power. Standard IC processing techniques set device supply levels at 36V, limiting available output swing. Additionally, supplying currents beyond tens of milliamperes requires large output transistors and causes undesirable IC power dissipation.

Many applications, however, require greater output power than most monolithic amplifiers will deliver. When voltage or current gain (or both) is needed, a separate output stage is necessary. The power gain stage, sometimes called a "booster," is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. The output stage's gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit phase shift, frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see box section, "The Oscillation Problem").

The type of circuitry used in an output stage varies with the application, which can be quite diverse. Current and voltage boosting are common requirements, although both are often simultaneously required. Voltage gain stages are usually associated with the need for high voltage power supplies, but output stages which inherently generate such high voltages are an alternative.

A simple, easily used current booster is a good place to begin a study of power gain stages.

150mA Output Stage

Figure 1A shows the LT1010 monolithic 150mA current booster placed within the feedback loop of a fast FET amplifier. At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f, so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Small signal bandwidth is reduced by C_f, but considerable load isolation can be obtained without reducing it below the power bandwidth. Often a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

The LT1010 is particularly adept at driving large capacitive loads, such as cables.

The follower configuration (Figure 1B) is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3μF.

Figure 1C shows LT1010's used in a bridge type differential output stage. This permits increased voltage swing across the load, although the load must float.

All of these circuits will deliver 150mA of output current. The LT1010 supplies short circuit and thermal overload protection. Slew limit is set by the op amp used.

High Current Booster

Figure 2 uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.

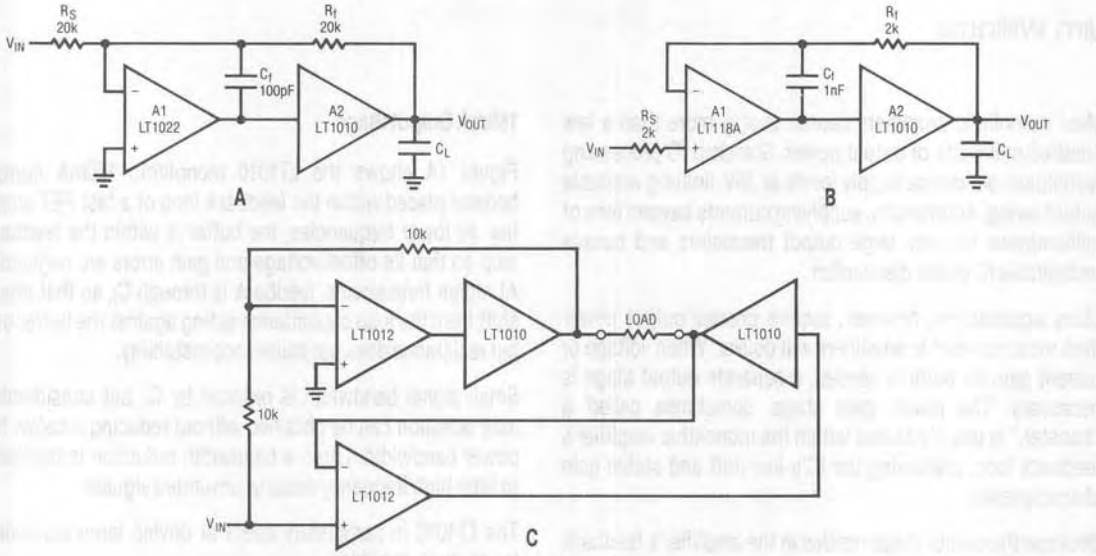


Figure 1. LT1010 Output Stages

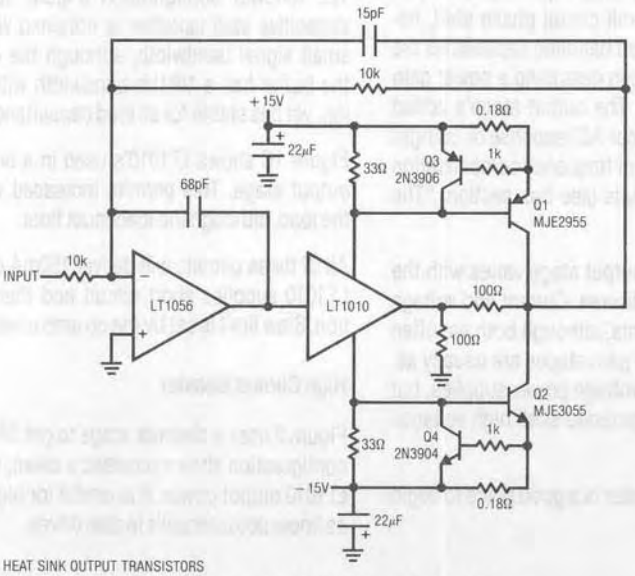


Figure 2. LT1010 Based Output Stage

The output transistors have low F_t, and no special frequency compensation considerations are required. The LT1056 is rolled off by the 68pF capacitor for dynamic stability, and the 15pF feedback capacitor trims edge response. At full power (±10V, 3A peaks), bandwidth is 100kHz and slew rate about 10V/μs.

Ultra-Fast Fed—Forward Current Booster

The previous circuits place the output stage booster within the op amp's feedback loop. Although this ensures low drift and gain stability, the op amp's response limits speed. Figure 3 shows a very wideband current boost stage. The LT1012 corrects DC errors in the booster stage, and does not see high frequency signals. Fast signals are fed directly to the stage via Q5 and the 0.01μF coupling capacitors. DC and low frequency signals drive the stage via the op amp's output. This parallel path approach allows very broadband performance without sacrificing the DC stability of the op amp. Thus, the LT1012's output is effectively current and speed boosted.

The output stage consists of current sources Q1 and Q2 driving the Q3-Q5 and Q4-Q7 complementary emitter followers. The transistors specified have F_t's approaching 1GHz, resulting in a very fast stage. The diode network at the output steers drive away from the transistor bases when output current exceeds 250mA, providing fast short circuit protection. Net inversion in the stage means the feedback must return to the LT1012's positive input. The circuit's high frequency summing node is the junction of the 1k and 10k resistors at the LT1012. The 10k-39pF pair filters high frequencies, permitting accurate DC summation at the LT1012's positive input. The low frequency roll-off of the fast stage is matched to the high frequency characteristics of the LT1012 section, minimizing aberration in the circuit's AC response. The 8pF feedback capacitor is selected to optimize settling characteristics at the highest speeds.

This current boosted amplifier features a slew rate in excess of 1000V/μs, a full power bandwidth of 7.5MHz and a 3dB point of 14MHz. Figure 4 shows the circuit driving a 10V pulse into a 50Ω load. Trace A is the input and Trace B is the output.

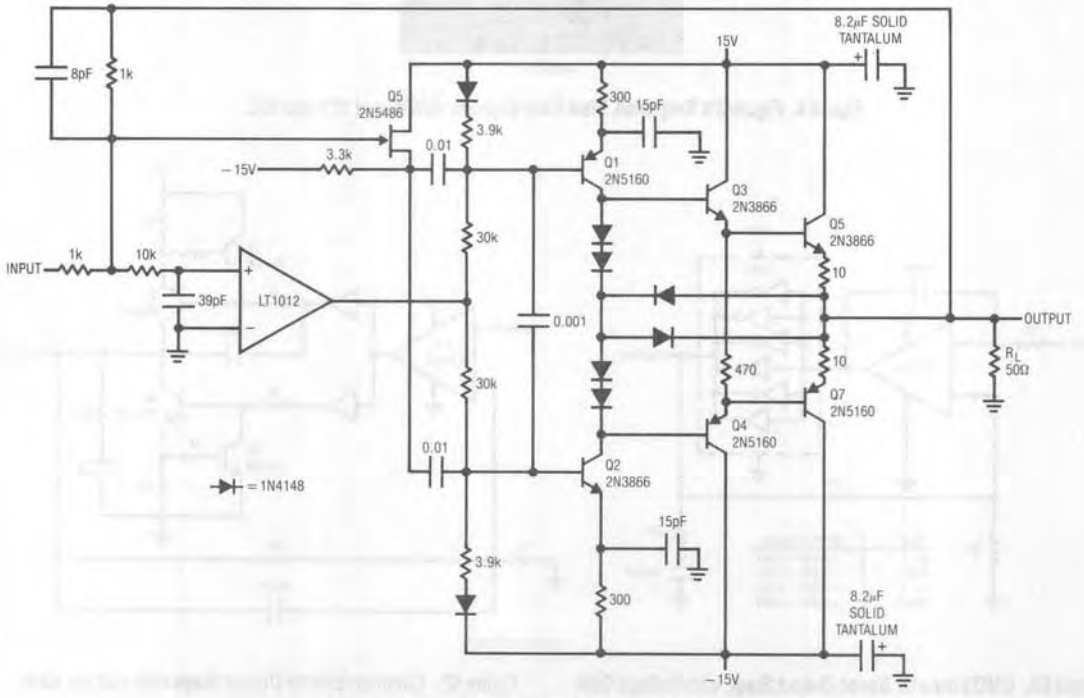


Figure 3. Fed-Forward Wideband Current Booster

Slew and settling characteristics are quick and clean, with pulse fidelity approaching the quality of the input pulse generator. Note that this circuit relies on summing action, and cannot be used in the non-inverting mode.

Simple Voltage Gain Stages

Voltage gain is another type of output stage. A form of voltage gain stage is one that allows output swing very near the supply rails. Figure 5A utilizes the resistive nature of the complementary outputs of a CMOS logic inverter to make such a stage. Although this is an unusual application for a logic inverter, it is a simple, inexpensive way to extend an amplifier's output swing to the supply rails. This circuit is particularly useful in 5V powered analog systems, where improvements in available output swing are desirable to maximize signal processing range.

The paralleled logic inverters are placed within the LT1013's feedback loop. The paralleling drops output resistance, aiding swing capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. An RC damper eliminates oscillation in the inverter stage, which has high gain-bandwidth when running in its linear region. Local capacitive feedback at the amplifier gives loop compensation. The table provided shows that output swing is quite close to the positive rail, particularly at loads below several milliamperes.

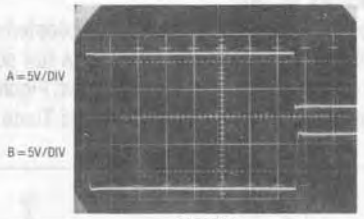


Figure 4. Figure 3's Response. Slew Rate Exceeds 1000V/μs at 10V Into 50Ω.

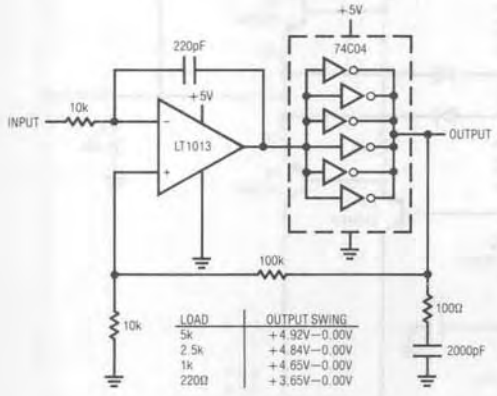


Figure 5A. CMOS Inverter Based Output Stage with Voltage Gain

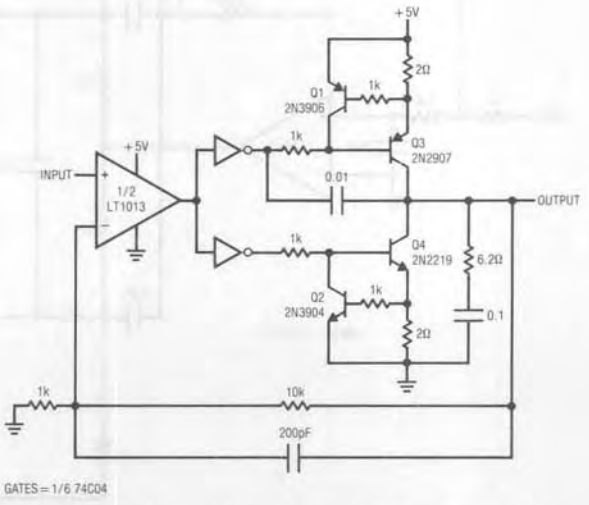


Figure 5B. Common Emitter Output Stage with Voltage Gain

Figure 5B is similar, except that the CMOS inverters drive bipolar transistors to reduce saturation losses, even at relatively high currents. Figure 6A shows Figure 5B's output saturation characteristics. Note the extremely low saturation limits below 25mA. Removing the current limit circuitry permits even better performance, particularly at high output currents.

Figure 6B shows waveforms of operation for circuit Figure 5A. The LT1013's output (Trace B) servos around the 74C04's switching threshold (about 1/2 supply voltage) as it controls the circuit's output (Trace A). This allows the amplifier to operate well within its output swing range while controlling a circuit output with nearly rail-to-rail capability.

High-Current Rail-to-Rail Output Stage

Figure 7 is another rail-to-rail output stage, but features higher output current and voltage capability. The stage's voltage gain and low saturation losses allow it to swing nearly to the rails while simultaneously supplying current gain.

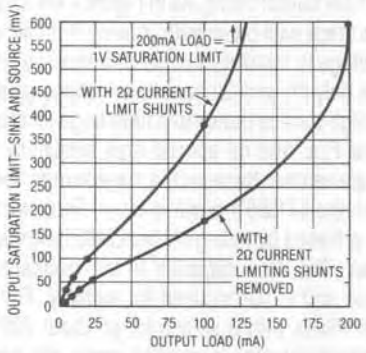


Figure 6A. Figure 5B's Saturation Characteristics

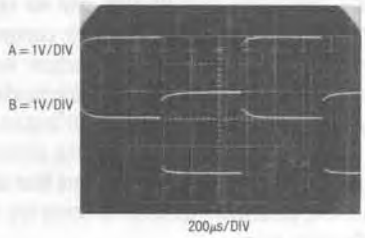
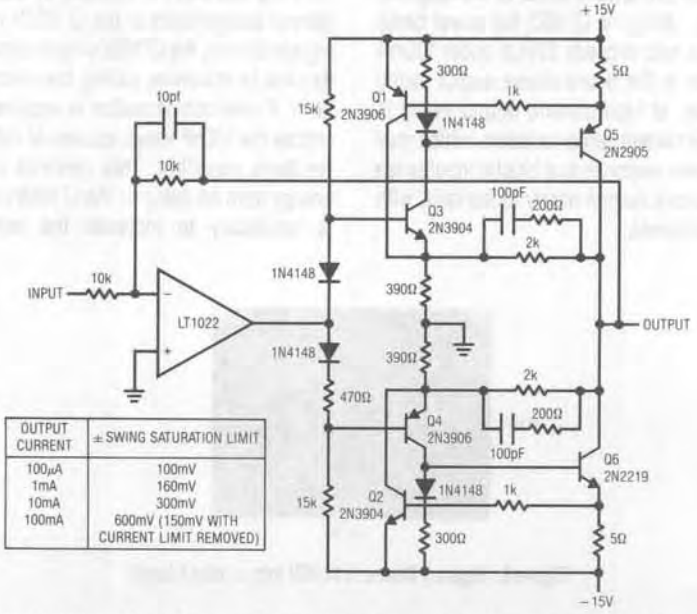


Figure 6B. Figure 5A's Waveforms



OUTPUT CURRENT	± SWING SATURATION LIMIT
100μA	100mV
1mA	160mV
10mA	300mV
100mA	600mV (150mV WITH CURRENT LIMIT REMOVED)

Figure 7. Complementary Closed Loop Common Emitter Stages Provide High Current and Good Saturation Performance

Q3 and Q4, driven from the op-amp, provide complementary voltage gain to output transistors Q5-Q6. In most amplifiers, the output transistors run as emitter followers, furnishing current gain. Their V_{BE} drop, combined with voltage swing limitations of the driving stage, introduces the swing restrictions characteristic of such stages. Here, Q5 and Q6 run common emitter, providing additional voltage gain and eliminating V_{BE} drops as a concern. The voltage inversion of these devices combines with the drive stage inversion to yield overall non-inverting operation. Feedback is to the LT1022's negative input. The 2k-390Ω local feedback loop associated with each side of the booster limits stage gain to about 5. This is necessary for stability. The gain bandwidth available through the Q3-Q5 and Q4-Q6 connections is quite high, and not readily controllable. The local feedback reduces the gain bandwidth, promoting stage stability. The 100pF-200Ω damper across each 2k feedback resistor provides heavy gain attenuation at very high frequencies, eliminating parasitic local loop oscillations in the 50-100MHz range. Q1 and Q2, sensing across the 5Ω shunts, furnish 125mA current limiting. Current flow above 125mA causes the appropriate transistor to come on, shutting off the Q3-Q4 driver stage.

Even with the feedback enforced gain-bandwidth limiting, the stage is quite fast. AC performance is close to the amplifier used to control the stage. Using the LT1022, full power bandwidth is 600kHz and slew rate exceeds 23V/μs under 100mA output loading. The chart in the figure shows output swing versus loading. Note that, at high current, output swing is primarily limited by the 5Ω current sense resistors, which may be removed. Figure 8 shows response to a bipolar input pulse for 25mA loading. The output swings nearly to the rails, with clean dynamics and good speed.

± 120V Output Stage

Figure 9 is another voltage gain output stage. Instead of minimizing saturation losses, it provides high voltage outputs from a ± 15V powered amplifier. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. ± 15V power for the LT1055 control amplifier is derived from the high voltage supplies via the zener diodes. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing ± 10V LT1055 drives to cause full ± 120V output swing. As in Figure 7, the local feedback reduces stage gain-bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low F_T's, and no special high frequency roll-off precautions are needed. Because the stage inverts, feedback is returned to the LT1055's positive input. Frequency compensation is achieved by rolling off the LT1055 with the local 100pF-10k pair. The 33pF capacitor in the feedback peaks edge response and is not required for stability. Full power bandwidth is 15kHz with a slew limit of about 20V/μs. As shown, the circuit operates in inverting mode, although non-inverting operation is possible by exchanging the input and ground assignments at the LT1055's input. Under non-inverting conditions, the LT1055's input common-mode voltage limits must be observed, setting the minimum non-inverting gain at 11. If over-compensation is required, it is preferable to increase the 100pF value, instead of increasing th e 33pF loop feedback capacitor. This prevents excessive high voltage energy from coupling to the LT1055's inputs during slew. If it is necessary to increase the feedback capacitor, the

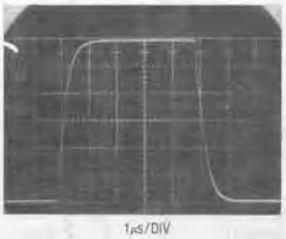


Figure 8. Figure 7 Drives ± 14.85V Into a 100mA Load

summing point should be diode clamped to ground or to the LT1055 supply terminals. Figure 10 shows results with a ±12V input pulse (Trace A). The output (Trace B) responds with a cleanly damped 240V peak-to-peak pulse.

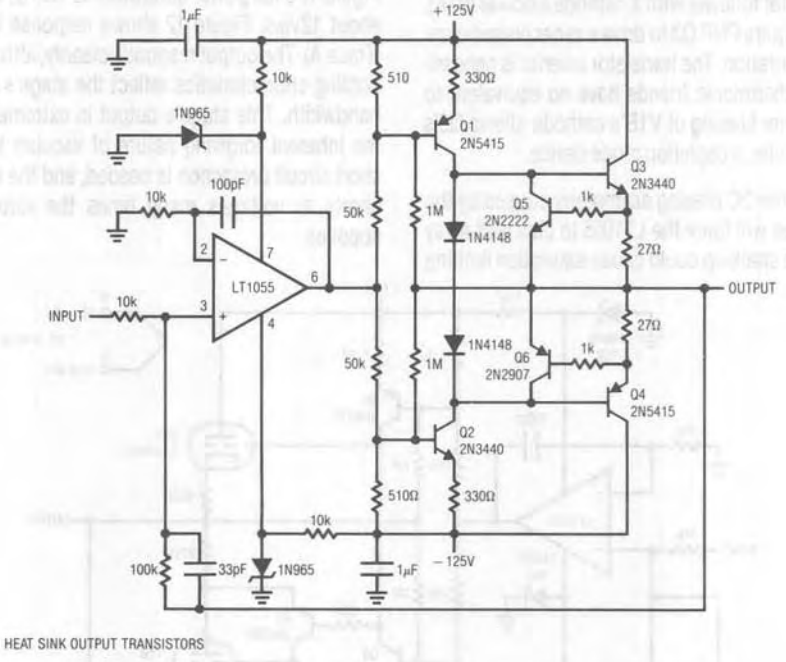


Figure 9. ±120V Output Stage. DANGER! High Voltages Present. Use Caution.

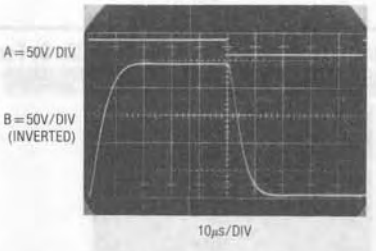


Figure 10. Figure 9 Swinging ±120V Into 6kΩ. DANGER! High Voltages Present. Use Caution.

Figure 11 is a similar stage, except that Figure 9's output transistors are replaced with vacuum tubes. Most of this stage is conceptually identical to Figure 9, but major changes are needed to get the vacuum tube output to swing negatively. Positive swing is readily achieved by simply replacing Figure 9's NPN emitter follower with a cathode follower (V1A). Negative outputs require PNP Q3 to drive a zener biased common cathode configuration. The transistor inverter is necessitated because our thermionic friends have no equivalent to PNP transistors. Zener biasing of V1B's cathode allows Q3's swing to cut off the tube, a depletion mode device.

Without correction, the DC biasing asymmetry caused by the Q3-V1B configuration will force the LT1055 to bias well away from zero. Tolerance stack-up could cause saturation limiting in the LT1055's output, reducing overall available swing. This is avoided by skewing the stage's bias string with the potentiometer adjustment. To make this adjustment, ground the input and trim the potentiometer for 0V out at the LT1055.

Figure 11's full power bandwidth is 12kHz, with a slew rate of about 12V/μs. Figure 12 shows response to a bipolar input (Trace A). The output responds cleanly, although the slew and settling characteristics reflect the stage's asymmetric gain-bandwidth. This stage's output is extremely rugged, due to the inherent forgiving nature of vacuum tubes. No special short circuit protection is needed, and the output will survive shorts to voltages many times the value of the ±150V supplies.

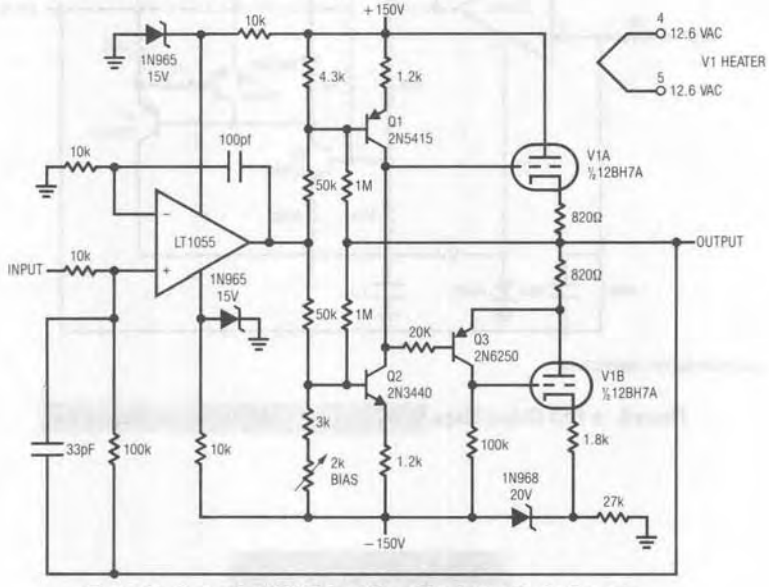


Figure 11. Rugged ±120V Output Stage Employing Mr. De Forest's Descendants. DANGER! High Voltages Present. Use Caution.

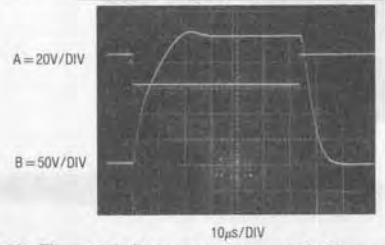


Figure 12. Figure 11's Response. Asymmetric Slew and Settling Are Due to Q3-V1B Connection. DANGER! High Voltages Present. Use Caution.

Unipolar Output, 1000V Gain Stage

Figure 13 shows a unipolar output gain stage which swings 1000V and supplies 15W. This boost stage has the highly desirable property of operating from a single, low voltage supply. It does not require a separate high voltage supply. Instead, the high voltage is directly generated by a switching converter which is an integral part of the gain stage.

A2's output drives Q3, forcing current into T1. T1's primary is chopped by MOSFET's Q1 and Q2, which receive complementary drive from the 74C04 based square wave oscillator. A1 supplies power to the oscillator. T1 provides voltage step-up. Its rectified and filtered output is the boost stage's output.

The 1M-10k divider furnishes feedback to A2, closing a loop around it. The 0.01μF capacitor from Q3's emitter to A2's negative input gives loop stability and the 0.002μF unit trims step response damping. C1 is used for short circuit limiting. Current from Q1 and Q2 passes through the 0.1Ω shunt. Abnormal output currents cause shunt voltage to rise, tripping C1's output low. This simultaneously removes drive from Q3, Q1 and Q2's gates and the oscillator, resulting in output shutdown. The 1k-1000pF filter ensures that C1 does not trip due to current spikes or noise during normal operation.

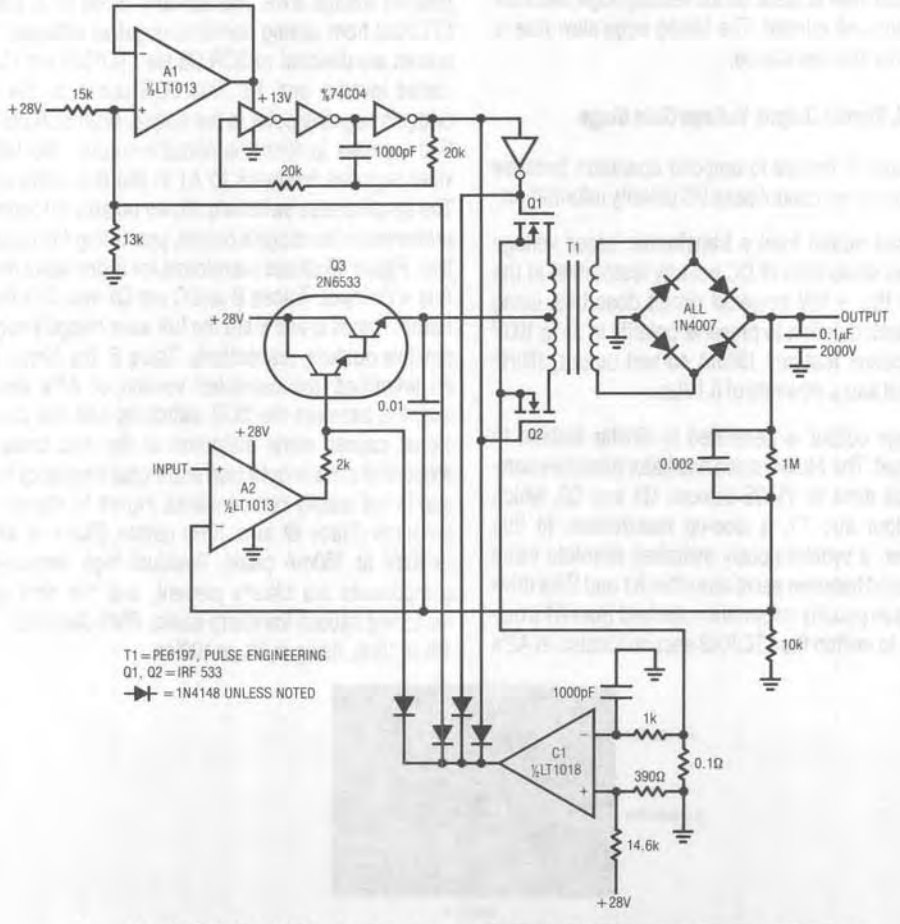


Figure 13. 15 Watt, 1000V Unipolar Output Stage. DANGER! High Voltages Present. Use Caution.

A2 supplies whatever drive is required to close the loop, regardless of the output voltage called for. The low, resistive saturation losses of the VMOS FETs combined with A2's servo action allows controlled outputs all the way down to 0V.

Substituting higher power devices for Q1 and Q2 along with a larger transformer allows more output power, although dissipation in Q3 will become excessive. If higher power is desired, a switched mode stage should be substituted for Q3 to maintain efficiency.

The 0.1μF filter capacitor at the output limits full power bandwidth to about 60Hz. Figure 14 shows dynamic response at full load. Trace A, a 10V input, produces a 1000V output in Trace B. Note that slew is faster on the leading edge, because the stage cannot sink current. The falling edge slew rate is determined by the load resistance.

± 15V Powered, Bipolar Output, Voltage Gain Stage

Figure 13's output is limited to unipolar operation because the step-up transformer cannot pass DC polarity information.

Obtaining bipolar output from a transformer based voltage booster requires some form of DC polarity restoration at the output. Figure 15's ± 15V powered circuit does this, using synchronous demodulation to preserve polarity in its ± 100V output. This booster features 150mA current output, 150Hz full power output and a slew rate of 0.1V/μs.

The high voltage output is generated in similar fashion to Figure 13's circuit. The 74C04 based oscillator furnishes complementary gate drive to VMOS devices Q1 and Q2, which chop Q3's output into T1, a step-up transformer. In this design, however, a synchronously switched absolute value amplifier is placed between servo amplifier A1 and Q3's drive point. Input signal polarity information, derived from A1's output, causes C1 to switch the LTC1043 section located at A2's positive input. This circuitry is arranged so that A2's output is the positive absolute value of A1's input signal. A second, synchronously switched LTC1043 section gates oscillator pulses to the appropriate SCR trigger transformer at the output. For positive inputs LTC1043 pins 2 and 6 are connected, as well as pins 3 and 18. A2, acting as a unity gain follower, passes A1's output directly and drives Q3. Simultaneously, oscillator pulses are conducted through an inverter via LTC1043 pin 18. The inverter drives trigger transformer T2, turning Q4 on. Q4, biased from the full wave bridge's positive point, supplies positive polarity voltage to the output.

Negative inputs cause the LTC1043 switch positions to reverse. A2, functioning as an inverter, again supplies Q3 with positive voltage drive. The Schottky diode at A2 prevents the LTC1043 from seeing transient negative voltages. Oscillator pulses are directed to SCR Q5 via LTC1043 pin 15, its associated inverter and T3. This SCR connects the full wave bridge's negative point to the output. Both SCR cathodes are tied together to form the circuit's output. The 100k-10k divider supplies feedback to A1 in the conventional manner. The synchronous switching allows polarity information to be preserved in the stage's output, permitting full bipolar operation. Figure 16 shows waveforms for a sine wave input. Trace A is A1's input. Traces B and C are Q1 and Q2's drain waveforms. Traces D and E are the full wave bridge's negative and positive outputs, respectively. Trace F, the circuit output, is an amplified, reconstructed version of A1's input. Phase skewing between the SCR switching and the carrier borne signal causes some distortion at the zero crossover. The amount of skew is both load and signal frequency dependent, and is not readily compensated. Figure 17 shows distortion products (Trace B) at a 10Hz output (Trace A) at full load (± 100V at 150mA peak). Residual high frequency carrier components are clearly present, and the zero point SCR switching causes the sharp peaks. RMS distortion measured 1% at 10Hz, rising to 6% at 100Hz.

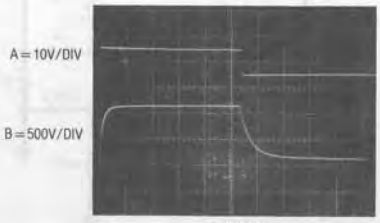


Figure 14. Figure 13's Pulse Response. DANGER! High Voltages Present. Use Caution.

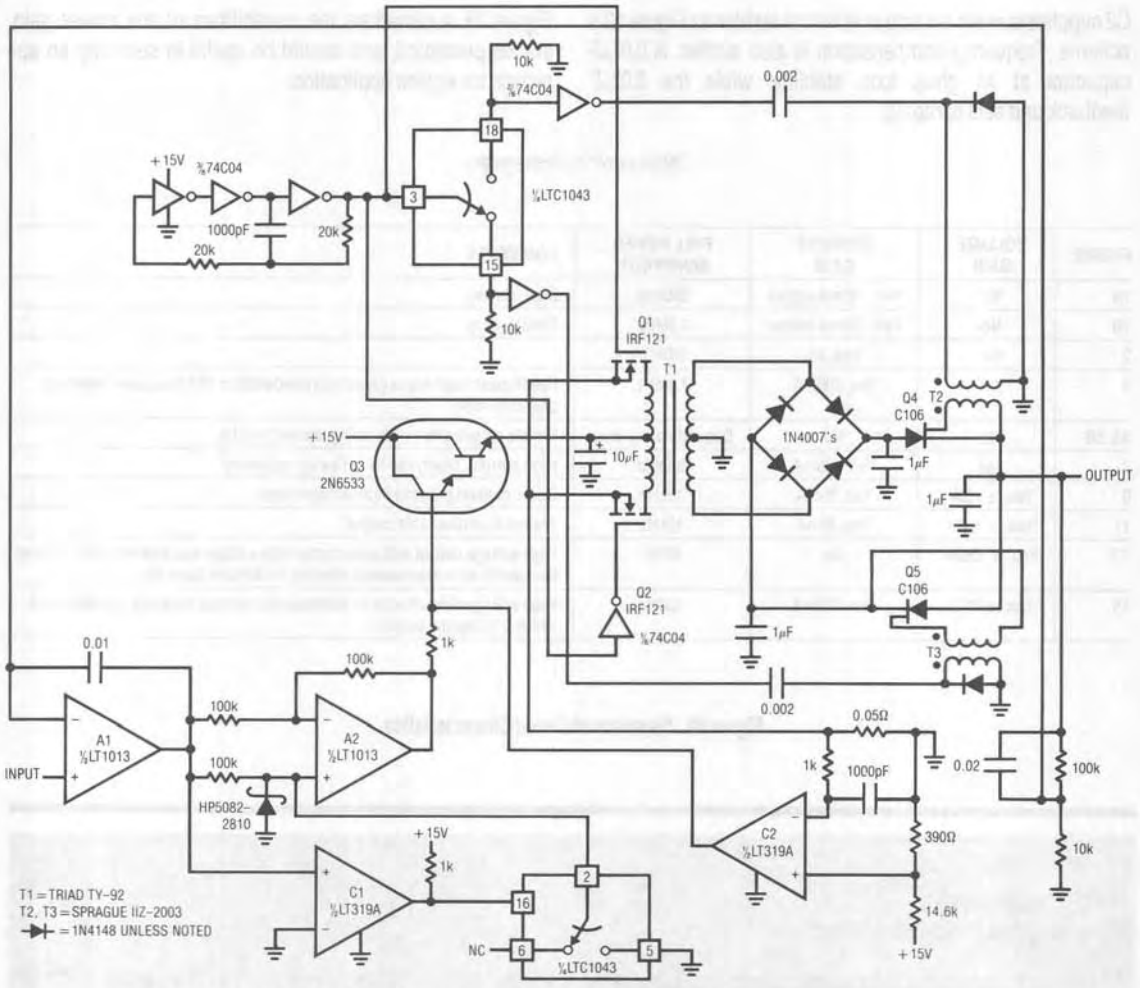


Figure 15. ± 100V Output Stage Runs From ± 15V Supply. DANGER! High Voltages Present. Use Caution.

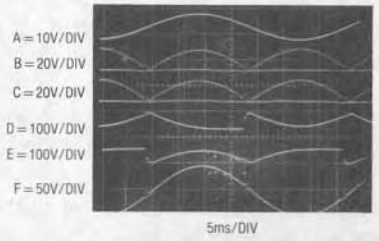


Figure 16. Figure 15's Operating Details. DANGER! High Voltages Present. Use Caution.

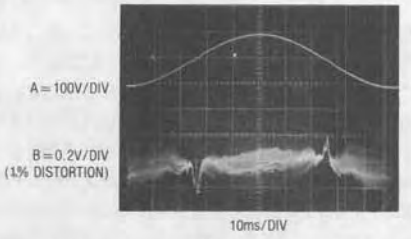


Figure 17. Crossover Residue Reflects Chopping and Zero Cross Switching. DANGER! High Voltages Present. Use Caution.

C2 supplies current limiting in identical fashion to Figure 13's scheme. Frequency compensation is also similar. A 0.01μF capacitor at A1 gives loop stability, while the 0.02μF feedback unit sets damping.

Figure 18 summarizes the capabilities of the power gain stages presented, and should be useful in selecting an approach for a given application.

FIGURE	VOLTAGE GAIN	CURRENT GAIN	FULL POWER BANDWIDTH	COMMENTS
1A	No	Yes, 150mA output	600kHz	Simple, easy.
1B	No	Yes, 150mA output	1.5MHz	Simple, easy.
2	No	Yes, 3A	100kHz	
3	No	Yes, 200mA	7.5MHz	Feedforward technique gives high bandwidth >1000V/μs slew. Inverting operation only.
5A, 5B	Yes	No	Depends on op amp	Simple stages allow wide swing, almost to rails.
7	Yes	Yes, 125mA	600kHz	High current, nearly rail-to-rail swing capability.
9	Yes, ±120V	Yes, 25mA	15kHz	Good, general purpose high voltage stage.
11	Yes, ±120V	Yes, 25mA	12kHz	Almost indestructable output.
13	Yes, +1000V	No	60Hz	High voltage output with no external high voltage supplies required. Limited bandwidth with assymetrical slewing. Positive outputs only.
15	Yes, ±100V	Yes, 150mA	150Hz	High voltage outputs with no external high voltage supplies. Limited bandwidth. Full bipolar output.

Figure 18. Summary of Circuit Characteristics

The Oscillation Problem (Frequency Compensation Without Tears)

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed power gain stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria, and can be used to predict stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; *local* and *loop* oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 7 furnishes an instructive example. The Q3-Q5 and Q4-Q6 pairs have high gain bandwidth. The intended resistive feedback loops allow them to oscillate in the 50-100MHz region without the 100pF-200Ω network shunting the DC feedback. This network rolls off gain-bandwidth, preventing oscillation. It is worth noting that a ferrite bead in series with the 2kΩ resistor will give similar results. In this case, the bead raises the inductance of the wire, attenuating high frequencies.

The photo in Figure B1 shows text Figure 7 following a bipolar squarewave input with the local high frequency RC compensation networks removed. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high F_t transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different F_t's to achieve stability. Emitter followers are notorious sources of oscillation, and should never be directly driven from low impedance sources.

Text Figure 5 uses an RC damper network from the 74C04 inverters to ground to eliminate local oscillations. In that circuit the 74C04's are forced to run in their linear region. Although their DC gain is low, bandwidth is high. Very small parasitic feedback terms result in high frequency oscillations. The damper network provides a low impedance to ground at high frequency, breaking up the unwanted feedback path.

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillaton. Loop oscillations are usually relatively low in frequency, typically 10Hz-1MHz.

A good way to eliminate loop caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain-bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives "too late." The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to "brute force" compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain-bandwidth. The feedback capacitor serves to trim step response only and should not be relied on to stop outright oscillation.

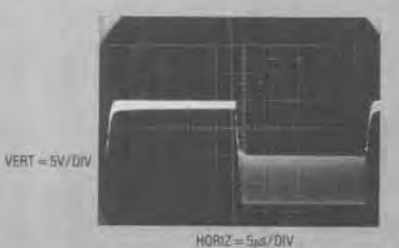
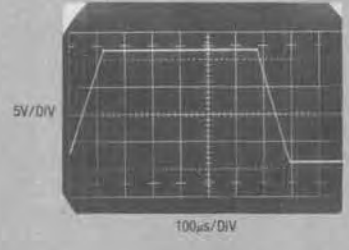


Figure B1. Typical Local Output Stage Oscillation

Figures B2 and B3 illustrate these issues. The 600kHz gain-bandwidth LT1012 amplifier used with the LT1010 current buffer produces the output shown in Figure B2. The LT1010's 20MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1012's internal roll-off is well below that of the output stage, and stability is achieved with no external compensation components. Figure B3 uses a 15MHz LT318A as the control amplifier. The associated photo shows the results. Here, the control amplifier's roll-off, close to the output stages, causes problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the LT318A's gain-bandwidth (see text Figure 1).

The fact that the slower op amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is "free". The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability.

Text Figure 9's high voltage stage is an interesting case. The high voltage transistors are very slow devices, and the LT1055 amplifier has a much higher gain-bandwidth than the output stage. The LT1055 is locally compensated by the 10k-100pF network, giving it an integrator-like response. This compensation, combined with the damping provided by the 33pF feedback capacitor, gives good loop response. The procedure used to compensate this circuit is typical of what is done to stabilize boosted amplifier loops and is worth reviewing.



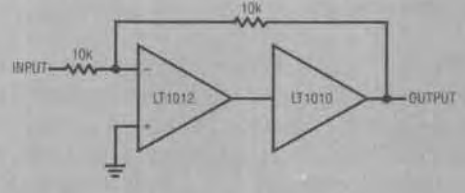
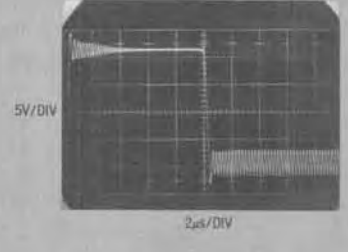


Figure B2. A Slow Control Amplifier Gives "Free" Loop Compensation



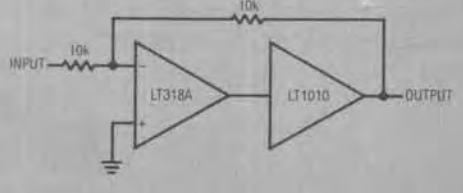


Figure B3. A Fast Control Amplifier Gives "Free" Loop Oscillation

With no compensation components installed, the circuit is turned on and oscillations are observed (photo, Figure B4). The relatively slow oscillation frequency suggests a loop oscillation problem. The LT1055 gain-bandwidth is degenerated with the RC components around the amplifier. The RC time constant is chosen to eliminate oscillations and give the best possible response (photo, Figure B5) with no loop feedback capacitor in place. Observe that the 1μs time constant selected offers significant attenuation at the oscillation frequency noted in the photo, Figure B4. Finally, the loop feedback capacitor (33pF) is selected to give the optimum damping shown in text Figure 10.

When making tests like these, remember to investigate the effects of various loads and output operating voltages. Sometimes a compensation scheme which appears fine gives bad results for some output conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

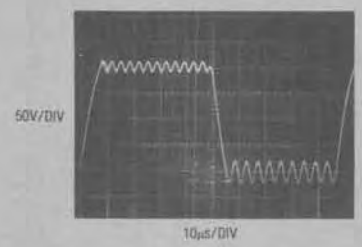


Figure B4. Oscillations After Slewing Suggest a Loop Problem

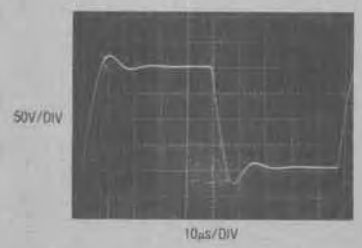


Figure B5. Control Amplifier Roll-Off Stabilizes B4's Problems

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