Appendix A

Single-Supply Circuit Collection

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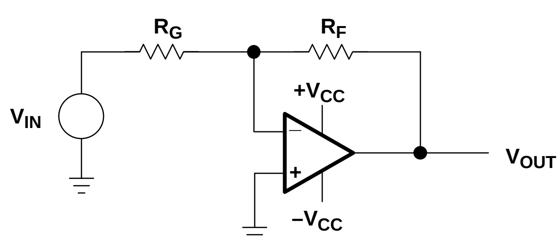
A.1 Introduction

Portable and single-supply electronic equipment is becoming more popular each day. The demand for single-supply op amp circuits increases with the demand for portable electronic equipment because most portable systems have one battery. Split- or dual-supply op amp circuit design is straightforward because op amp inputs and outputs are referenced to the normally grounded center tap of the supplies. In the majority of split-supply applications, signal sources driving the op amp inputs are referenced to ground, thus with one input of the op amp referenced to ground, as shown in Figure A–1, there is no need to consider input common-mode voltage problems.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_G} \qquad \text{A–1A}$$



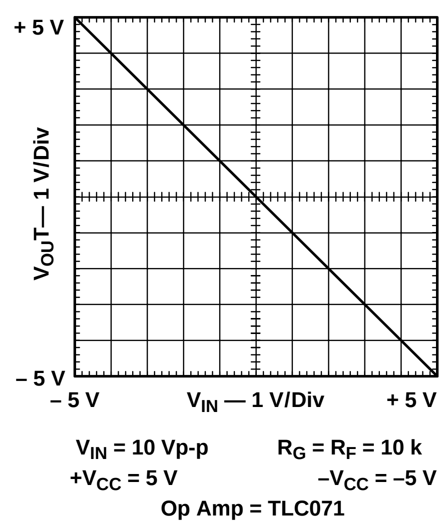


Figure A–1. Split-Supply Op Amp Circuit

When the signal source is not referenced to ground (see Figure A–2 and Equation A–1B), the voltage difference between ground and the reference voltage shows up amplified in the output voltage. Sometimes this situation is OK, but other times the difference voltage must be stripped out of the output voltage.

$$V_{OUT} = -\left(V_{IN} + V_{REF}\right)\frac{R_F}{R_G} \qquad \text{A–1B}$$

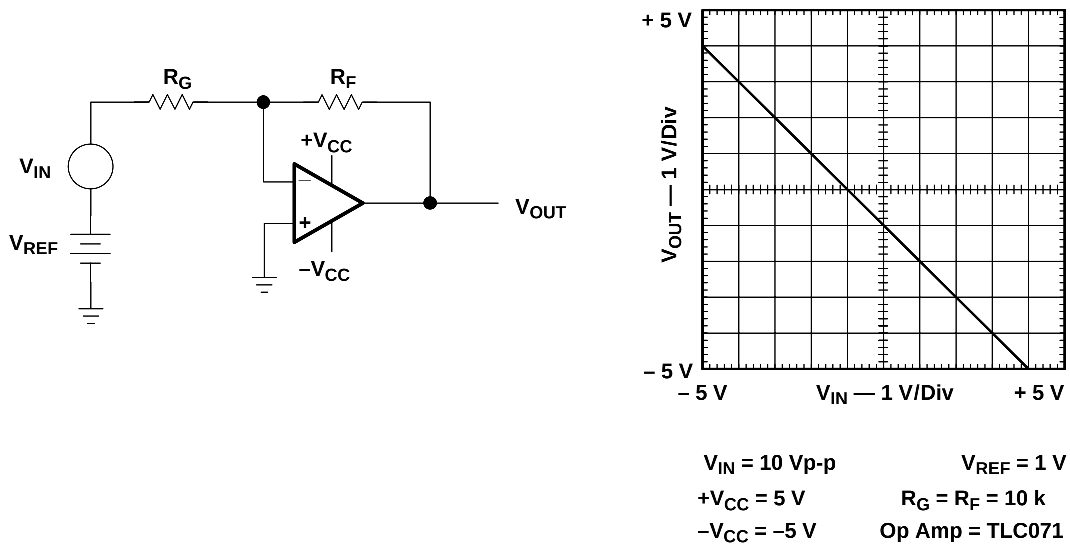


Figure A–2. Split-Supply Op Amp Circuit With Reference Voltage Input

An input bias voltage is used to eliminate the difference voltage when it must not appear in the output voltage (see Figure A–3 and Equation A–1C). The voltage, V_{REF}, is in both input circuits, hence it is named a common-mode voltage. Voltage-feedback op amps, like those used in this document, reject common-mode voltages because their input circuit is constructed with a differential amplifier (chosen because it has natural common-mode voltage rejection capabilities).

$$V_{OUT} = -\left(V_{IN} + V_{REF}\right)\frac{R_F}{R_G} + V_{REF}\left(\frac{R_F}{R_F + R_G}\right)\left(\frac{R_F + R_G}{R_G}\right) = -V_{IN}\frac{R_F}{R_G} \qquad \text{A–1C}$$

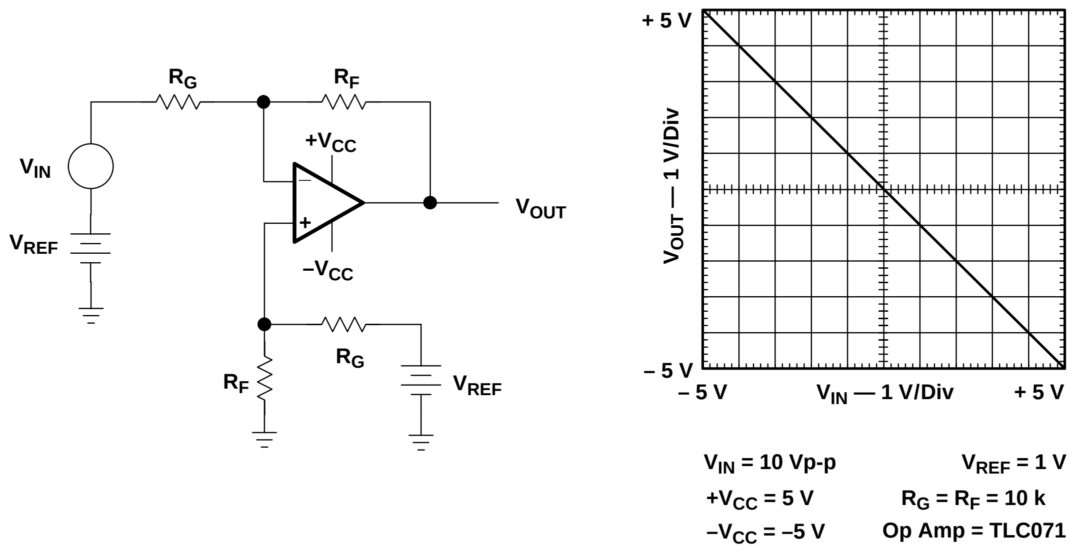


Figure A–3. Split-Supply Op Amp Circuit With Common-Mode Voltage

When signal sources are referenced to ground, single-supply op amp circuits always have a large input common-mode voltage. Figure A–4 shows a single-supply op amp circuit that has its input voltage referenced to ground. The input voltage is not referenced to the midpoint of the supplies like it would be in a split-supply application, rather it is referenced to the lower power supply rail. This circuit malfunctions when the input voltage is positive because the output voltage would have to go negative — hard to do with a positive supply. It operates marginally with small negative input voltages because most op amps do not function well when the inputs are connected to the supply rails.

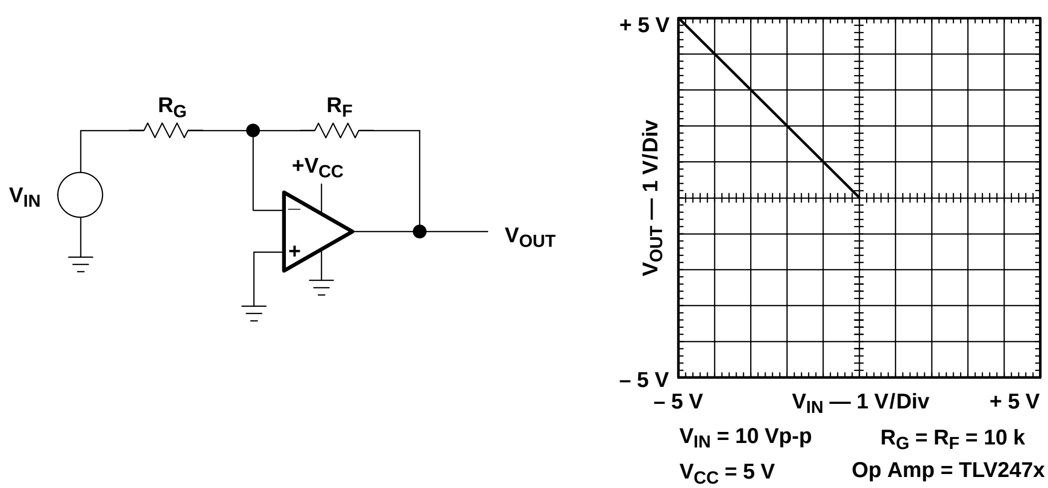


Figure A–4. Single-Supply Op Amp Circuit

The constant requirement to account for inputs connected to ground or other reference voltages makes it difficult to design single-supply op amp circuits. This appendix presents a collection of single-supply op amp circuits, including their description and transfer equation. Those without a good working knowledge of op amp equations should reference the *Understanding Basic Analog* series of application notes available from Texas Instruments. Application note SLAA068, *Understanding Basic Analog — Ideal Op Amps* develops the ideal op amp equations. Circuit equations in this appendix are written with the ideal op amp assumptions as specified in *Understanding Basic Analog — Ideal Op Amps.* The assumptions appear in Table A–1 for easy reference.

Table A–1. Ideal Op Amp Assumptions

PARAMETER NAME	PARAMETER SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Op amp gain	a	∞

Detailed information about designing single-supply op amp circuits appears in application note SLOA030, *Single-Supply Op Amp Design Techniques*. Unless otherwise specified, all op amp circuits shown here are single-supply circuits. The single supply may be wired with the negative or positive lead connected to ground, but as long as the supply polarity is correct, the wiring does not affect circuit operation.

A.2 Boundary Conditions

All op amps are constrained to output voltage swings less than or equal to their power supply. Use of a single supply limits the output voltage to the range of the supply voltage. For example, when the supply voltage V_{CC} equals +10 V, the output voltage is limited to the range $0 \le V_{OUT} \le 10$. This limitation precludes negative output voltages when the circuit has a positive supply voltage, but it does not preclude negative input voltages. As long as the voltage on the op amp input leads does not become negative, the circuit can handle negative voltages applied to the input resistors.

Beware of working with negative (positive) input voltages when the op amp is powered from a positive (negative) supply because op amp inputs are highly susceptible to reverse-voltage breakdown. Also, ensure that no *start-up* condition reverse biases the op amp inputs when the input and supply voltage are opposite polarity. It may be advisable to protect the op amp inputs with a diode (Schottky or germanium) connected anode to ground and cathode to the op amp input.

A.3 Amplifiers

Many types of amplifiers can be created using op amps. This section consists of a selection of some basic, single-supply op amp circuits that are available to the designer during the concept stage of a design. The circuit configuration and correct single-supply dc biasing techniques are presented for the following cases: inverting, noninverting, differential, T-network, buffer and ac-coupled amplifiers.

A.3.1 Inverting Op Amp with Noninverting Positive Reference

The ideal transfer equation is given in Equation A–1.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_G} + V_{REF}\left(\frac{R_F + R_G}{R_G}\right) \qquad \text{A–1}$$

The transfer equation for this circuit (Figure A–5) takes the form of Y = –mX + b. The transfer function slope is negative, and the dc intercept is positive. R_F and R_G are contained in both halves of the equation, thus it is hard to obtain the desired slope and dc intercept without modifying V_{REF}. This is the minimum component count configuration for this transfer function. When the reference voltage is 0, the input voltage is constrained to negative voltages because positive input voltages would cause the output voltage to saturate at ground.

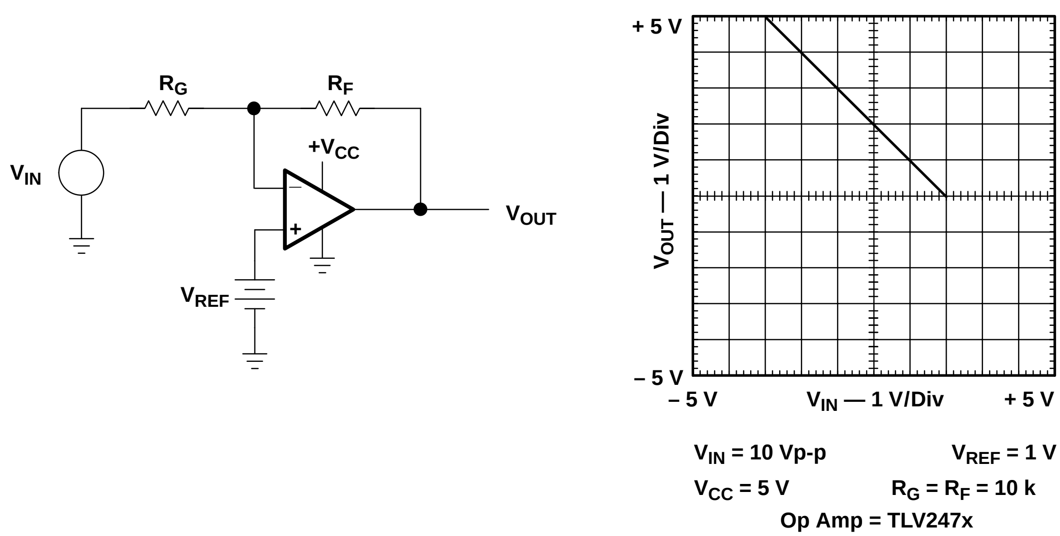


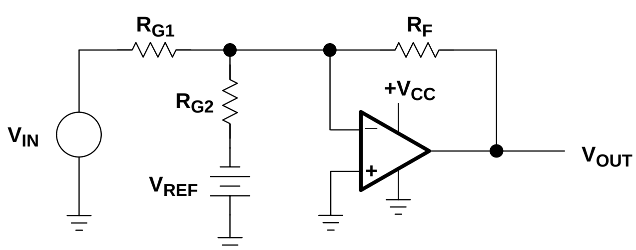
Figure A–5. Inverting Op Amp with Noninverting Positive Reference

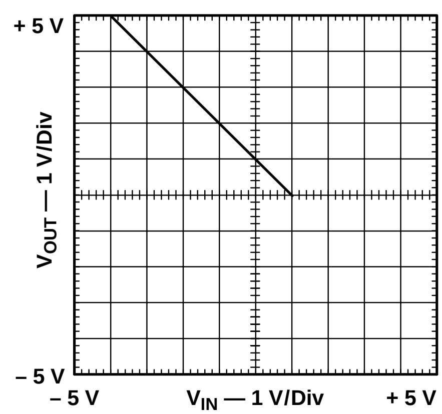
A.3.2 Inverting Op Amp with Inverting Negative Reference

The transfer equation takes the form of Y = –mX + b and is given in Equation A–2.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_{G1}} + V_{REF}\frac{R_F}{R_{G2}} \qquad \text{A–2}$$

The transfer function slope is negative, and the dc intercept is positive (Figure A–6). R_{G1} and R_{G2} are contained in the equation, thus it is easy to obtain the desired slope and dc intercept by adjusting the value of both resistors. Because of the virtual ground at the inverting input, R_{G2} is the terminating impedance for V_{REF}. When the reference voltage is 0, the input voltage is constrained to negative voltages because positive input voltages would cause the output voltage to saturate at ground.





V_{IN} = 10 Vp-p $\quad V_{REF}$ = –1 V

V_{CC} = 5 V $\quad R_{G1} = R_{G2} = R_F$ = 10 k

Op Amp = TLV247x

Figure A–6. Inverting Op Amp with Inverting Negative Reference

A.3.3 Inverting Op Amp with Noninverting Negative Reference

The transfer equation takes the form of Y = –mX – b and is given in Equation A–3.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_G} - V_{REF}\left(\frac{R_F + R_G}{R_G}\right) \qquad \text{A–3}$$

The transfer function slope is negative, and the dc intercept is negative. R_F and R_G are contained in both halves of the equation, thus it is hard to obtain the desired slope and dc intercept without modifying V_{REF}. This is the minimum component count configuration for this transfer function. The slope and dc intercept terms in Equation A–3 are both negative, hence, unless the correct input voltage range is selected, the output voltage will saturate at ground. The negative input voltage must be limited to less than –400 mV because op amp inputs either break down or have protection circuits that forward bias when large negative voltages are applied to the inputs.

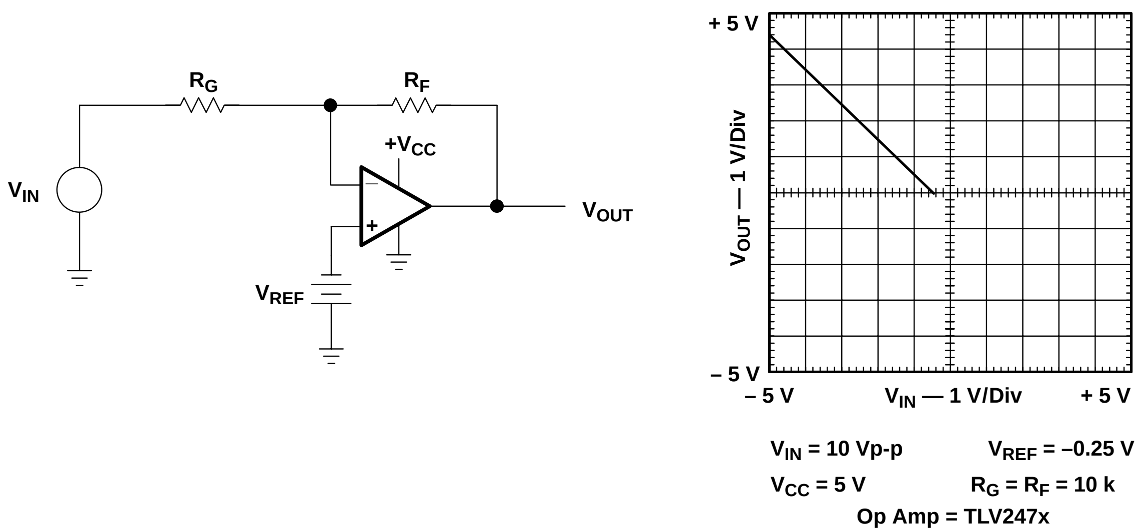


Figure A–7. Inverting Op Amp with Noninverting Negative Reference

A.3.4 Inverting Op Amp with Inverting Positive Reference

The transfer equation takes the form of Y = –mX – b and is given in Equation A–4.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_{G1}} - V_{REF}\frac{R_F}{R_{G2}} \qquad \text{A–4}$$

The transfer function slope is negative, and the dc intercept is negative. R_{G1} and R_{G2} are contained in the equation, thus it is easy to obtain the desired slope and dc intercept by adjusting the value of both resistors. Because of the virtual ground at the inverting input, R_{G2} is the terminating impedance for V_{REF}. The slope and dc intercept terms in Equation A–4 are both negative, hence, unless the correct input voltage range is selected, the output voltage will saturate.

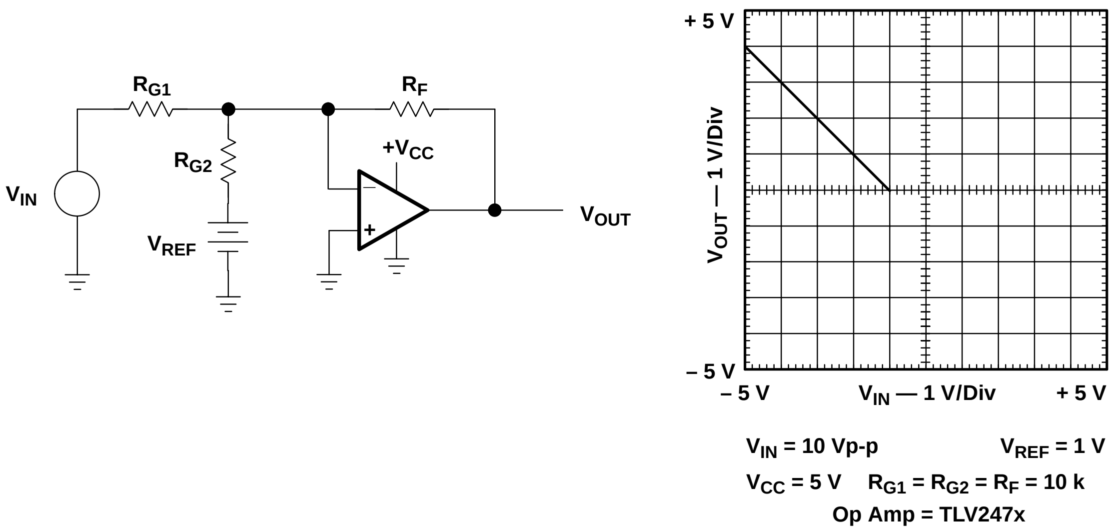


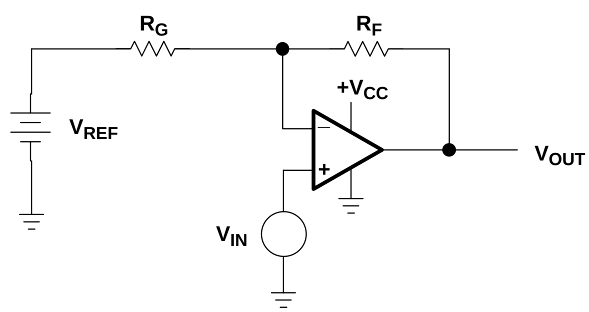
Figure A–8. Inverting Op Amp with Inverting Positive Reference

A.3.5 Noninverting Op Amp with Inverting Positive Reference

The transfer equation takes the form of Y = mX – b and is given in Equation A–5.

$$V_{OUT} = V_{IN}\frac{R_F + R_G}{R_G} - V_{REF}\frac{R_F}{R_G} \qquad \text{A–5}$$

The transfer function slope is positive, and the dc intercept is negative. This is the minimum component count configuration for this transfer function. The reference termination resistor is connected to a virtual ground, so R_G is the load across V_{REF}. R_F and R_G are contained in both halves of the equation, thus it is hard to obtain the desired slope and dc intercept without modifying V_{REF} or placing an attenuator in series with V_{IN}.



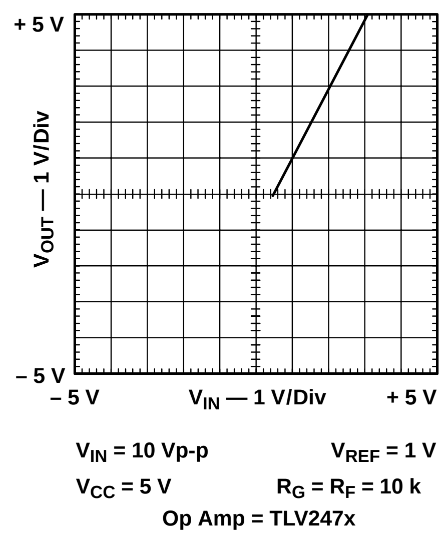


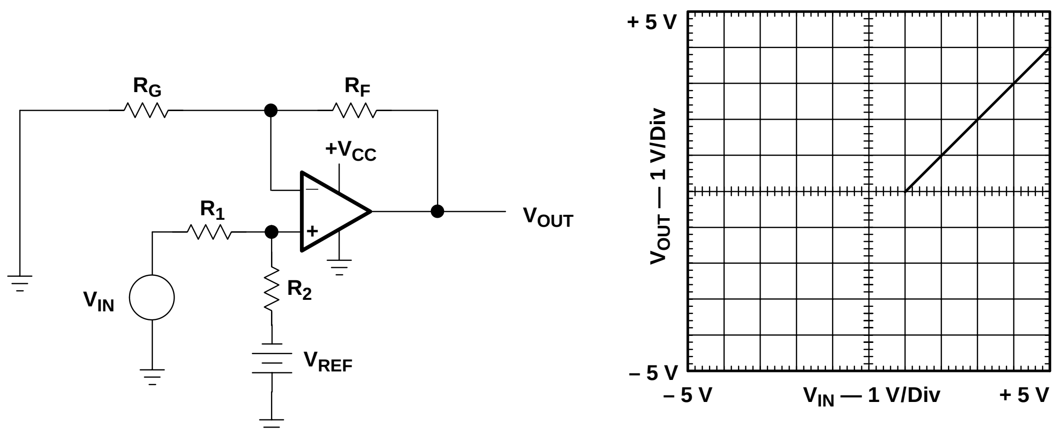
Figure A–9. Noninverting Op Amp with Inverting Positive Reference

A.3.6 Noninverting Op Amp with Noninverting Negative Reference

The transfer equation takes the form of Y = mX – b and is given in Equation A–6.

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\frac{R_F + R_G}{R_G} - V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\frac{R_F + R_G}{R_G} \qquad \text{A–6}$$

The transfer function slope is positive, and the dc intercept is negative. The reference is terminated in R_1 and R_2. R_1 and R_2 can be selected independent of R_F and R_G to obtain the desired slope and dc intercept. The price for the extra degree of freedom is two resistors.



V_{IN} = 10 Vp-p **V_{REF} = –1 V**
V_{CC} = 5 V **Op Amp = TLV247x**
$R_1 = R_2 = R_G = R_F$ = 10 k

Figure A–10. Noninverting Op Amp with Noninverting Negative Reference

A.3.7 Noninverting Op Amp with Inverting Negative Reference

The transfer equation takes the form of Y = mX + b and is given in Equation A–7.

$$V_{OUT} = V_{IN}\frac{R_F + R_G}{R_G} + V_{REF}\frac{R_F}{R_G} \qquad \text{A–7}$$

The transfer function slope is positive, and the dc intercept is positive. This is the minimum component count configuration for this transfer function. The reference termination resistor is connected to a virtual ground, so R_G is the load across V_{REF}. R_F and R_G are contained in both halves of the equation. Thus it is hard to obtain the desired slope and dc intercept without modifying V_{REF} or placing an attenuator in series with V_{IN}.

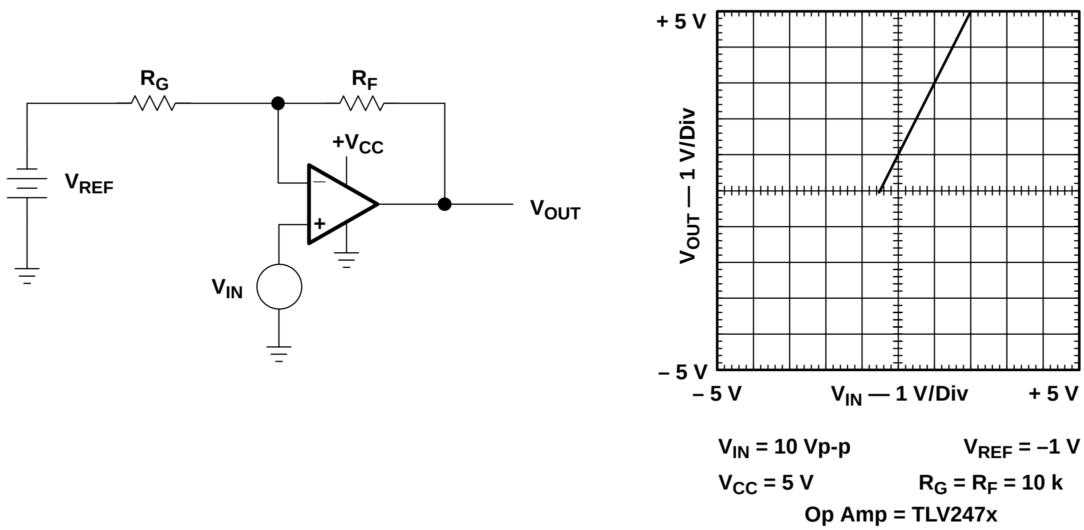


Figure A–11. Noninverting Op Amp with Inverting Positive Reference

A.3.8 Noninverting Op Amp with Noninverting Positive Reference

The transfer equation takes the form of Y = mX + b and is given in Equation A–8.

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\frac{R_F + R_G}{R_G} + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\frac{R_F + R_G}{R_G} \qquad \text{A–8}$$

The transfer function slope is positive, and the dc intercept is positive. The reference is terminated in R_1 and R_2. R_1 and R_2 can be selected independent of R_F and R_G to obtain the desired slope and dc intercept. The price for the extra degree of freedom is two resistors.

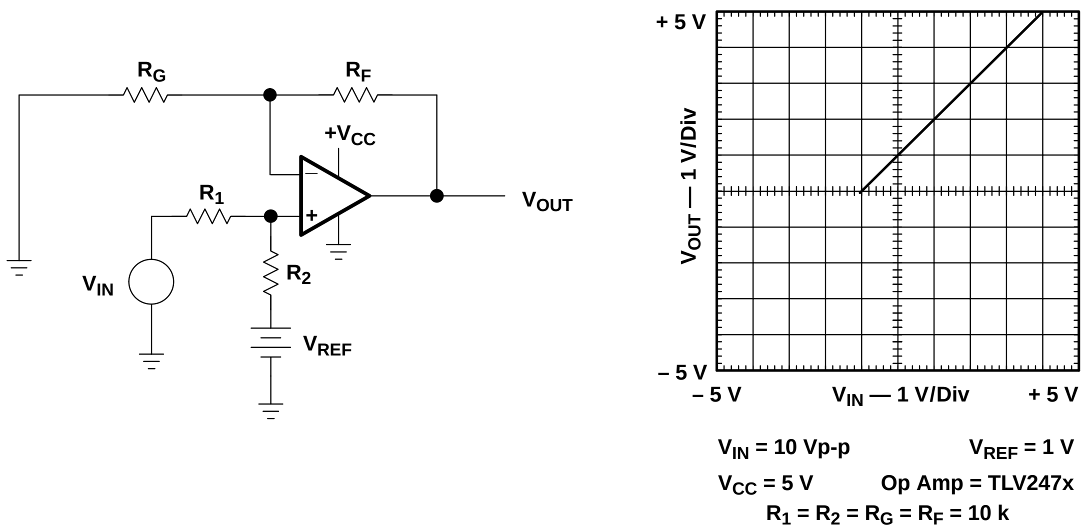


Figure A–12. Noninverting Op Amp with Noninverting Positive Reference

A.3.9 Differential Amplifier

When R_F is set equal to R_2 and R_G is set equal to R_1, Equation A–9 reduces to Equation A–10.

$$V_{OUT} = V_{IN2}\,\frac{R_F + R_G}{R_G}\left(\frac{R_2}{R_1 + R_2}\right) - V_{IN1}\,\frac{R_F}{R_G} \qquad \text{A–9}$$

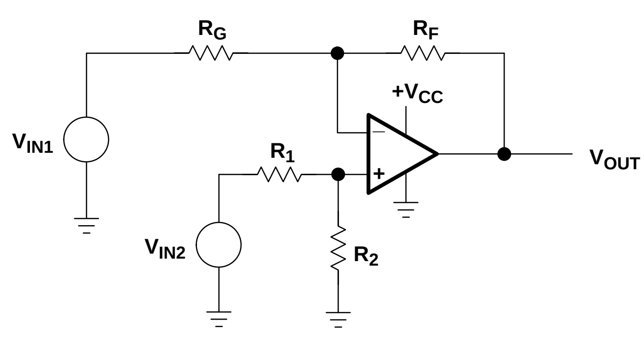
$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\frac{R_F}{R_G} \qquad \text{A–10}$$

These resistors must be matched very closely to obtain good differential performance. The mismatch error in these resistors reduces the common-mode performance, and the mismatch shows up in the output as an amplified common-mode voltage.

Consider Equation A–10. Note that only the difference signal is amplified, thus this configuration is called a differential amplifier. The differential amplifier is a popular circuit in precision applications where it is used to amplify sensor outputs while rejecting common-mode noise.

The inverting input impedance is R_G because of the virtual ground at the inverting op amp input. The noninverting input impedance is $R_F + R_G$ because the noninverting op amp input impedance approaches infinity. The two input impedances are different, and this leads to two problems with this circuit.

First, mismatched input impedances preclude any attempts to cancel input bias currents through resistor matching. Often R_2 is set equal to $R_F \| R_G$ so that the bias currents develop equal common-mode voltages which the op amp rejects. This is not possible when $R_2 = R_F$ and $R_1 = R_G$ unless the source impedances are matched. Second, high output impedance sensors are often used, and when high output sensors work into mismatched input impedances, errors occur.



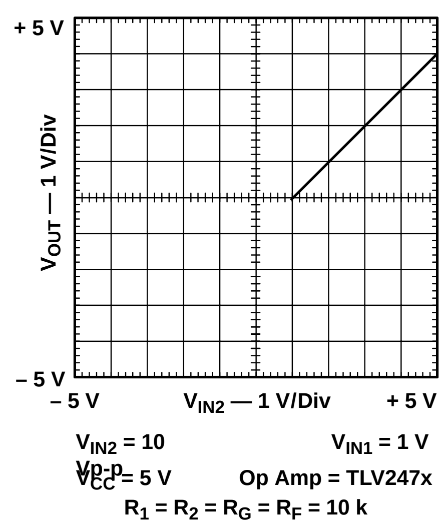


Figure A–13. Differential Amplifier

A.3.10 Differential Amplifier With Bias Correction

When R_F is set equal to R_2 and R_G is set equal to R_1, Equation A–11 reduces to Equation A–12.

$$V_{OUT} = V_{IN2}\,\frac{R_F + R_G}{R_G}\left(\frac{R_2}{R_1 + R_2}\right) + V_{REF}\,\frac{R_F + R_G}{R_G}\left(\frac{R_1}{R_1 + R_2}\right) - V_{IN1}\,\frac{R_F}{R_G} \qquad \text{A–11}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\frac{R_F}{R_G} + V_{REF} \qquad \text{A–12}$$

When an offset voltage must be eliminated from or added to the input signal, this differential amplifier circuit is employed. The reference voltage can be positive or negative depending upon the polarity offset required, but care must be taken to protect the op amp inputs and not exceed the output range.

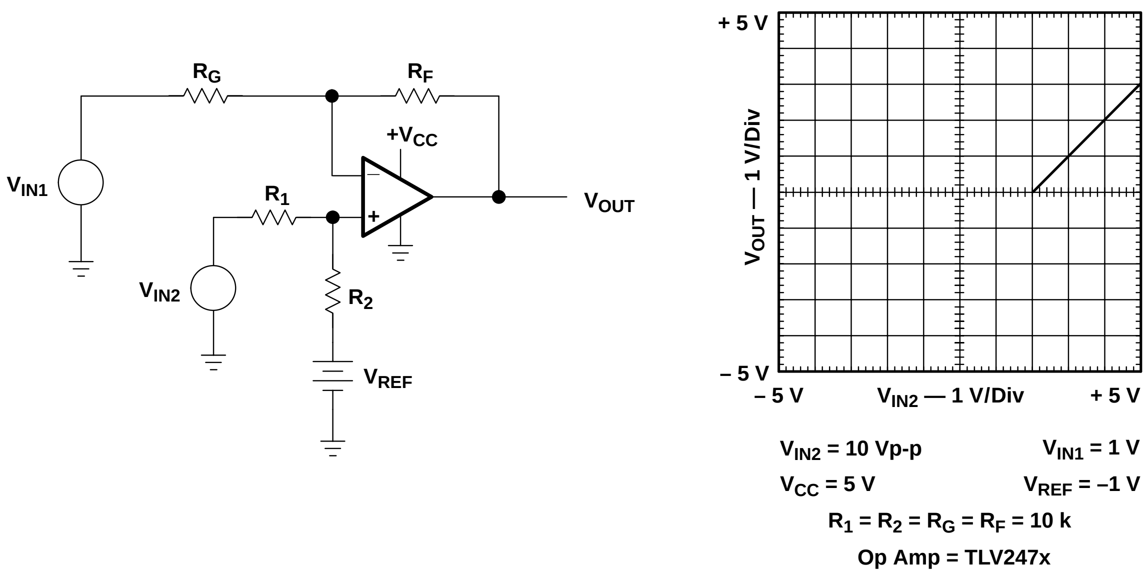


Figure A–14. Differential Amplifier with Bias Correction

A.3.11 High Input Impedance Differential Amplifier

When R_F is set equal to R_1 and R_G is set equal to R_2, Equation A–13 reduces to Equation A–14.

$$V_{OUT} = V_{IN1}\frac{R_1 + R_2}{R_1}\left(-\frac{R_F}{R_G}\right) + V_{IN2}\frac{R_F + R_G}{R_G} \qquad \text{A–13}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\frac{R_F + R_G}{R_G} \qquad \text{A–14}$$

Each input signal is connected to an op amp noninverting input that is very high impedance. The input impedance of the circuit is very high, and it is matched, so this circuit is often used to interface to high-impedance sensors. Each op amp has a signal propagation time, and V_{IN1} experiences two propagation delays versus V_{IN2}'s one propagation delay. At high frequencies, the propagation delay becomes a significant portion of the signal period, and this configuration is not usable at that frequency.

R_F and R_2, and R_G and R_1 should be matched to achieve good common-mode rejection capability. Bias current cancellation resistors equal to R_F || R_G should be connected in series with the input sources for precision applications.

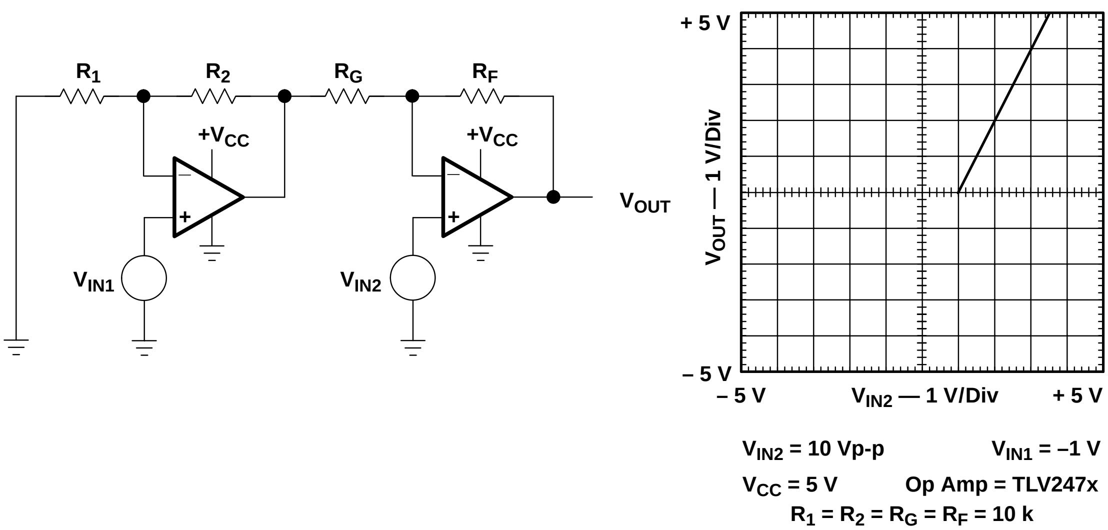


Figure A–15. High Input Impedance Differential Amplifier

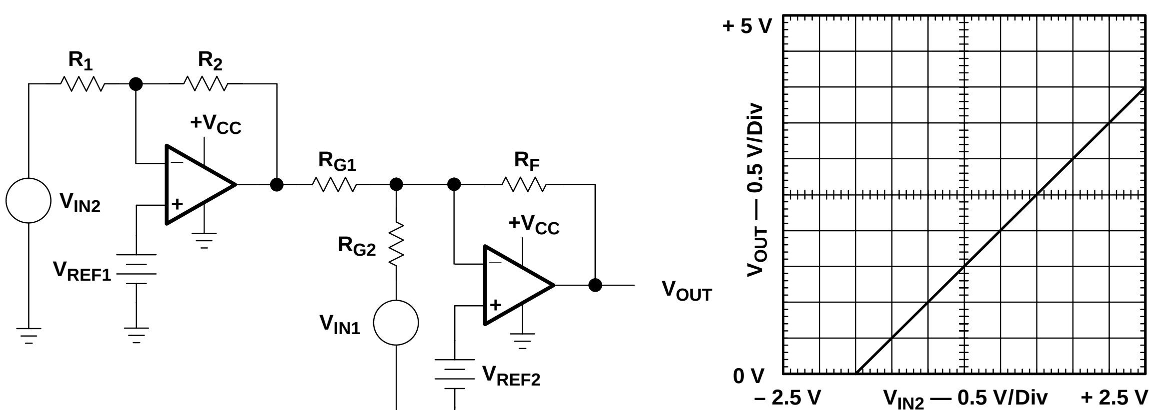
A.3.12 High Common-Mode Range Differential Amplifier

When all resistors are equal, Equation A–15 reduces to Equation A–16.

$$V_{OUT} = V_{IN2}\left(-\frac{R_2}{R_1}\right)\left(-\frac{R_F}{R_{G1}}\right) + V_{REF1}\left(\frac{R_1 + R_2}{R_1}\right)\left(-\frac{R_F}{R_{G1}}\right) + V_{IN1}\left(-\frac{R_F}{R_{G2}}\right) + V_{REF2}\left(\frac{R_F + R_{G1} \parallel R_{G2}}{R_{G1} \parallel R_{G2}}\right) \qquad \text{A–15}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right) - 2V_{REF1} + 3V_{REF2} \qquad \text{A–16}$$

R_1 and R_{G2} are equal-value resistors terminated into a virtual ground, hence, the input sources are equally terminated. This configuration has high common-mode capability because R_1 and R_{G2} limit the current that can flow into or out of the op amp. Thus, the input voltage can rise to any value that does not exceed the op amp's drive capability. The voltage references, V_{REF1} and V_{REF2}, are added for bias purposes. Without bias, the output voltage of the op amps would saturate at ground, and the bias voltages keep the output voltage of the op amp positive.



V_{IN1} = 1 V　　V_{IN2} = 5 Vp-p
V_{REF1} = 1.25 V　　V_{REF2} = 1.67 V
V_{CC} = 5 V　　Op Amp = TLV247x
$R_1 = R_2 = R_F = R_{G1} = R_{G2}$ = 10 k

Figure A–16. High Common-Mode Range Differential Amplifier

A.3.13 High-Precision Differential Amplifier

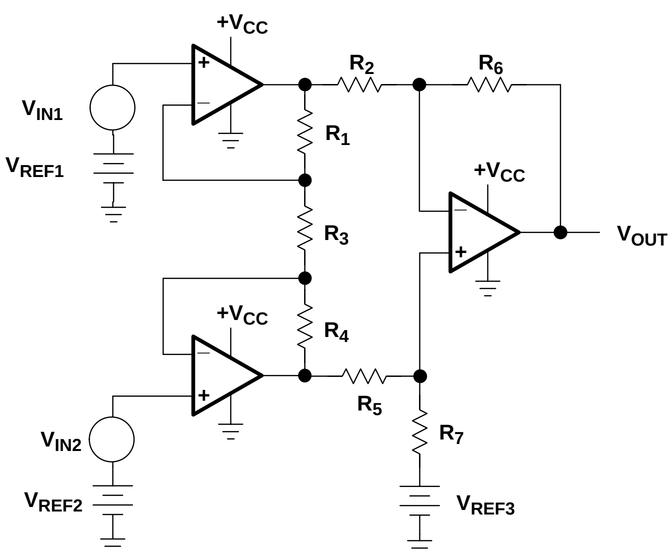
When $R_7 = R_6$, $R_5 = R_2$, $R_1 = R_4$, and $V_{REF1} = V_{REF2}$, Equation A–17 reduces to Equation A–18.

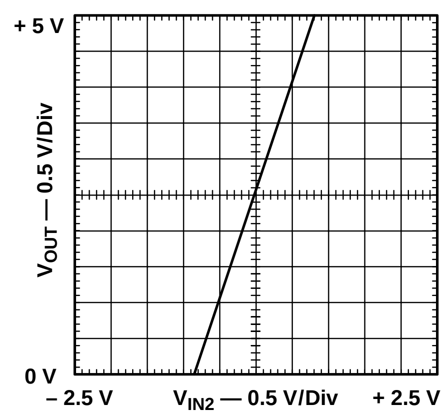
$$V_{OUT} = \left(V_{IN2} + V_{REF2}\right)\left(\frac{2R_4 + R_3}{R_3}\right)\left(\frac{R_7}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right) - \left(V_{IN1} + V_{REF1}\right)\left(\frac{2R_1 + R_3}{R_3}\right)\frac{R_6}{R_2} + V_{REF3}\left(\frac{R_5}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right) \quad \text{A–17}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\left(\frac{2R_1}{R_3} + 1\right)\left(\frac{R_6}{R_2}\right) + V_{REF3} \quad \text{A–18}$$

In this circuit configuration, both sources work into the input impedance of a noninverting op amp. This impedance is very high, and if the op amps are identical, both impedances are very nearly equal. The propagation delay is still equal to two op amp propagation delays, but the propagation delay is very nearly equal, so any distortion resulting from unequal propagation delays is minimized.

The equal resistors should be matched with more precision than is expected from the circuit. Resistor matching eliminates distortion due to unequal gains, and it reduces the common-mode voltage feed through. Resistors equal to $(R_1 \parallel R_3)/2$ may be placed in series with the sources to reduce errors resulting from bias currents. This differential amplifier has the unique feature that the gain can be changed with only one resistor, and if the gain setting resistor is R3, no resistor matching is required to change gain.





V_{IN1} = 2.5 V, V_{REF1} = 2.5 V, V_{CC} = 5 V, V_{IN2} = 5 Vp-p, V_{REF2} = 2.5 V, V_{REF3} = 2.5 V

$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7$ = 10 k

Op Amp = TLV247x

Figure A–17. High-Precision Differential Amplifier

A.3.14 Simplified High-Precision Differential Amplifier

When R_F is set equal to R_2, R_G is set equal to R_1, and $V_{REF1} = V_{REF2}$, Equation A–19 reduces to Equation A–20.

$$V_{OUT} = \left(V_{IN2} + V_{REF2}\right)\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) - \left(V_{IN1} + V_{REF1}\right)\left(\frac{R_F}{R_G}\right) + V_{REF3}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \qquad \text{A–19}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\left(\frac{R_F}{R_G}\right) + V_{REF3} \qquad \text{A–20}$$

Both input sources are loaded equally with very high impedances in the simplified high precision differential amplifier. This configuration eliminates three resistors, two of which are matched, but it sacrifices flexibility in gain setting capability because the gain must be set with a matched pair of resistors.

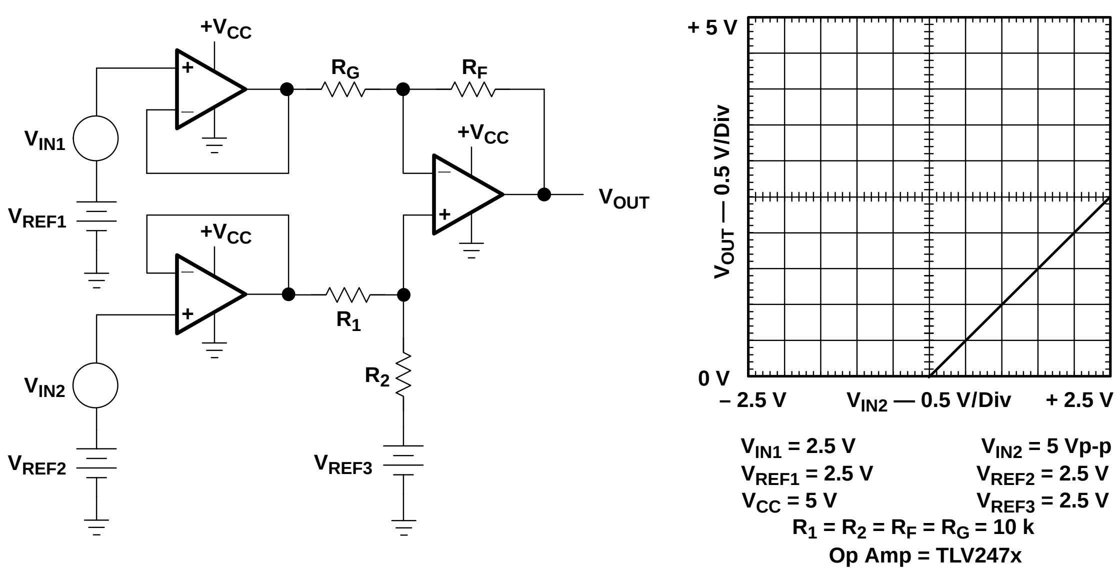


Figure A–18. Simplified High-Precision Differential Amplifier

A.3.15 Variable Gain Differential Amplifier

When R_1 is set equal to R_3 and R_2 is set equal to R_4, Equation A–21 reduces to Equation A–22.

$$V_{OUT} = V_{IN1}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right)\left(\frac{R_G}{R_F}\right) - V_{IN2}\left(\frac{R_4}{R_3}\right)\left(\frac{R_G}{R_F}\right) \qquad \text{A–21}$$

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\left(\frac{R_4}{R_3}\right)\left(\frac{R_F}{R_G}\right) \qquad \text{A–22}$$

When a function is enclosed in a feedback loop, the function acts inverted on the closed loop transfer function. Thus, the gain stage R_F/R_G ends up being an attenuator. The circuit shown in Figure A–19 can be used with any of the differential amplifiers to change gain without affecting matched resistors. R_1, R_3 and R_2, R_4 must be matched to reduce the common-mode voltage.

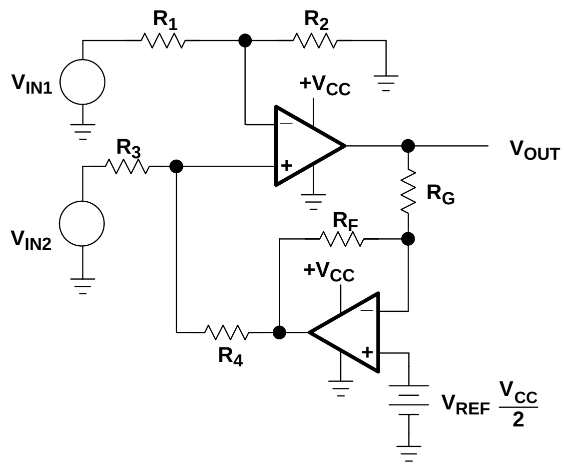


Figure A–19. Variable Gain Differential Amplifier

A.3.16 *T* Network in the Feedback Loop

Sometimes it is desirable to have a low-resistance path to ground in the feedback loop. Standard inverting op amps cannot do this when the driving circuit sets the input resistor value and the gain specification sets the feedback resistor value. Inserting a *T* network in the feedback loop yields a degree of freedom that enables both specifications to be met with a low dc resistance path to ground in the feedback loop.

$$V_{OUT} = -V_{IN}\left(\frac{R_2 + R_3 + \frac{R_2R_3}{R_4}}{R_1}\right) + V_{REF}\left(1 + \frac{R_2 + R_3 + \frac{R_2R_3}{R_4}}{R_1}\right) \quad \text{A–23}$$

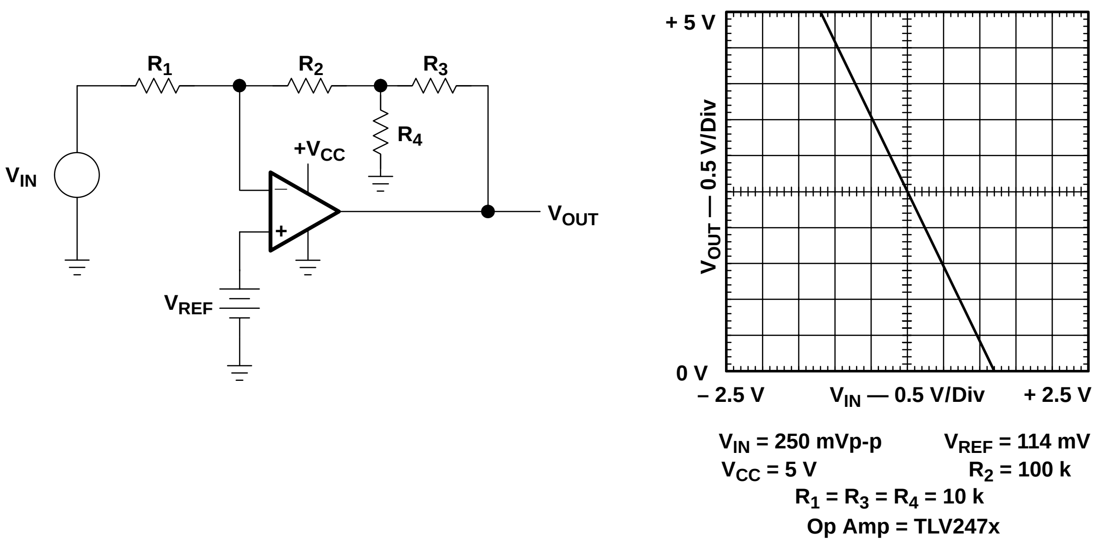


Figure A–20. T Network in the Feedback Loop

A.3.17 Buffer

The buffer input signal polarity must be unipolar because the output voltage swing is unipolar. When this limitation precludes the buffer, a differential amplifier with the negative input correctly biased is used, or a reference voltage is added to the buffer to offset the output voltage. R_F must be included when the op amp inputs are not rated for the full supply voltage. In that case, R_F limits the current into the op amp inputs, thus preventing latch up. Most new op amp inputs can withstand the full supply voltage, so they often leave R_F out as cost savings. The main attraction of the buffer is that it has very high input impedance and very low output impedance. The impedance transformation capability is why buffers are often added to the input of other circuits.

$$V_{OUT} = V_{IN} + V_{REF} \quad \text{A–24}$$

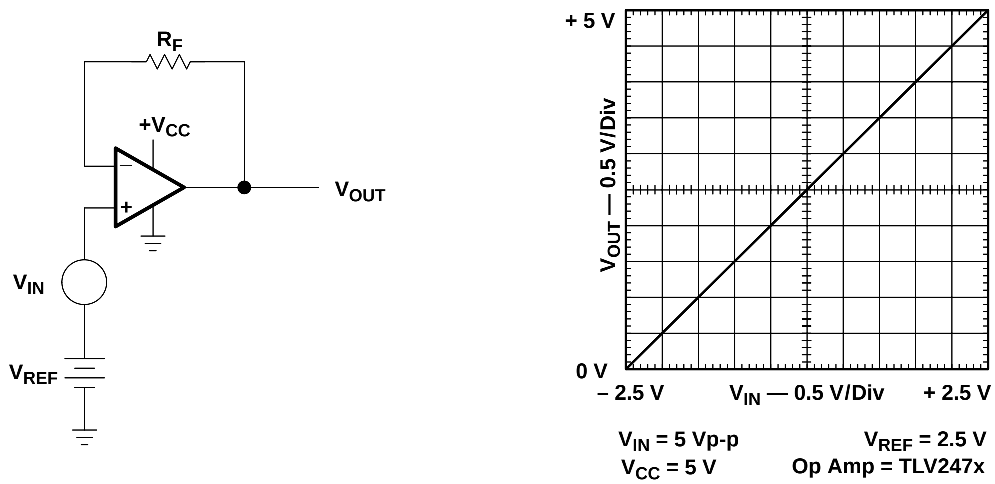


Figure A–21. Buffer

A.3.18 Inverting AC Amplifier

V_{CC} and resistors R set a dc level of $V_{CC}/2$ at the inverting input. R_G is connected to ground through a capacitor, thus the circuit functions as a buffer for dc. This causes the dc output voltage to be $V_{CC}/2$, so the quiescent output voltage is the middle of the supply voltage, and it is ready to swing to either rail as the input signal commands.

The ac gain is given in Equation A–25. R_G and C form a coupling network for the ac signal. Good coupling networks should be constant low impedance at the signal frequencies, so Equation A–26 should be satisfied to get good low-frequency performance. The lowest frequency component of the input signal, f_{MIN}, is determined by completing a Fourier series on the input signal. Then, setting f_{MIN} = 100f in Equation A–26 ensures that the 3-dB breakpoint introduced by R_G and C is two decades lower than f_{MAX}.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_G} + \frac{V_{CC}}{2} \qquad \text{A–25}$$

$$f = \frac{1}{200\pi R_G C} \qquad \text{A–26}$$

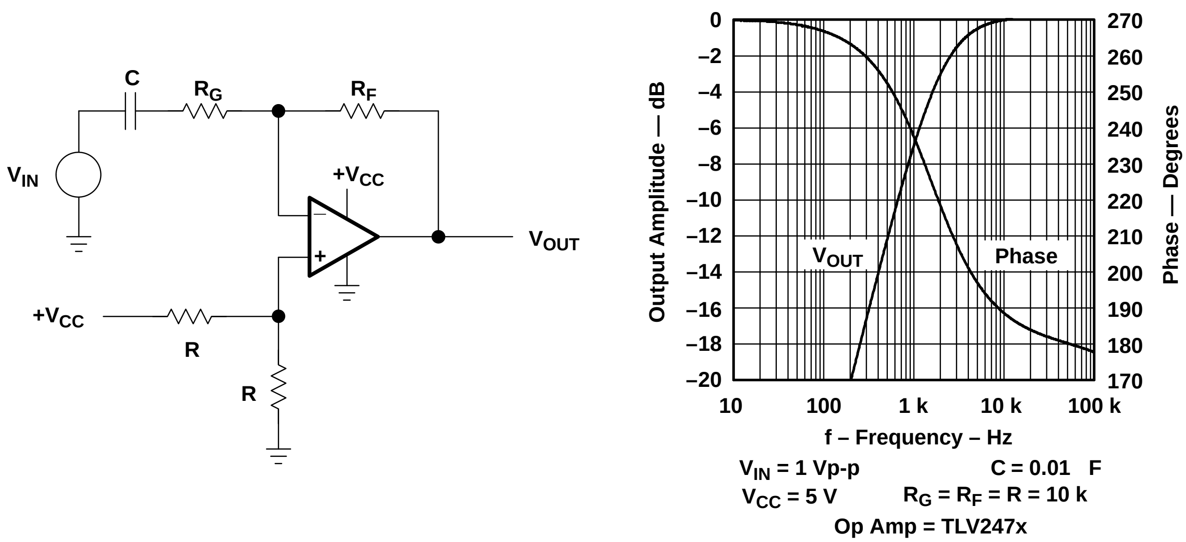


Figure A–22. Inverting AC Amplifier

A.3.19 Noninverting AC Amplifier

V_{CC} and the resistors (R) set a dc level of $V_{CC}/2$ at the inverting input. R_G is connected to ground through a capacitor, thus the circuit functions as a buffer for dc. This causes the dc output voltage to be $V_{CC}/2$, so the quiescent output voltage is the middle of the supply voltage, and it is ready to swing to either rail as the input signal commands.

The ac gain is given in Equation A–27. R_G and C create a coupling network for the ac signal. Good coupling networks should be a constant low impedance at the signal frequencies, so Equation A–28 should be satisfied to get good low frequency performance. The lowest frequency component of the input signal, f_{MIN}, is determined by completing a Fourier series on the input signal. Then, setting f_{MIN} = 100f in Equation A–28 ensures that the 3-dB breakpoint introduced by R_G and C is two decades lower than f_{MAX}. The breakpoint for R_G and C_1 is set in a similar manner.

$$V_{OUT} = V_{IN}\frac{R_F + R_G}{R_G} + \frac{V_{CC}}{2}\left(\frac{R_F + R_G}{R_G}\right) \qquad \text{A–27}$$

$$f = \frac{1}{200\pi R_G C} \qquad \text{A–28}$$

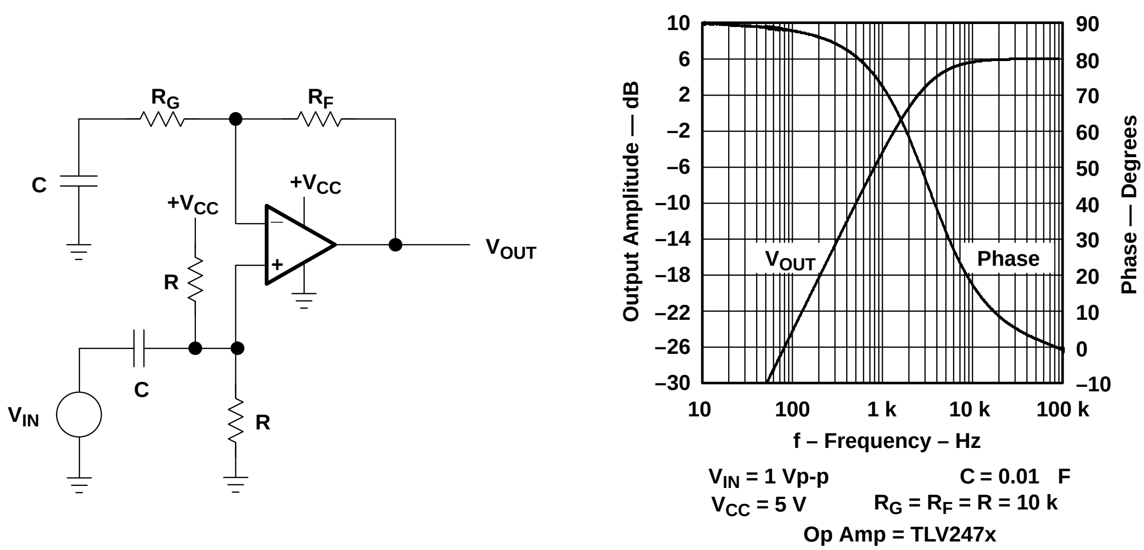


Figure A–23. Noninverting AC Amplifier