# LOCK-IN AMPLIFIER USES SINGLE IC

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The circuit of Figure 1, which combines a synchronous filter with a phase detector, will detect a modulated signal buried in noise. The dc output is proportional to the modulated signal, while the underlying component of noise is smoothed by the RC filter. Although the technique has been used before, the circuit described here uses a single IC instrumentation amplifier (in this case, the AD520†). The circuit was developed for multi-channel radiometry, where economical circuitry and high performance are a desirable combination, but it should find application in many fields where signal-in-noise detection is required.

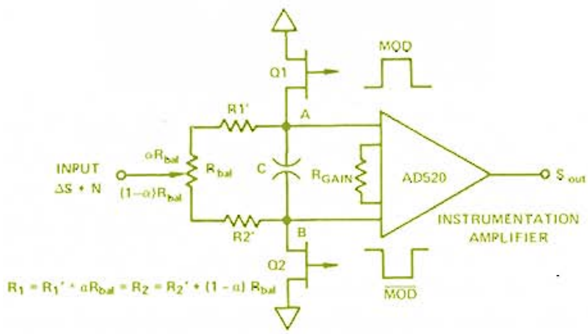


Figure 1. Synchronous demodulator

The operation of the circuit is illustrated in Figure 2. During the first half-cycle, FET Q1 is on and grounds the capacitor at A; at the same time, Q2 is off and presents a high impedance to the capacitor at B. The capacitor starts to charge up positively on the time constant $R_1C$. In the next half-cycle, the situation is reversed – Q2 is grounded and Q1 is open, the capacitor retains its previous charge and continues to charge negatively at B on the time constant $T = R_2C$, $(R_1 \cong R_2)$. In this way, the capacitor charges up to average value $\pm\Delta S/4$, which is differentially amplified to give $G_0\Delta S/2$ at the output. Only a signal which is coherent with the reference frequency will be amplified, and the random noise components will be smoothed by the RC network.

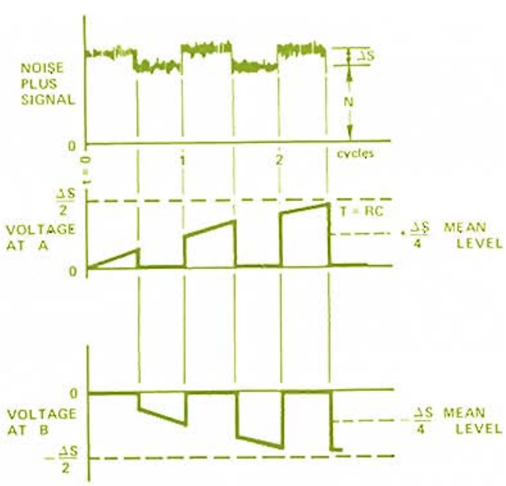


Figure 2. Waveforms at the input

In operation, the circuit is found to have excellent zero level stability. When operating with T = 1s and $G_o = 100$, the long-term instability, noise plus drift at the output, is ≅ 1mV peak-to-peak.

The effective noise at the output can be calculated from the usual radiometer equation. For a modulated signal ΔS, masked in underlying noise $N_{rms}$, the signal/noise ratio at the output is given by

$$\left(\frac{S}{N}\right)_{out} = \frac{\Delta S}{N_{rms}}(\beta T)^{1/2} \qquad (1)$$

where β is the bandwidth of the band-limited noise at the input and T = RC. For example, if ΔS = 10mV, $N_{rms}$ = 1V, β = 10kHz, T = 1s, and $G_o$ = 100,

$$\left(\frac{S}{N}\right)_{out} = \frac{10^{-2}}{1}(10^4)^{1/2} = 1 \qquad (2)$$

and $S_{out} = G_o\Delta V_s = 1V$. Thus, a 10mV signal masked by $1V_{rms}$ noise would just be detectable as a 1V signal at the output.

Besides its economy, there are a number of other advantages of the circuit. For example,

- The dc component of the signal-plus-noise is rejected by the amplifier's common-mode rejection (up to 120dB here).
- The use of a single capacitor across the high-impedance input of the amplifier (instead of two capacitors to common) provides improved common-mode rejection for the unwanted noise components.
- The use of a classic instrumentation amplifier provides all of its expected benefits, including symmetrical (and high) input impedance, and stable gain, determined by a single gain resistor (once the scale resistor has been selected).
- The smoothing time constant, T = RC, is determined by a single high-quality (polystyrene or polycarbonate) capacitor, given $R_1$, $R_2$. The circuit performs with reference frequencies beyond 10kHz.

In practice, in order to balance the system, a large dc signal is applied at the input, and $R_{adj}$ is adjusted for zero dc output. This, at the same time, balances the circuit for ac symmetry $(R_1 = R_2)$. ▶▶▶



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†For information on the AD520, request **L17**.