HIGH SPEED OP AMPS REVISITED – 1

WHAT DOES "HIGH SPEED" MEAN TO THE USER?

by Jerry Fishman

Because of the demand for increased speed in computers and data-acquisition systems, the circuit engineer is designing with higher-speed analog components than he may have used in the past. And nowadays, there is a much wider choice available to him, in the form of both IC's and discrete modules, each specified in terms of whatever its strong points happen to be, i.e., slewing rate, settling time, bandwidth, output current, stability, low noise.

Often the designer finds it difficult to interpret the manufacturers' specs in terms of his own application to make an informed choice. And when he uses the device he has chosen in his circuit, he may find that its performance is quite different from what he expected (or was led to believe he could obtain). There is often a world of difference between manufacturers' test circuits and the hurly-burly world of real applications.

There is no doubt that high-speed amplifier terminology can be confusing. What is a high-speed amplifier to one designer might be a medium-speed amplifier to another. A high slewing-rate amplifier, a fast-settling amplifier, and a wide-bandwidth amplifier - all are fast, but in quite different ways. In these pages, we shall seek to dispel some of the confusion by providing practical definitions of the specifications, relating them to applications, and discussing some of the factors that affect the design of practical high-speed circuits.

Since the great majority of high-speed amplifiers considered for use now (and increasingly in the future) are integrated-circuit, this discussion will lay heavy emphasis on integrated circuits. As the table on page 11 shows,* "high-speed" op amps are characterized by small-signal unity-gain bandwidths of the order of 10MHz or more, slewing rates in excess of about 20V/μs, submicrosecond settling times to within 0.1%, and settling times of the order of 1 μs to within 0.01%.

SLEWING RATE

Slewing rate is the maximum available rate-of-change of output voltage. If an ideal step could be applied to the input of an op amp circuit, the output rate of change would be limited, principally by the speed with which capacitance can be charged by current ($dV/dt_{max} = I_{max}/C$), either at the output (maximum output current into the load capacitance) or at some point inside the amplifier.

Slewing rate is affected by the external "gain" connection of the feedback elements; it is affected by the value of external compensating capacitance; it is affected by whether the configuration is inverting or non-inverting; and it very likely differs between the leading edge and trailing edge of the waveform. It is also affected by the portion of the response over which the measurement is performed (typically from 10% to 90% of the difference between the initial and final values).

*Ed. note: The table on page 11 provides a comparison of the specifications of typical members of various high-speed op amp families, both I.C. and discrete-module.

There is little uniformity among manufacturers on how to measure slewing rate. The spec usually quoted is the one that makes the amplifier look best. However, it should be measured for both leading and trailing edge and specified for the worst case, usually unity-gain, non-inverting. However, while there is no one correct method or configuration, it is important that the manufacturer and the user agree on the same criteria.

Figure 1 is a simplified representation of an operational amplifier that shows how the slewing rate is internally affected by the current in the input stage and the compensation capacitor. In Figure 1, the current through each collector circuit is I, and both are furnished by a current source, 2I. In the linear (small input-difference) mode, the currents are I + ΔI and I – ΔI, where the ΔI's tend to be small. However, if the input signal becomes large enough to shut one of the input transistors off (which happens when the amplifier is desperately trying to follow a fast input, and can't make it, creating a large difference signal), the current through Q2 can range from 0 to 2I. Since the active load usually seeks to maintain its current at the static value I, the difference current, I or –I, flows through the input of the next stage.

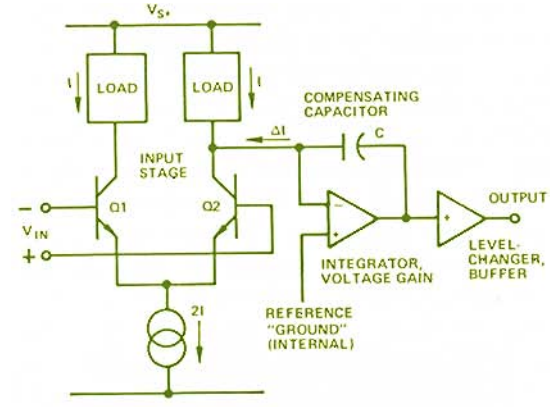

Figure 1. Simplified typical op amp configuration

The next stage is usually an integrator; that is, it has a constant 90° phase shift and an amplitude response that is inversely proportional to frequency (-6dB per octave). It controls the amplifier's overall frequency response; with the right value of capacitance, it will ensure stability over the whole range of resistive feedback ratios. (That is, a feedback amplifier must have a tailored response, rather than a "flat-out" wideband response, in order to be universally stable. More on this later.) With a constant current (I or –I) flowing through the capacitor, the output of the amplifier changes at the rate I/C; it cannot change at a faster rate. This is the internally-determined slewing rate. In the AD518, for example, the value of I

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is 400μA, and C = 5pF, which gives a nominal slewing rate of 80V/μs.

All operational amplifiers use compensation of this sort, but the actual circuitry can differ considerably. In some, the integrating capacitor is connected between the collectors; in others, it is "grounded," either to common, or to one side of the supply.* In many integrated-circuit op amps, it is connected externally, and chosen by the user for the best compromise between stability and bandwidth.

For a given value of signal gain, a non-inverting configuration may require more compensation than its inverting counterpart. Figure 2 shows two circuits that have gains of 1. But the non-inverting amplifier has a loop gain of A, while the inverting amplifier has a loop gain of A/2, which would lead one to expect that the non-inverting amplifier will require more compensating capacitance. Consequently, the inverting configuration will slew at a faster rate, if the user has connected a smaller value of compensating capacitance.

The relationship usually employed to relate slewing rate to full-power sinusoidal output is

$$dE_o/dt\big|_{max} = d(E_{oFS} \sin \omega t) / dt = E_{oFS}\,\omega$$

Since $\omega = 2\pi f$, the frequency for full-power output is

$$\frac{dE_o/dt\ _{max}}{2\pi E_{oFS}}$$

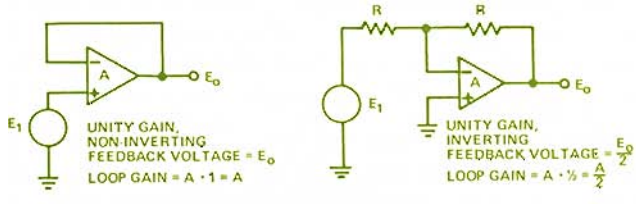

Figure 2. Inverting circuit has less loop gain

Thus, for a 10-volt amplifier, 6V/μs of slewing rate corresponds to a full-power frequency of 100kHz.

The usefulness of slewing rate as a measure of performance is rather restricted: It provides an approximation of the frequency range at which distortion becomes excessive, it suggests the narrowest pulse-width that may be gotten through an amplifier with reasonable fidelity, and it provides a measure of the sharpness of signals that may be applied with response predicted by the small-signal response. However, to predict the rate at which high accuracy can be maintained, one must know the *settling time.*

SETTLING TIME

Settling time† is the time elapsed from the application of an ideal step-input to the time the closed-loop amplifier output enters and remains within a specified error band, usually symmetrical about the final value (Figure 3). Settling time includes a brief propagation delay, the time required for the output to slew to the vicinity of the final value, the recovery from the overload condition associated with slewing (that capacitors must be discharged, and any thermal unbalances must be resolved), and the final time to settle to within the specified range.

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*741-type amplifiers are an example of this connection. For such amplifiers, the negative supply must be extremely well-regulated, since high-frequency noise and ripple are transmitted directly to the amplifier output.

†A comprehensive and useful discussion of settling time may be found in *Analog Dialogue*, Volume 4, No. 1

CHOOSING A HIGH-SPEED OP AMP

The general rule for packaged circuits applies: Pick the lowest-cost I.C. that you are sure will do the job; if you can't find (or adapt) one that will, it will become necessary to pick the most suitable discrete design.

It is usually the case that I.C.'s have considerable advantages in cost and size. However, to meet the needs of extreme performance requirements, modules may still be necessary. Examples of situations that require modules are:

- **Large amounts of power are involved — 20 to 100mA of output current at ±10V (the faster the circuit, the lower the impedances, hence the greater the power and dissipation requirements).**
- **Noise must be extremely low: less than 10μV rms (in a 5MHz bandwidth).**
- **Settling times must be less than 500ns to within 0.01% or 100ns to within 0.1%; slewing rates must be in excess of 120V/μs; and/or unity gain bandwidths must be greater than 35MHz; any or all of these on a min-max basis.**
- **Any or all of the above with internal compensation.**

Generally, a manufacturer's sales and applications engineers can be of assistance in making a good choice; the broader the product line available, the more reliable and dispassionate the advice that will be obtained, especially if the manufacturer, like Analog Devices, offers a wide variety of both IC and discrete high-speed amplifiers. The table below lists a number of the types available from ADI, both IC and modular, as examples of the available specification mix.*

RELEVANT CHARACTERISTICS OF
TYPICAL HIGH-SPEED OPERATIONAL AMPLIFIERS

at 25°C and V_s = ±15V, unless noted otherwise

Type Designation	Unity-gain BW (MHz) Typical	Slewing Rate (V/μs) Minimum	Settling Time (0.1%) Maximum	Settling Time (0.01%) Maximum	Price 1+ $U.S.
INTEGRATED CIRCUITS					
AD509S, differential	20	100	0.5	2.5	26.00
AD509K, differential	20	80	0.5	2.5	18.75
AD508J, differential	20	80	0.2(T)	1.0(T)	11.50
AD506J, inverting	4 to 10§	120	0.8(T)	2.0(T)	15.00
AD518J, differential	12	50	0.8(T)	2.0(T)	3.00
AD528J, differential FET	10	50	0.8(T)	—	18.00
AD507J, differential	35	20	0.9(T)	—	9.50
DISCRETE MODULES					
50J, differential FET	80	500	0.1	0.2(0.05%)	75.00
51A, differential FET	80	400(T)	0.14	0.35	99.00
48J, differential FET	15	125/90†	0.25(T)	0.3(T)	49.00
45J, differential FET	10	75	0.5(T)	1.0	37.00
44J, differential FET	10	75/50†	0.5(T)	1.0	42.00
120A, inverting	10 to 100§	250	—	1.0(T)	78.00
47A, differential FET	10	50	0.5(T)	1.0	77.00

§Bandwidth adjustable
(T) Typical value
† Inverting/non-inverting

*To request information on a specific type, use the blank spaces at the head of the reply card. For catalog information on the whole product line, request L7.

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This definition is now widely accepted. At one time, though, some manufacturers defined settling time in terms of the final "tail" only. When short settling times are quoted, the reader should make sure that the above "long-form" definition is the one used.

Settling time is a closed-loop parameter determined by a combination of amplifier characteristics, nonlinear as well as linear. Thus, it cannot be predicted readily from such open-loop specs as slewing rate and small-signal bandwidth. An extremely-high slewing rate does not insure a rapid settling time, because slewing rate is only one of the factors affecting it. An amplifier with an extremely-high slewing rate can often have a long settling time.

Normally, the final value achieved in the definition is not necessarily the exactly correct value of amplifier output, since that value is affected by amplifier open-loop gain, offset voltage and drift, and common-mode error. Settling time to within a given band cannot be defined at all if noise is excessive. However, a desire for a given level of settling-time performance usually implies that the amplifier must also have satisfactorily-small levels of error due to such causes.

For example, fast-settling amplifiers are used in many applications for high-accuracy conversion systems requiring fast settling to either 10- or 12-bit accuracy, within ±½ least-significant bit (0.05% or 0.0125%). If an amplifier has a rated output voltage of 10V, 0.0125% represents 1.25mV of error. For such high degrees of resolution, other errors, as well as settling time, must be minimized.

Op amps designed for optimum response at high closed-loop gains at moderate frequencies often have transfer functions that provide only marginal stability when the closed-loop gain is reduced to values near unity. The amplifier used for fast settling to high accuracy should have a closed-loop response that is (at least theoretically) only slightly less than critically damped, since any oscillation or ringing may prolong settling time.

And, in practical circuits that have stray capacitance, the added lags caused by the external loop elements will cause a system to ring, even if it has an amplifier with sufficient phase margin. For this reason, designers of fast-settling op amps try to have the open-loop frequency characteristics strongly dominated by a single time constant. This is stated in many ways, all with the same meaning: constant 90° phase shift, −6dB/octave (or −20dB/decade) rolloff, unit lag, exponential time response.

The term "settling time" is also used to indicate the time required to restore the output to its original level after it has been disturbed by a transient associated with a step change of load. In conversion circuits, the settling time is the time required to achieve and remain within ±½ least-significant bit of final value.

Because of the low final-value errors and wide-ranging slewing transients, settling time is quite difficult to measure. Measurement circuits for settling-time in analog circuits are described in Volume 4, No. 1 of *Analog Dialogue*; settling-time measurements for conversion circuits are shown in the *Analog-Digital Conversion Handbook*, starting on page II-116.

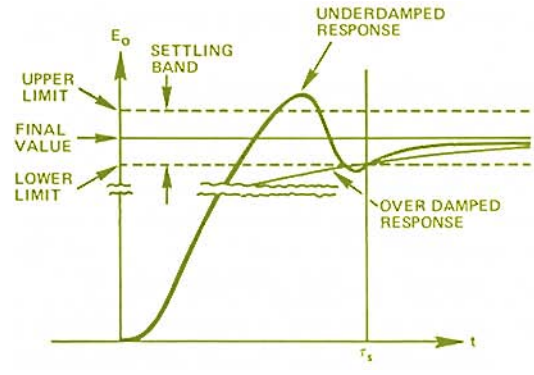

Figure 3. Examples of settling time. Voltage scale greatly magnified in vicinity of final value.

MINIMIZING SETTLING TIME

The settling time of a practical op amp circuit is determined by the input source, the operational amplifier, and the associated circuitry (including stray capacitances and the non-ideal nature of circuit components, such as resistors and diodes). While the amplifier alone is predictable, as specified in a certain configuration, what is painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of good high-speed design are:

Power supplies and grounds should be properly connected and bypassed (typically, with 0.1μF ceramic capacitors, connected at the op amp socket) to avoid introduction of noise, stray feedback paths, or ground loops. Load- and summing-point-capacitances should be minimized or compensated for. All connections should be short and direct, to minimize lead inductance and capacitive coupling.

Resistors should be metal-film types; they have less capacitance and stray inductance than wirewound types, yet have excellent accuracies, temperature coefficients, and tracking.

Capacitors in critical locations should use extended-foil construction, with dielectrics of polystyrene, Teflon, or polycarbonate, to minimize dielectric absorption.

Circuit impedance levels should be as low as is consistent with the output capabilities of the amplifier and the signal source. Don't overlook sockets or the p.c. board itself as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier.

SLOW BUT ACCURATE

As noted, fast settling to an uncertain final value is useless. On the other hand, not-too-slow settling to an accurately determined final value can be quite useful. For example, the low-drift, high-gain, high CMR, low-noise (0.5μV/°C max, 106 & 110dB min, 0.6μVp-p max – 0.1 to 10Hz) AD504M* integrated-circuit op amp, connected for gain-of-100, settles to within 0.01% in about 1ms, quite adequate for chart recorders, panel meters, and many measurement circuits. ▶▶▶

To be continued. The next installment will discuss stability and phase margin, and the use of Bodé plots as an indispensible tool for predicting small-signal instabilities.

*For information on the AD504 family, request L2.