Applications for a High Speed FET Input Op Amp

National Semiconductor
Application Note 75

INTRODUCTION

The principal limitations in speed and bandwidth in IC FET input op amps have been reduced by over an order of magnitude with the introduction of the LH0062/LH0062C. Internal compensation assures unity gain stability with bandwidths in excess of 15 MHz. Voltage follower slew rate is typically 75 V/μs and is guaranteed in excess of 50 V/μs. Furthermore, external components may be used to extend the slew rate to 120 V/μs and settling times under 1 μs. The LH0062H (TO-5) is pin compatible with LM101, LM741 and LH0022. A summary of the LH0062's performance characteristics is given in Table I.

CIRCUIT DESCRIPTION

The LH0062 is basically a two stage amplifier (*Figure 1*) consisting of a N channel junction FET input stage (Q_1 and Q_2) and a PNP output stage (Q_4 and Q_5). Q_1 and Q_2 are a well matched interdigitated monolithic pair that provide high common mode rejection and input offset voltage tracking usually associated only with bipolar designs. The current mirror (Q_6 and Q_7) converts to single ended operation in addition to providing active high impedance load for Q_4 and Q_5 thus providing high gain. Q_3 and D_1 provide a temperature compensated current source for the input stage and Q_8, Q_9, D_2 and D_3 form a class AB output buffer. Detailed schematic is illustrated in *Figure 2*. Note that the FET inputs are protected by 5V zener diodes and input current under transient conditions should be limited by inserting a 1 kΩ or larger resistor in series with one of the inputs.

TABLE I. Summary of LH0062 Characteristics

Parameter (T_A = 25°C)	Min	Typ	Max	Units
Input Offset Voltage		2.0	5.0	mV
Input Bias Current			20	pA
Voltage Gain	50	100		V/mV
Slew Rate	50	75		V/μs
Bandwidth		15		MHz

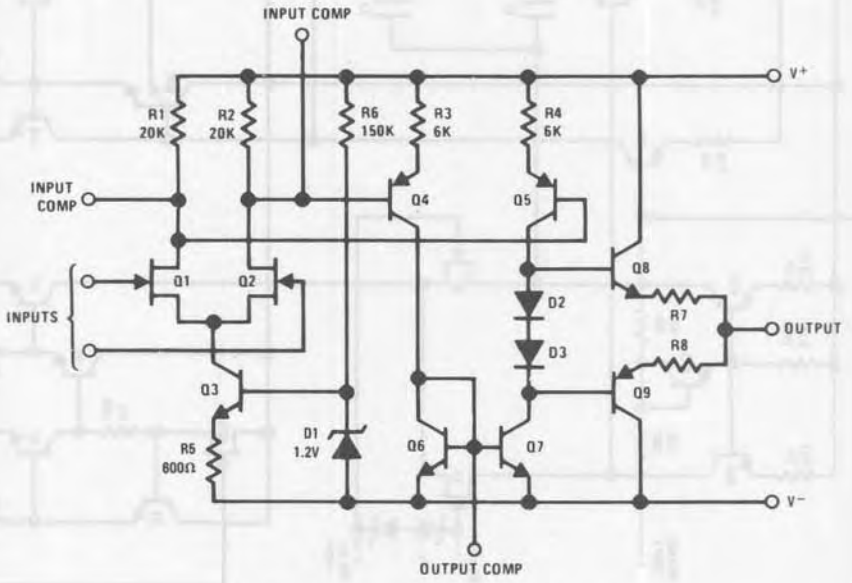

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FIGURE 1. Simplified LH0062 Circuit Schematic

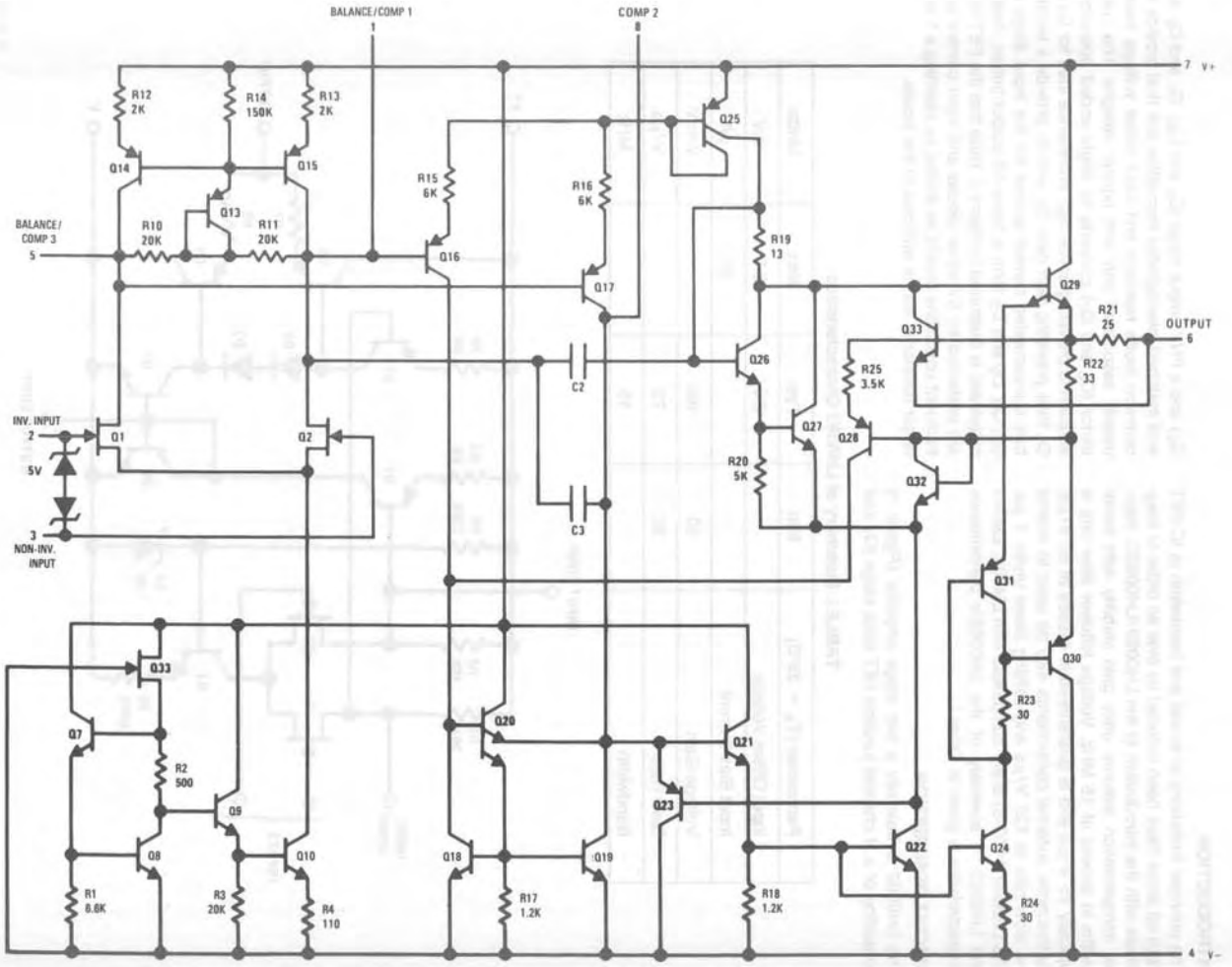

FIGURE 2. Complete LH0062 Schematic

COMPENSATION CONSIDERATIONS

As noted earlier, the LH0062 is internally compensated for unity gain stability. However, a few precautions are advised. Like most wide band amplifiers, the LH0062 is sensitive to power supply inductance, and decoupling the supplies with 0.1 μF ceramic disc capacitors within an inch or two of the device will prevent spurious oscillations and save a fair amount of grief. The device is capable of driving 50 pF to 100 pF loads; for larger loads, an isolation resistor, R_3 as shown in *Figure 3* is recommended. Alternatively, a current buffer such as the LH0002 or LH0033 may be used for loads in excess of 500 pF with no degradation in slew rate as shown in *Figure 4*.

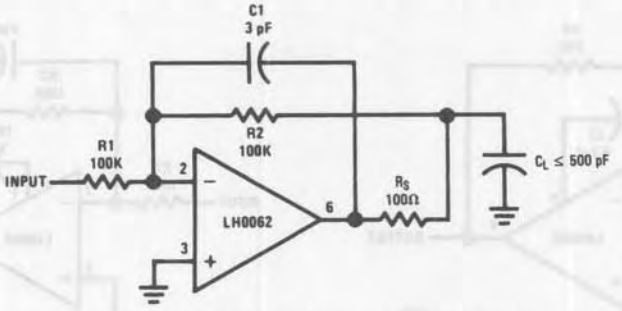

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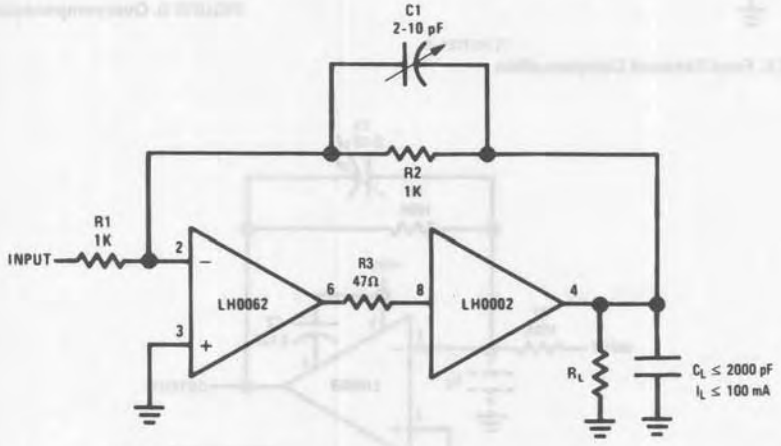
FIGURE 3. Isolating a Capacitive Load up to 500 pF



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Note: In the examples above, at a small capacitor, C1, is used to cancel the effects of stray capacitance at the input.

FIGURE 4. Driving Capacitances in Excess of 500 pF and Loads

The LH0062 may be feed-forward compensated in inverting mode applications as shown in *Figure 5*. This boosts slew rate to over 120 V/μs and bandwidth to over 30 MHz. When full bandwidth is not required, the device may be over-compensated as shown in *Figure 6* to reduce bandwidth to 5 MHz. This technique improves phase margin and reduces susceptibility to spurious oscillations in applications where speed is less critical.

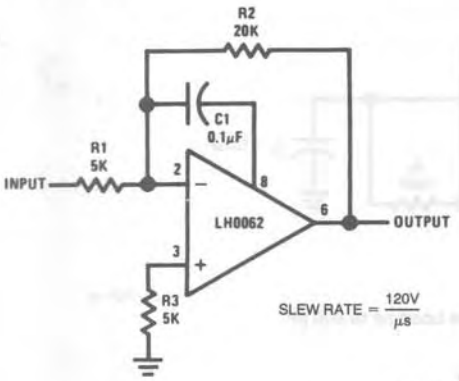

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FIGURE 5. Feed Forward Compensation

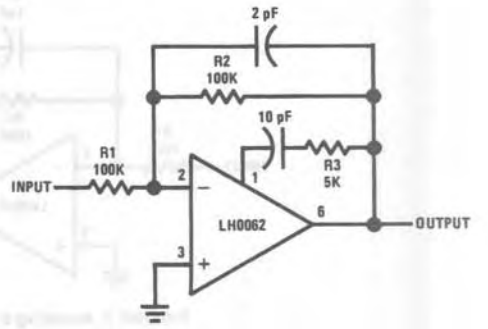

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FIGURE 6. Overcompensation

Minimum settling time of less than 1 μs to 0.1% for a 20V input step is obtained as illustrated in *Figure 7*. A small tweak capacitor, C_1 is recommended to cancel stray board layout capacitance, C_S. Once best value of trimmer capacitor C_1 is determined for a particular layout, it may be replaced with a fixed value.

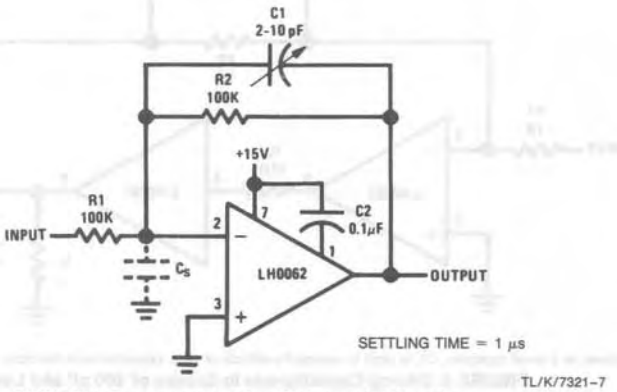

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FIGURE 7. Compensation for Minimum Settling Time

APPLICATIONS

The circuit of *Figure 8* is a high speed sample and hold with sample acquisition time of 10 μs for 0.1% accuracy and aperture time of approximately 25 ns. Resistor, R_6, is used to limit input current during power on and off transients. Although the inputs of the LH0062 are protected by back-to-back diodes excessive input current could damage the device. Resistor R_9 and the pot, R_8, allow null of the output offset with negligible effect on offset drift.

The peak detector of *Figure 9* will acquire a +10V peak signal in under 4 μs with droop rates under 20 mV/sec. Reversing the polarity of diodes D_1 and D_2 will allow peak detecting negative signals. Any ultra-low leakage diode may be substituted for the 2N930 collector-base junction.

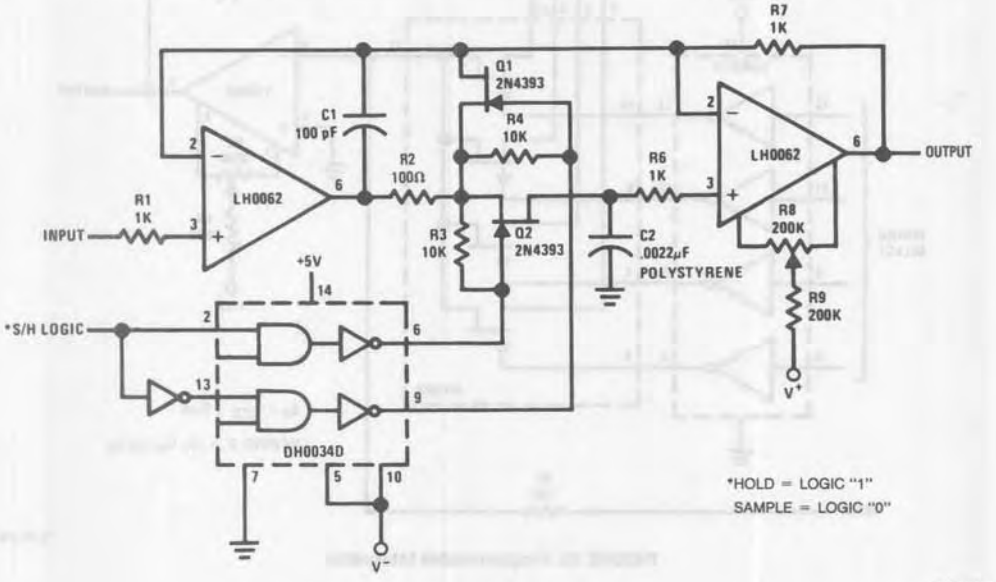

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FIGURE 8. High Speed Sample and Hold

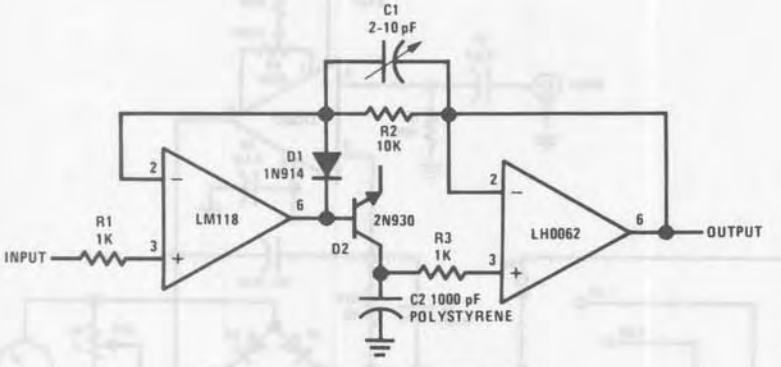

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FIGURE 9. High Speed Peak Detector

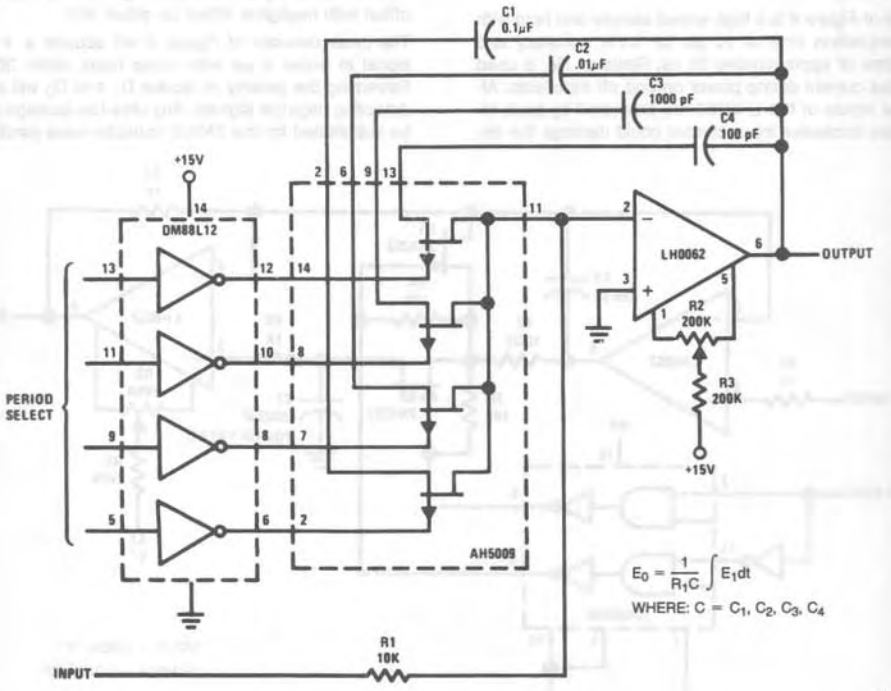

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FIGURE 10. Programmable Integrator

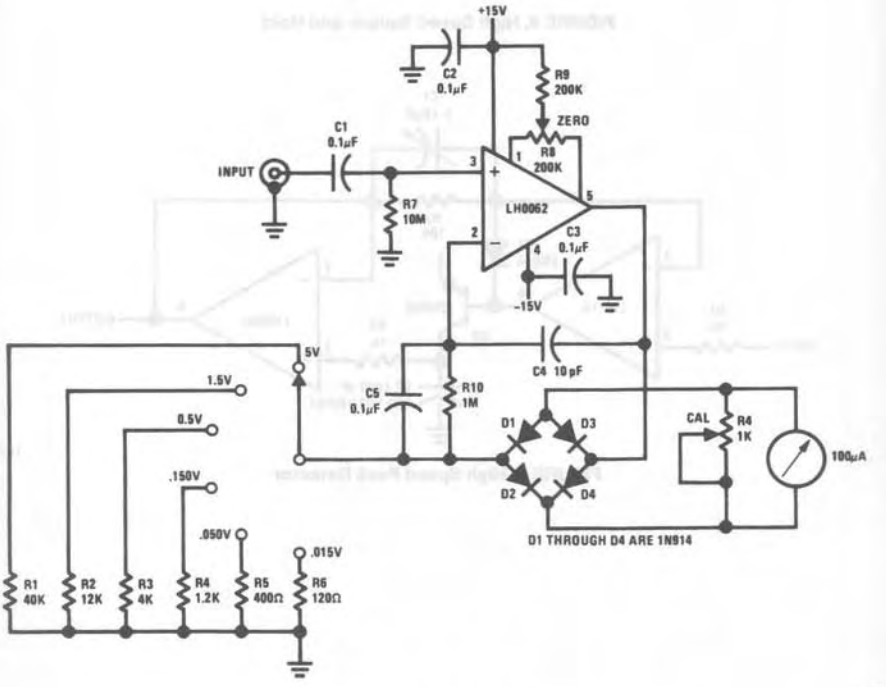

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FIGURE 11. Wide Band AC Voltmeter

The circuit of *Figure 10* is a programmable integrator with a range in period from 1 μs to 1 ms. For best results C_1 through C_4 should be low leakage construction such as polycarbonate or polystyrene. A simple method of implementing the offset adjustment is to momentarily insert a 100 kΩ resistor between pins 2 and 6 of the LH0062. With the switches of the AH5009 off, the output may be set to zero with R_2.

The circuit of *Figure 11* is a wide band AC voltmeter capable of measuring AC signals as low as 15 mV at frequencies from 100 Hz to 500 kHz. Full scale sensitivity may be changed by altering the values R_1 through R_6 ($R \cong V_{IN}/100\ \mu A$).

HEAT SINKING, GUARDING, AND BOOTSTRAPPING

The LH0062 is specified for operation without an external heat sink. However, standby power is typically 240 mW causing a junction rise of approximately 60°C. A clip-on heat sink can reduce internal heating hence reduce input bias current from 20 pA at 25°C ambient to 2 or 3 pA.

Guarding input leads is recommended in stringent applications. An excellent discussion on guarding is given in AN-63 and the techniques discussed are directly applicable to the LH0062. Another benefit of guarding is reduced input capacitance. By bootstrapping the inputs, as shown in *Figure 12*, the apparent input capacitance is reduced to fractions of a pico-farad.

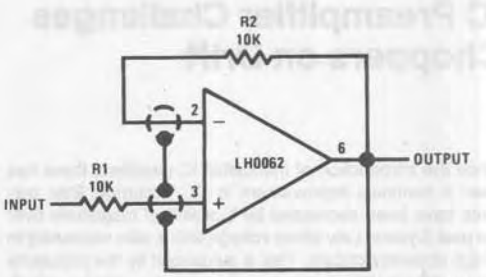

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FIGURE 12. Guard/Bootstrap for Unity Gain

Furthermore, the case of the LH0062 is electrically isolated, and the output may be tied to case in order to eliminate stray capacitance introduced by the header.

REFERENCES

1. R. K. Underwood, *"New Design Techniques for FET Op Amps,"* National Semiconductor AN-63, March 1972.
2. R. C. Dobkin, *"LM118 Op Amp Slews 70 V/μs,"* National Semiconductor LB-17, September 1971.