SECTION 7-6

EMI/RFI Considerations

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Analog circuit performance is often adversely affected by high frequency signals from nearby electrical activity. And, equipment containing analog circuitry may also adversely affect systems external to it. Reference 1 (page 4) describes this complementary transmission of undesirable high frequency signals from or into local equipment as per an IEC50 definition. These corresponding aspects of broad arena of *electromagnetic compatibility*, better known as EMC, are:

- *It describes the ability of electrical and electronic systems to operate without interfering with other systems . . .*
- *It also describes the ability of such systems to operate as intended within a specified electromagnetic environment.*

Complete EMC assurance would indicate that the equipment under design should neither produce spurious signals, nor be vulnerable to out-of-band external signals (i.e., those outside its intended frequency range). It is the latter class of EMC problem to which analog equipment most often falls prey. It is the graceful handling of these spurious signals that are emphasized within this section.

The externally produced electrical activity may generate noise, and is referred to either as electromagnetic interference (EMI), or radio frequency interference (RFI). In this section, we will refer to EMI in terms of both electromagnetic and radio frequency interference. One of the more challenging tasks of the analog designer is the control of equipment against undesired operation due to EMI. It is important to note that in this context, *EMI and or RFI is almost always detrimental*. Once given entrance into the equipment, it can and will degrade its operation, quite often considerably.

This section is heavily oriented towards minimizing undesirable analog circuit operation due to the *receipt* of EMI/RFI. Misbehavior of this sort is also known as EMI or RFI *susceptibility*, indicating a tendency towards anomalous equipment behavior when exposed to EMI/RFI. There is, of course, a complementary EMC issue, namely with regard to spurious *emissions.* However, since analog circuits typically involve fewer of pulsed, high speed, high current signal edges that give rise to such spurious signals (compared to high speed logic, for example), this aspect of EMC isn't as heavily treated here. Nevertheless, the reader should bear in mind that it can be important, particularly if the analog circuitry is part of a mixed-signal environment along with high speed logic.

Since all of these various EMC design points can be critical, *the end-of-chapter references are strongly recommended for supplementary study*. Indeed, for a thorough, fully competent design with respect to EMI, RFI, and EMC, the designer will need to become intimately acquainted with one or more of these references (see References 1–6). As for the material following, it is best viewed as an introduction to this extremely broad but increasingly important topic.

EMI/RFI Mechanisms

To understand and properly control EMI and RFI, it is helpful to first segregate it into manageable portions. Thus it is useful to remember that when EMI/RFI problems do occur, they can be fundamentally broken down into a *Source*, a *Path*, and a *Receiver*. As a systems designer, you have under your direct control the receiver part of this landscape, and perhaps some portion of the path. But seldom will the designer have control over the actual source.

EMI Noise Sources

There are countless ways in which undesired noise can couple into an analog circuit to ruin its accuracy. Some of the many examples of these noise sources are listed in Figure 7-97.

- EMI/RFI noise sources can couple from anywhere
- Some common sources of externally generated noise:
  - Radio and TV Broadcasts
  - Mobile Radio Communications
  - Cellular Telephones
  - Vehicular Ignition
  - Lightning
  - Utility Power Lines
  - Electric Motors
  - Computers
  - Garage Door Openers
  - Telemetry Equipment

Figure 7-97: Some common EMI noise sources

Since little control is possible over these sources of EMI, the next best management tool to exercise over them is to recognize and understand the possible paths by which they couple into the equipment under design.

EMI Coupling Paths

The EMI coupling paths are actually very few in terms of basic number. Three very general paths are by:

1. *Interference due to conduction (common-impedance)*
2. *Interference due to capacitive or inductive coupling (near-field interference)*
3. *Electromagnetic radiation (far-field interference)*

Noise Coupling Mechanisms

EMI energy may enter wherever there is an impedance mismatch or discontinuity in a system. In general this occurs at the interface where cables carrying sensitive analog signals are connected to PC boards, and through power supply leads. Improperly connected cables or poor supply filtering schemes are often perfect conduits for interference.

Conducted noise may also be encountered when two or more currents share a common path (impedance). This common path is often a high impedance “ground” connection. If two circuits share this path, noise currents from one will produce noise voltages in the other. Steps may be taken to identify potential sources of this interference (see References 1 and 2, plus Section 2 of this chapter).

Figure 7-98 shows some of the general ways noise can enter a circuit from external sources.

- Impedance mismatches and discontinuities
- Common-mode impedance mismatches → Differential Signals
- Capacitively Coupled (Electric Field Interference)
  - dV/dt → Mutual Capacitance → Noise Current
    (Example: 1V/ns produces 1mA/pF)
- Inductively Coupled (Magnetic Field)
  - di/dt → Mutual Inductance → Noise Voltage
    (Example: 1mA/ns produces 1mV/nH)

Figure 7-98: How EMI finds paths into equipment

There is a capacitance between any two conductors separated by a dielectric (air and vacuum are dielectrics, as well as all solid or liquid insulators). If there is a change of voltage on one conductor there will be change of charge on the other, and a *displacement current* will flow in the dielectric. Where either the capacitance or the dV/dT is high, noise is easily coupled. For example, a 1 V/ns rate-of-change gives rise to displacement currents of 1 mA/pF.

If changing magnetic flux from current flowing in one circuit threads another circuit, it will induce an emf in the second circuit. Such *mutual inductance* can be a troublesome source of noise coupling from circuits with high values of dI/dT. As an example, a mutual inductance of 1 nH and a changing current of 1 A/ns will induce an emf of 1 V.

Reducing Common-Impedance Noise

Steps to be taken to eliminate or reduce noise due to the conduction path sharing of impedances, or *common-impedance noise* are outlined in Figure 7-99.

- Common-impedance noise
  - Decouple op amp power leads at LF and HF
  - Reduce common-impedance
  - Eliminate shared paths
- Techniques
  - Low impedance electrolytic (LF) and local low inductance (HF) bypasses
  - Use ground and power planes
  - Optimize system design

Figure 7-99: Some solutions to common-impedance noise

These methods should be applied in conjunction with all of the related techniques discussed earlier within Section 2 of this chapter.

Power supply rails feeding several circuits are good common-impedance examples. Real-world power sources may exhibit low output impedance, or may they not—especially over frequency. Furthermore, PCB traces used to distribute power are both inductive and resistive, and may also form a ground loop. The use of power and ground planes also reduces the power distribution impedance. These dedicated conductor layers in a PCB are continuous (ideally, that is) and, as such, offer the lowest practical resistance and inductance.

In some applications where low level signals encounter high levels of common-impedance noise it will not be possible to prevent interference and the system architecture may need to be changed. Possible changes include:

1. *Transmitting signals in differential form*
2. *Amplifying signals to higher levels for improved S/N*
3. *Converting signals into currents for transmission*
4. *Converting signals directly into digital form*

Noise Induced by Near-Field Interference

Crosstalk is the second most common form of interference. In the vicinity of the noise source, i.e., near-field, interference is not transmitted as an electromagnetic wave, and the term crosstalk may apply to either inductively or capacitively coupled signals.

Reducing Capacitance-Coupled Noise

Capacitively-coupled noise may be reduced by reducing the coupling capacity (by increasing conductor separation), but is most easily cured by shielding. A conductive and grounded shield (known as a *Faraday shield*) between the signal source and the affected node will eliminate this noise, by routing the displacement current directly to ground.

With the use of such shields, it is important to note that it is always *essential* that a Faraday shield be grounded. A floating or open-circuit shield almost invariably increases capacitively-coupled noise. For a brief review of this shielding, consult Section 2 of this chapter, and see References 2 and 3 at the end of this section.

Methods to eliminate capacitance-coupled interference are summarized in Figure 7-100.

- Reduce Level of High dV/dt Noise Sources
- Use Proper Grounding Schemes for Cable Shields
- Reduce Stray Capacitance
  - Equalize Input Lead Lengths
  - Keep Traces Short
  - Use Signal-Ground Signal-Routing Schemes
- Use Grounded Conductive Faraday Shields to Protect
- Against Electric Fields

Figure 7-100: Methods to reduce capacitance-coupled noise

Reducing Magnetically-Coupled Noise

Methods to eliminate interference caused by magnetic fields are summarized in Figure 7-101.

To illustrate the effect of magnetically-coupled noise, consider a circuit with a closed-loop area of A cm^2 operating in a magnetic field with an rms flux density value of B gauss. The noise voltage V_n induced in this circuit can be expressed by the following equation:

$$V_n = 2\pi f B A \cos\theta \times 10^{-8} V \qquad \text{Eq. 7-8}$$

In this equation, *f* represents the frequency of the magnetic field, and θ represents the angle of the magnetic field B to the circuit with loop area A. Magnetic field coupling can be reduced by reducing the circuit loop

- Careful Routing of Wiring
- Use Conductive Screens for HF Magnetic Shields
- Use High Permeability Shields for LF Magnetic Fields (Mu-Metal)
- Reduce Loop Area of Receiver
  - Twisted Pair Wiring
  - Physical Wire Placement
  - Orientation of Circuit to Interference
- Reduce Noise Sources
  - Twisted Pair Wiring
  - Driven Shields

Figure 7-101: Methods to reduce magnetically-coupled noise

area, the magnetic field intensity, or the angle of incidence. Reducing circuit loop area requires arranging the circuit conductors closer together. Twisting the conductors together reduces the loop net area. This has the effect of canceling magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero. Reducing the magnetic field directly may be difficult. However, since magnetic field intensity is inversely proportional to the cube of the distance from the source, physically moving the affected circuit away from the magnetic field has a very great effect in reducing the induced noise voltage. Finally, if the circuit is placed perpendicular to the magnetic field, pickup is minimized. If the circuit's conductors are in parallel to the magnetic field the induced noise is maximized because the angle of incidence is zero.

There are also techniques that can be used to reduce the amount of magnetic-field interference, *at its source*. In the previous paragraph, the conductors of the receiver circuit were twisted together, to cancel the induced magnetic field along the wires. The same principle can be used on the source wiring. If the source of the magnetic field is large currents flowing through nearby conductors, these wires can be twisted together to reduce the net magnetic field.

Shields and cans are not nearly as effective against magnetic fields as against electric fields, but can be useful on occasion. At low frequencies magnetic shields using high permeability material such a Mu-metal can provide modest attenuation of magnetic fields. At high frequencies simple conductive shields are quite effective provided that the thickness of the shield is greater than the skin depth of the conductor used (at the frequency involved). Note—copper skin depth is $6.6/\sqrt{f}$ cm, with f in Hz.

Passive Components: Arsenal Against EMI

Passive components, such as resistors, capacitors, and inductors, are powerful tools for reducing externally induced interference when used properly.

Simple RC networks make efficient and inexpensive one-pole, low-pass filters. Incoming noise is converted to heat and dissipated in the resistor. But note that a fixed resistor does produce thermal noise of its own. Also, when used in the input circuit of an op amp or in amp, such resistor(s) can generate input-bias-current induced offset voltage. While matching the two resistors will minimize the dc offset, the noise will remain. Figure 7-102 summarizes some popular low-pass filters for minimizing EMI.

LP Filter Type	ADVANTAGE	DISADVANTAGE
RC Section	Simple Inexpensive	Resistor Thermal Noise $I_B \times$ R Drop $\rightarrow$ Offset Single-Pole Cutoff
LC Section (Bifilar)	Very Low Noise at LF Very Low IR Drop Inexpensive Two-Pole Cutoff	Medium Complexity Nonlinear Core Effects Possible
π Section (C-L-C)	Very Low Noise at LF Very Low IR Drop Pre-packaged Filters Multiple-Pole Cutoff	Most Complex Nonlinear Core Effects Possible Expensive

Figure 7-102: Using passive components within filters to combat EMI

In applications where signal and return conductors aren't well coupled magnetically, a common-mode (CM) choke can be used to increase their mutual inductance. Note that these comments apply mostly to in amps, which naturally receive a balanced input signal (whereas op amps are inherently unbalanced inputs—unless one constructs an in amp with them). A CM choke can be simply constructed by winding several turns of the differential signal conductors together through a high permeability (> 2000) ferrite bead. The magnetic properties of the ferrite allow differential-mode currents to pass unimpeded while suppressing CM currents.

Capacitors can also be used before and after the choke, to provide additional CM and differential-mode filtering, respectively. Such a CM choke is cheap and produces very low thermal noise and bias current-induced offsets, due to the wire's low DCR. However, there is a field around the core. A metallic shield surrounding the core may be necessary to prevent coupling with other circuits. Also, note that high current levels should be avoided in the core as they may saturate the ferrite.

The third method for passive filtering takes the form of packaged π-networks (C-L-C). These packaged filters are completely self-contained and include feedthrough capacitors at the input and the output as well as a shield to prevent the inductor's magnetic field from radiating noise. These more expensive networks offer high levels of attenuation and wide operating frequency ranges, but the filters must be selected so that for the operating current levels involved the ferrite doesn't saturate.

Reducing System Susceptibility to EMI

The general examples discussed above and the techniques illustrated earlier in this section outline the procedures that can be used to reduce or eliminate EMI/RFI. Considered on a *system* basis, a summary of possible measures is given in Figure 7-103.

- Always Assume that Interference Exists
- Use Conducting Enclosures Against Electric and HF
- Magnetic Fields
- Use Mu-Metal Enclosures against LF Magnetic Fields
- Implement Cable Shields Effectively
- Use Feedthrough Capacitors and Packaged PI Filters

Figure 7-103: Reducing system EMI/RFI susceptibility

Other examples of filtering techniques useful against EMI are illustrated later in this section, under "Reducing RFI rectification within op amp and in amp circuits."

The section immediately below further details shielding principles.

A Review of Shielding Concepts

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 4–9 cited at the end of the section for more detailed information.

Applying the concepts of shielding effectively requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receiver). If the circuit is operating close to the source (in the *near*, or induction-field), the field characteristics are determined by the source. If the circuit is remotely located (in the *far*, or radiation-field), the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2 π, or $\lambda/2\ \pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1 ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350 MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2 π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350 MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_o = 377\ \Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high current and low voltage (for example, a loop antenna or a power line transformer), the field is predominately magnetic and exhibits a wave impedance less than 377 Ω. If the source is low current and high voltage (for example, a rod antenna or a high speed digital switching circuit), the field is predominately electric and exhibits a wave impedance greater than 377 Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an *impedance mismatch* to the incident interference, because the impedance of the shield

is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e\,(\mathrm{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \qquad \text{Eq. 7-9}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;

μ_r = relative permeability of the shielding material, in Henries per meter;

f = frequency of the interference, and

r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m\,(\mathrm{dB}) = 14.6 + 10\log_{10}\left[\frac{fr^2\sigma_r}{\mu_r}\right] \qquad \text{Eq. 7-10}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}\,(\mathrm{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 7-11}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A\,(\mathrm{dB}) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 7-12}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9 dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss.

Thus for high frequency interference signals, lightweight, easily worked high conductivity materials such as copper or aluminum can provide adequate shielding. At low frequencies however, both reflection and absorption loss to magnetic fields is low. It is thus very difficult to shield circuits from low frequency magnetic fields. In these applications, high permeability materials that exhibit low reluctance provide the

best protection. These low reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.

To summarize the characteristics of metallic materials commonly used for shielded purposes: Use high conductivity metals for HF interference, and high permeability metals for LF interference.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Eq. 7-13 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\,(\text{dB}) = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 7-13}$$

where λ = wavelength of the interference and

L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0 dB shielding effectiveness). A rule of thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20 dB shielding effectiveness.

Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions and, as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, filters are recommended at the shield entry point.

General Points on Cables and Shields

Although covered in detail elsewhere, it is worth noting that the improper use of cables and their shields can be a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 2, 3, 5, and 6 for background.

As shown in Figure 7-104, proper cable/enclosure shielding confines sensitive circuitry and signals *entirely within the shield*, with no compromise to shielding effectiveness.

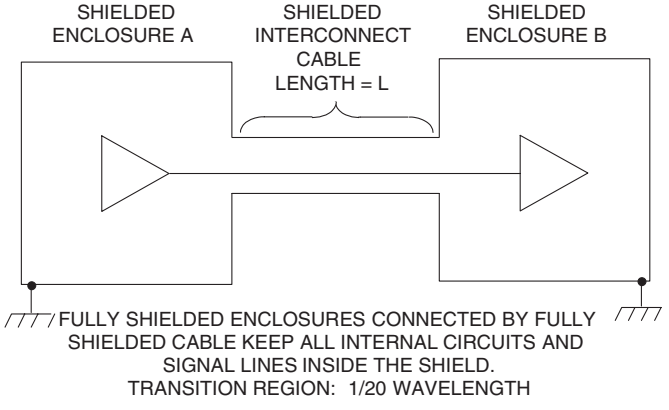


Figure 7-104: Shielded interconnect cables are either electrically long or short, depending upon the operating frequency

As can be noted by this diagram, the enclosures and the shield must be properly grounded, otherwise they can act as an antenna, thereby making the radiated and conducted interference problem worse (rather than better).

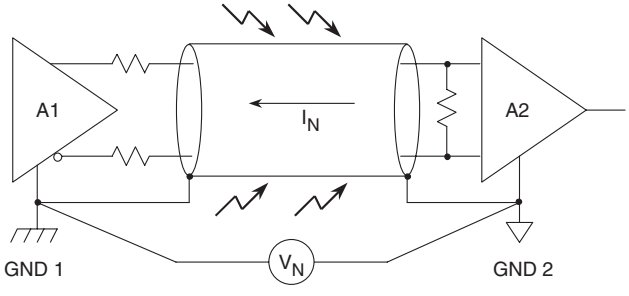
Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered electrically short if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference. Otherwise, it is considered to be electrically long.

For example, at 50 Hz/60 Hz, an electrically short cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In applications where the length of the cable is electrically long, or protection against high frequency interference is required, the preferred method is to connect the cable shield to low impedance points, *at both ends*. As will be seen shortly, this can be a direct connection at the driving end, and a capacitive connection at the receiver. If left ungrounded, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10 MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low impedance connections to ground.

In summary, for protection against low frequency (<1 MHz), electric-field interference, grounding the shield at one end is acceptable. For high frequency interference (>1 MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.

In practice, however, there is a caveat involved with directly grounding the shield at both ends. When this is done, it creates a low frequency ground loop, shown in Figure 7-105.



- V_N Causes Current in Shield (Usually 50Hz/60Hz)
- Differential Error Voltage is Produced at Input of A2 unless:
  - A1 Output is Perfectly Balanced and
  - A2 Input is Perfectly Balanced and
  - Cable is Perfectly Balanced

Figure 7-105: Ground loops in shielded twisted pair cable can cause errors

Whenever two systems A1 and A2 are remote from each other, there is usually a difference in the ground potentials at each system, i.e., V_N. The frequency of this potential difference is generally the line frequency (50 Hz or 60 Hz) and multiples thereof. But, if the shield is directly grounded at both ends as shown, noise current I_N flows in the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current flow produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver, so a certain portion of the shield current will appear as a differential noise signal, at the input of A2. The following illustrates correct shield grounding for various examples.

As noted above, cable shields are subject to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

Figure 7-106 shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end.

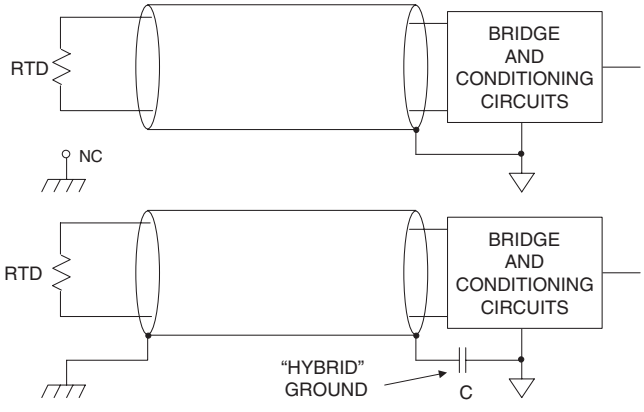


Figure 7-106: Hybrid grounding of shielded cable with passive sensor

Safety considerations may require that the remote end of the shield also be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor (0.01 μF to 0.1 μF), still providing high frequency grounding. The capacitor acts as a ground to RF signals on the shield but blocks low frequency line current to flow in the shield. This technique is often referred to as a *hybrid ground*.

A case of an active remote sensor and/or other electronics is shown Figure 7-107. In both situations, a hybrid ground is also appropriate, either for the balanced (upper) or the single-ended (lower) driver case. In both instances the capacitor "C" breaks the low frequency ground loop, providing effective RF grounding of the shielded cable at the A2 receiving end at the right side of the diagram.

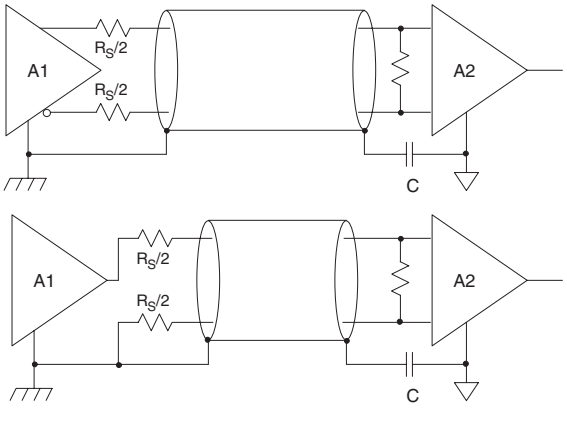


Figure 7-107: Impedance-balanced drive of balanced shielded cable aids noise-immunity with either balanced or single-ended source signals

There are also more subtle points that should be made with regard to the source termination resistances used, R_S. In both the balanced as well as the single-ended drive cases, the driving signal seen on the balanced line originates from a net impedance of R_S, which is split between the two twisted pair legs as twice $R_S/2$. In the upper case of a fully differential drive, this is straightforward, with an $R_S/2$ valued resistor connected in series with the complementary outputs from A1.

In the bottom case of the single-ended driver, note that there are still two $R_S/2$ resistors used, one in series with both legs. Here the grounded dummy return leg resistor provides an impedance-balanced ground connection drive to the differential line, aiding in overall system noise immunity. Note that this implementation is only useful for those applications with a balanced receiver at A2, as shown.

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in the upper portion of Figure 7-108. For this technique to work, however, the receiver must be a differential type with good high frequency CM rejection.

However, the receiver may be a single-ended type, such as typical of a standard single op amp type circuit. This is true for the bottom example of Figure 7-108, so there is no choice but to ground the coaxial cable shield at both ends for this case.

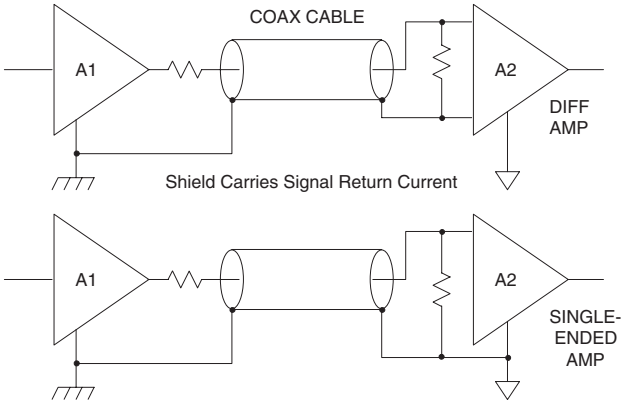


Figure 7-108: Coaxial cables can use either balanced or single-ended receivers

Input-Stage RFI Rectification Sensitivity

A well-known but poorly understood phenomenon in analog integrated circuits is *RFI rectification*, specifically as it occurs in op amps and in amps. While amplifying very small signals these devices can rectify large-amplitude, out-of-band HF signals, i.e., RFI. As a result, dc errors appear at the output in addition to the desired signal. The undesired HF signals can enter sensitive analog circuits by various means. Conductors leading into and out of the circuit provide a path for interference coupling into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling, as discussed earlier. The spurious signals appear at the amplifier inputs, along with the desired signal. The spurious signals can be several tens of mV in amplitude, however, which causes problems. Simply stated, it cannot be assumed that a sensitive, low bandwidth dc amplifier will always reject out-of-band spurious signals. While this would

be the case for a simple linear low-pass filter, op amp and in amp devices actually rectify high level HF signals, leading to nonlinearities and anomalous offsets. Methods of analysis for, as well as the prevention of, RFI rectification are discussed in this section.

Background: Op amp and In Amp RFI Rectification Sensitivity Tests

Just about all in amp and op amp input stages use emitter-coupled BJT or source-coupled FET differential pairs of some type. Depending on the device operating current, the interfering frequency and its relative amplitude, these differential pairs can behave as high frequency detectors. As will be shown, the detection process produces spectral components at the harmonics of the interference, as well at dc. It is the detected dc component of the interference that shifts amplifier bias levels, leading to inaccuracies.

The effect of RFI rectification within op amps and in amps can be evaluated with relatively simple test circuits, as described for the *RFI Rectification Test Configuration* (see page 1-38 of Reference 10). In these tests, an op amp or in amp is configured for a gain of –100 (op amp), or 100 (in amp), with dc output measured after a 100 Hz low-pass filter, preventing interference from other signals. A 100 MHz, 20 mV p-p signal is the test stimulus, chosen to be well above test device frequency limits. In operation, the test evaluates dc output shift observed under stimulus presence. While an ideal dc shift for this measurement would be zero, the actual dc shift of a given part indicates the relative RFI rectification sensitivity. Devices using both BJT and FET technologies can be tested by this method, as can devices operating at either low or high supply current levels.

In the original op amp test device set of Reference 10, some FET-input devices (OP80, OP42, OP249 and AD845) exhibited no observable shift in their output voltages, while several others showed shifts of less than 10 μV referred to the input. Of the BJT-input op amps, the amount of shift decreased with increasing device supply current. Only two devices showed no observable output voltage shift (AD797 and AD827), while others showed shifts of less than 10 μV referred to the input (OP200 and OP297). For other op amps, it is to be expected that similar patterns would be shown under such testing.

From these tests, some generalizations on RFI rectification can be made. First, device susceptibility appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibit greatest output voltage shift. Second, Ics with FET-input stages appeared to be less susceptible to rectification than those with BJTs. Note that these points are independent of whether the device is an op amp or an in amp. In practice this means that the lower power op amps *or* in amps will tend to be more susceptible to RFI rectification effects. And, FET-input op amps (or in amps) will tend to be *less* susceptible to RFI, especially those operating at higher currents.

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and thus it is inherently more linear than that of BJTs.

For the case of the lower supply current devices, transistors in the circuit are biased well below their peak f_T collector currents. Although the ICs may be constructed on processes whose device f_Ts can reach hundreds of MHz, charge transit times increase, when transistors are operated at low current levels. The impedance levels used also make RFI rectification in these devices worse. In low power op amps, impedances are on the order of hundreds to thousands of kΩs, whereas in moderate supply-current designs impedances might be no more than just a few kΩ. Combined, these factors tend to degrade a low-power device's RFI rectification sensitivity.

Figure 7-109 summarizes these general observations on RFI rectification sensitivity, and is applicable to both op amps and in-amps.

- BJT input devices *rectify* readily
  - Forward-biased B-E junction
  - Exponential I-V Transfer Characteristic
- FET input devices less sensitive to rectifying
  - Reversed-biased p-n junction
  - Square-law I-V Transfer Characteristic
- Low I_{supply} devices versus High I_{supply} devices
  - Low I_{supply} $\Rightarrow$ Higher rectification sensitivity
  - High I_{supply} $\Rightarrow$ Lower rectification sensitivity

Figure 7-109: Some general observations on op amp and in amp input stage RFI rectification sensitivity

An Analytical Approach: BJT RFI Rectification

While lab experiments can demonstrate that BJT-input devices exhibit greater RFI rectification sensitivity than comparable devices with FET inputs, a more analytical approach can also be taken to explain this phenomenon.

RF circuit designers have long known that p-n junction diodes are efficient rectifiers because of their nonlinear I-V characteristics. A spectral analysis of a BJT transistor current output for a HF sinewave input reveals that, as the device is biased closer to its "knee," nonlinearity increases. This, in turn, makes its use as a detector more efficient. This is especially true in low power op amps, where input transistors are biased at very low collector currents.

A rectification analysis for the collector current of a BJT has been presented in Reference 10, and will not be repeated here except for the important conclusions. These results reveal that the original quadratic second-order term can be simplified into a frequency-dependent term, $\Delta i_c(ac)$, at twice the input frequency and a dc term, $\Delta i_c(dc)$. The latter component can be expressed as noted in Eq. 7-14, the final form for the rectified dc term:

$$\Delta i_C\,(DC) = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} \qquad \text{Eq. 7-14}$$

This expression shows that the dc component of the second-order term is directly proportional to the *square* of the HF noise amplitude V_X, and, also, to I_C, the quiescent collector current of the transistor. To illustrate this point on rectification, note that the change in dc collector current of a bipolar transistor operating at an I_C of 1 mA with a spurious 10 mV_{peak} high frequency signal impinging upon it will be about 38 uA.

Reducing the amount of rectified collector current is a matter of reducing the quiescent current, or the magnitude of the interference. Since the op amp and in amp input stages seldom provide adjustable quiescent collector currents, reducing the level of interfering noise V_X is by far the best (and almost always the only) solution. For example, reducing the amplitude of the interference by a factor of 2, down to 5 mV_{peak} produces a net 4 to 1 reduction in the rectified collector current. Obviously, this illustrates the importance of keeping spurious HF signals away from RFI sensitive amplifier inputs.

An Analytical Approach: FET RFI Rectification

A rectification analysis for the drain current of a JFET has also been presented in Reference 10, and isn't repeated here. A similar approach was used for the rectification analysis of a FET's drain current as a function of a small voltage V_X, applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Eq. 7-15. Like the BJT, an FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given here, where the rectified dc drain current is directly proportional to the square of the amplitude of V_X, the spurious signal. However, Eq. 7-15 also reveals a very important difference between the *degree* of the rectification produced by FETs relative to BJTs.

$$\Delta i_D\,(DC) = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 7-15}$$

Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a JFET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P—parameters that are geometry and process dependent. Typically, JFETs used in the input stages of in amps and op amps are biased with their quiescent current of ~0.5 • I_{DSS}. Therefore, the change in a JFET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 7-110. In this example, a bipolar transistor with a unit emitter area of 576 μm² is compared to a unit-area JFET designed for an I_{DSS} of 20 μA and a pinch-off voltage of 2 V. Each device is biased at 10 μA and operated at T_A = 25°C.

- BJT:
  Emitter area = 576 μm²
  I_C = 10μA
  V_T = 25.68mV @ 25°C

$$\Delta i_C = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} = \frac{V_X^2}{264}$$

- JFET:
  I_{DSS} = 20μA (Z/L=1)
  V_P = 2V
  I_D = 10μA

$$\Delta i_D = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} = \frac{V_X^2}{400 \times 10^3}$$

- Conclusion: BJTs ~1500 more sensitive than JFETs

Figure 7-110: Relative sensitivity comparison – BJT versus JFET

The important result is that, under identical quiescent current levels, the change in collector current in bipolar transistors is about 1500 times greater than the change in a JFET's drain current. This explains why FET-input amplifiers behave with less sensitivity to large amplitude HF stimulus. As a result, they offer more RFI rectification immunity.

What all this boils down to is this: Since a user has virtually no access to the amplifier's internal circuitry, the prevention of IC circuit performance degradation due to RFI is left essentially to those means which are external to the ICs.

As the analysis above shows, regardless of the amplifier type, *RFI rectification is directly proportional to the square of the interfering signal's amplitude*. Therefore, to minimize RFI rectification in precision amplifiers, the level of interference must be reduced or eliminated, *prior to the stage*. The most direct way to reduce or eliminate the unwanted noise is by proper filtering.

This topic is covered in the section immediately following.

Reducing RFI Rectification within Op Amp and In Amp Circuits

EMI and RFI can seriously affect the dc performance of high accuracy analog circuits. Because of their relatively low bandwidth, precision op amps and in amps simply won't accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into a precision amplifier through either its input, output, or power supply pins, they can be internally rectified by various amplifier junctions, ultimately causing an undesirable dc offset at the output. The previous theoretical discussion of this phenomenon has shown its basic mechanisms. The logical next step is to show how proper filtering can minimize or eliminate these errors.

Elsewhere in this chapter we have discussed how proper supply decoupling minimizes RFI on IC power pins. Further discussion is required with respect to the amplifier inputs and outputs, *at the device level*. It is assumed at this point that system level EMI/RFI approaches have already been implemented, such as an RFI-tight enclosure, properly grounded shields, power rail filtering, and so forth. The steps following can be considered as circuit-level EMI/RFI prevention.

Op Amp Inputs

The best way to prevent input stage rectification is to use a low-pass filter located close to the op amp input as shown in Figure 7-111. In the case of the inverting op amp at the left, filter capacitor C is placed between equal-value resistors R1-R2. This results in a simple corner frequency expression, as shown in the figure. At very low frequencies or dc, the closed loop gain of the circuit is –R3/(R1+R2). Note that C cannot be connected directly to the inverting input of the op amp, since that would cause instability. The filter bandwidth can be chosen at least 100 times the signal bandwidth to minimize signal loss.

For the noninverting case on the right, capacitor C can be connected directly to the op amp input as shown, and an input resistor with a value "R" yields the same corner frequency as the inverting case. In both cases low inductance chip-style capacitors should be used, such as NP0 ceramics. The capacitor should in any case be free of losses or voltage coefficient problems, which limits it to either the NP0 mentioned, or a film type.

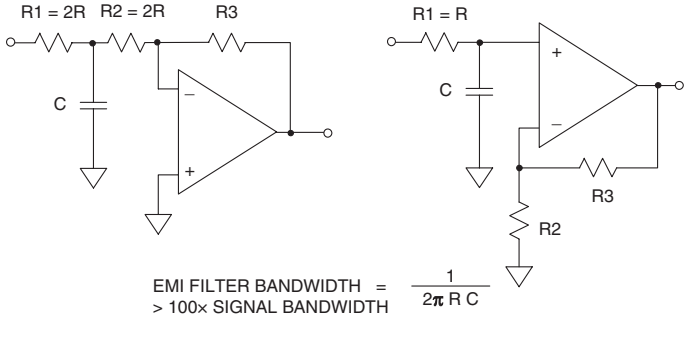


Figure 7-111: Simple EMI/RFI noise filters for op amp circuits

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100 Ω at 10 MHz to 100 MHz. This requires a large value capacitor to attenuate lower frequencies.

In Amp Inputs

Precision in amps are particularly sensitive to dc offset errors due to the presence of CM EMI/RFI. This is very much like the problem in op amps. And, as is true with op amps, the sensitivity to EMI/RFI is more acute with the lower power in amp devices.

A general-purpose approach to proper filtering for device level application of in amps is shown in Figure 7-112. In this circuit the in amp could, in practice, be any one of a number of devices. The relatively complex balanced RC filter preceding the in amp performs all of the high frequency filtering. The in amp would be programmed for the gain required in the application, via its gain-set resistance (not shown).

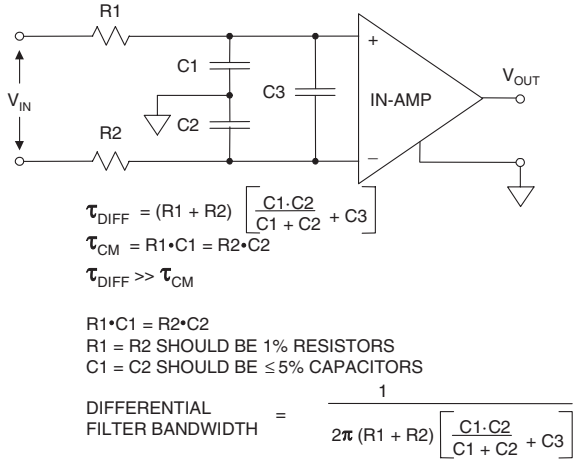
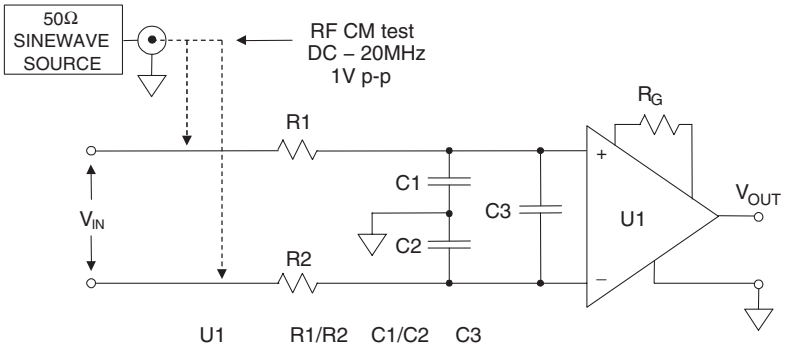


Figure 7-112: A general-purpose common-mode/ differential-mode RC EMI/RFI filter for in amps

Within the filter, note that fully balanced filtering is provided for both CM (R1-C1 and R2-C2) as well as differential mode (DM) signals (R1+R2, and C3 ‖ the series connection of C1-C2). If R1-R2 and C1-C2 aren't well matched, some of the input common-mode signal at V_{IN} will be converted to a differential mode signal at the in amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. Also, to aid this matching, R1 and R2 should be 1% metal film resistors. It is assumed that the source resistances seen at the V_{IN} terminals are low with respect to R1-R2, and matched. In this type of filter, C3 should be chosen much larger than C1 or C2 (C3 ≥ C1, C2), in order to suppress spurious differential signals due to CM⇒DM conversion resulting from mismatch of the R1-C1 and R2-C2 time constants.

The overall filter bandwidth should be at least 100 times the input signal bandwidth. Physically, the filter components should be symmetrically mounted on a PC board with a large area ground plane and placed close to the in amp inputs for optimum performance.

Figure 7-113 shows a family of these filters, as suited to a range of different in amps. The RC components should be tailored to the different in amp devices, as per the table. These filter components are selected for a reasonable balance of low EMI/RFI sensitivity and a low increase in noise (vis-à-vis that of the related in amp, without the filter).



U1	R1/R2 1%	C1/C2 ≤5%	C3 10%
AD620/621/622	4.02k	1nF	47nF
AD623	10k	1nF	22nF
AD627	20k	1nF	22nF

Figure 7-113: Flexible common-mode and differential-mode RC EMI/RFI filters are useful with the AD620 series, the AD623, AD627, and other in amps

To test the EMI/RFI sensitivity of the configuration, a 1 V p-p CM signal can be applied to the input resistors, as noted. With a typically used in amp such as the AD620 working at a gain of 1000, the maximum RTI input offset voltage shift observed was 1.5 µV over the 20 MHz range. In the AD620 filter example, the differential bandwidth is about 400 Hz.

Common-mode chokes offer a simple, one-component EMI/RFI protection alternative to the passive RC filters, as shown in Figure 7-114.

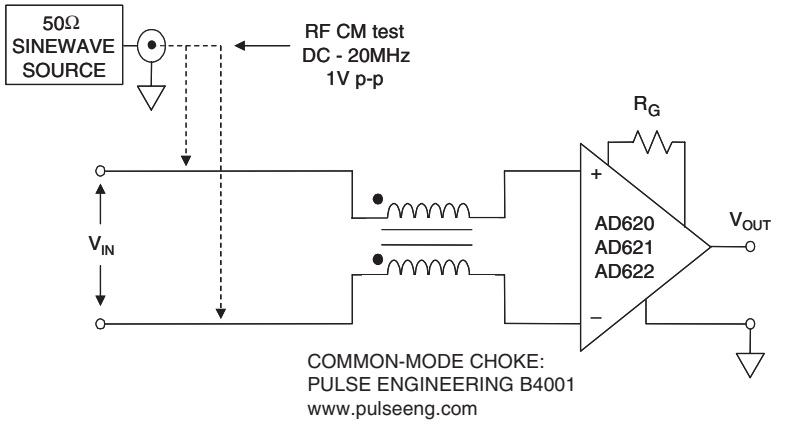


Figure 7-114: For simplicity as well as lowest noise EMI/RFI filter operation, a common-mode choke is useful with the AD620 series in amp devices

In addition to being a low component count approach, choke-based filters offer low noise, by dispensing with the resistances. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 7-114 is a Pulse Engineering B4001. The maximum RTI offset shift measured from dc to 20 MHz at G = 1000 was 4.5 µV. Either an off-the-shelf choke such as the B4001 can be used for this filter, or, alternately one can be constructed. Since balance of the windings is important, bifilar wire is suggested. The core material must of course operate over the expected frequency band. Note that, unlike the Figure 7-113 family of RC filters, a choke-only filter offers no differential filtration. Differential mode filtering can be optionally added, with a second stage following the choke, by adding the R1-C3-R2 connections of Figure 7-112.

For further information on in amp EMI/RFI filtering, see References 10, and 12 – 15.

Amplifier Outputs and EMI/RFI

In addition to filtering the input and power pins, amplifier *outputs* also need to be protected from EMI/RFI, especially if they must drive long lengths of cable, which act as antennas. RF signals received on an output line can couple back into the amplifier input where it is rectified, and appears again on the output as an offset shift.

A resistor and/or ferrite bead, or both, in series with the output is the simplest and least expensive output filter, as shown in Figure 7-115 (upper circuit).

Adding a resistor-capacitor-resistor "T" circuit as shown in Figure 7-115 (lower circuit) improves this filter with just slightly more complexity. The output resistor and capacitor divert most of the high frequency energy away from the amplifier, making this configuration useful even with low power active devices. Of course, the time constant of the filter parts must be chosen carefully, to minimize any degradation of the desired output signal. In this case the RC components are chosen for an approximate 3 MHz signal bandwidth, suitable for instrumentation or other low bandwidth stages.

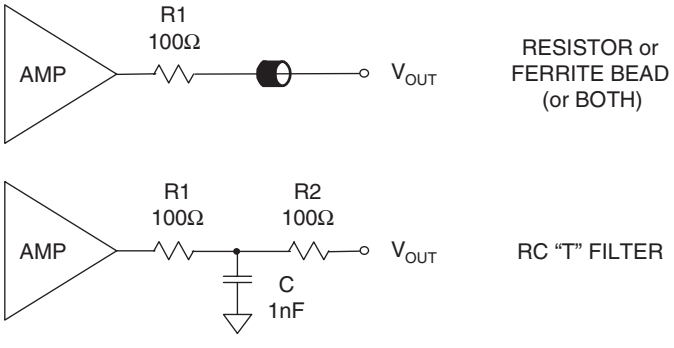


Figure 7-115: Op amp and in amp outputs should be protected against EMI/RFI, particularly if they drive long cables.

Printed Circuit Board Design for EMI/RFI Protection

This section summarizes general points on EMI/RFI with respect to the printed circuit board (PCB) layout. It complements earlier chapter discussions on general PCB design techniques. When a PCB design has not been optimized in terms of EMI/RFI, system performance can be compromised. This is true not only for signal-path performance, but also for the system's susceptibility to EMI, plus the degree of EMI radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

To summarize earlier points of this section, a real-world PCB layout may allow multiple paths through which high-frequency noise can couple/radiate into and/or out of the circuit.

This is especially true for digital circuitry, operating at high *edge rates*. It is the rapid changes of logic state ($1 \Rightarrow 0$ or $0 \Rightarrow 1$), i.e., the edge rate that contains the HF energy which can easily radiate as EMI. While similar points are applicable to precision high-speed analog or mixed analog/digital circuits, logic devices are by far the worst potential EMI offenders. Identifying critical circuits and paths helps in designing the PCB for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

Carefully Choose Logic Devices

Logic-family speaking, a key point in minimizing system noise problems is to *choose devices no faster than actually required by the application*. Many designers assume that faster is always better—fast logic is better than slow, high bandwidth amplifiers better than low bandwidth, and fast DACs and ADCs are better, even if the speed isn't required by the system. Unfortunately, faster is *not* better, and actually may be worse for EMI concerns.

Many fast DACs and ADCs have digital inputs and outputs with edge rates in the 1 ns/V region. Because of this wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 ns to 3 ns. These high speed data converters and amplifiers are thus easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, and so forth. With some of these high speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. A ferrite bead just before the local decoupling capacitor is very effective in filtering high frequency noise on supply lines. Of course, with circuits requiring bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

Design PCBs Thoughtfully

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution. Critical signal paths should be routed by hand, to avoid undesired coupling and/or emissions.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with

signal crossovers, and so forth. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes, nor analog and digital power planes.

Designing Controlled Impedances Traces on PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141 (see Reference 16).

Note that following figures use the term "ground plane." It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 7-116. This type of transmission line might be a signal wire used within a breadboard, for example. It is composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.

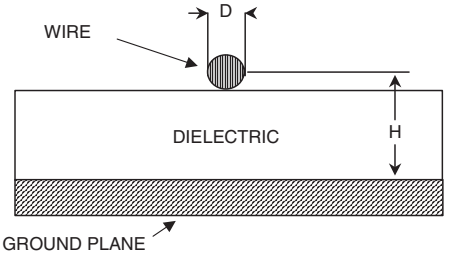


Figure 7-116: A wire microstrip transmission line with defined impedance is formed by an insulated wire spaced from a ground plane

The impedance of this line in ohms can be estimated with Eq. 7-16. Here D is the conductor diameter, H the wire spacing above the plane, and ε_r the dielectric constant.

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{D}\right] \qquad \text{Eq. 7-16}$$

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141 (see Reference 16), but information on two popular examples is shown here.

Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these is accurate?" is an extremely pertinent question. The unfortunate answer is, *none is perfectly so.* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 16, but even these come with application caveats.

Reference 17 has evaluated the Reference 16 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. Reference 18 also evaluates the Reference 16 equations, offering an alternative and even more complex set (see Reference 19). The equations quoted below are from Reference 16, and offered here as a starting point for a design, subject to further analysis, testing, and design verification. The bottom line is, study carefully and take PCB trace impedance equations with a proper dose of salt.

Microstrip PCB transmission lines

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip,* or more simply, *microstrip*.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 7-117.

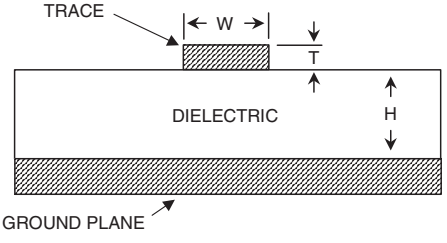


Figure 7-117: A microstrip transmission line with defined impedance is formed by a PCB trace of appropriate geometry, spaced from a ground plane

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 7-17 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant ε_r, the characteristic impedance is:

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \qquad \text{Eq. 7-17}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 7-18.

$$C_O(pF/in) = \frac{0.67(\varepsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \qquad \text{Eq. 7-18}$$

As an example including these calculations, a 2-layer board might use 20 mil wide (W), 1 ounce (T = 1.4) copper traces separated by 10 mil (H) FR-4 (ε_r = 4.0) dielectric material. The resulting impedance for this microstrip would be about 50 Ω. For other standard impedances, for example the 75 Ω video standard, adjust "W" to about 8.3 mils.

Some Microstrip Rules of Thumb

This example touches an interesting and quite handy point. Reference 17 discusses a useful rule of thumb pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50 Ω (as in the first example, with W = 20 mils).

Careful readers will note that Eq. 7-17 predicts Z_o to be about 46 Ω, generally consistent with accuracy quoted in Reference 17 (>5%). The IPC microstrip equation is most accurate between 50 Ω and 100 Ω, but is substantially less so for lower (or higher) impedances. Reference 20 gives tabular results of various PCB industry impedance calculator tools.

The propagation delay of the microstrip line can also be calculated, as per Eq. 7-19. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 21). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given ε_r), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}\,(\text{ns/ft}) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-19}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

$$t_{pd}\,(\text{ps/in}) = 85\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-20}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional rules of thumb can be useful in designing the timing of signals across PCB trace runs.

Symmetric Stripline PCB Transmission Lines

A method of PCB design preferred from many viewpoints is a multilayer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 7-118. The low impedance ac ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

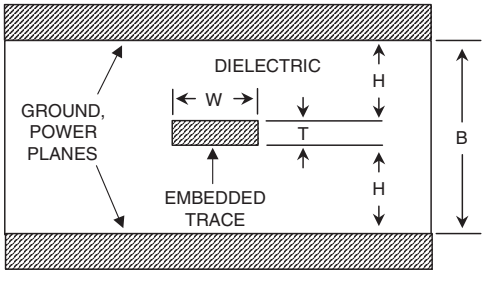


Figure 7-118: A symmetric stripline transmission line with defined impedance is formed by a PCB trace of appropriate geometry embedded between equally spaced ground and/or power planes

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.

The characteristic impedance of this arrangement is again dependent upon geometry and the ε_r of the PCB dielectric. An expression for Z_O of the stripline transmission line is:

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right] \qquad \text{Eq. 7-21}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to 2H + T. Reference 17 indicates that the accuracy of this Reference 16 equation is typically on the order of 6%.

Another handy rule of thumb for the symmetric stripline in an $\varepsilon_r = 4.0$ case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50 Ω. Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in as shown in Eq. 7-22.

$$C_O(pF/in) = \frac{1.41(\varepsilon_r)}{\ln[3.81H/(0.8W + T)]} \qquad \text{Eq. 7-22}$$

The propagation delay of the symmetric stripline is shown in eq. 7-23.

$$t_{pd}(ns/ft) = 1.017\sqrt{\varepsilon_r} \qquad \text{Eq. 7-23}$$

or, in terms of ps:

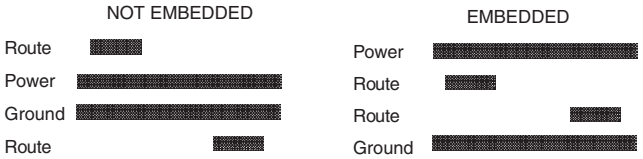
$$t_{pd}(ps/in) = 85\sqrt{\varepsilon_r} \qquad \text{Eq. 7-24}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.

Some Pros and Cons of Embedding Traces

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There are, of course, many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage—the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 7-119.



- Advantages
  - Signal traces shielded and protected
  - Lower impedance, thus lower emissions and crosstalk
  - Significant improvement > 50MHz
- Disadvantages
  - Difficult prototyping and troubleshooting
  - Decoupling may be more difficult
  - Impedance may be too low for easy matching

Figure 7-119: The pros and cons of not embedding versus the embedding of signal traces in multilayer PCB designs

Multilayer PCBs can be designed *without* the use of embedded traces, as shown in the left cross-sectional example. This embedded case could be considered as a doubled two-layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This nonembedded arrangement will have greater emissions and susceptibility to external signals, vis-à-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision of embedded versus not-embedded for the PCB design becomes a trade-off, in this case one of reduced emissions versus ease of testing.

Transmission Line Termination Rule of Thumb

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. A good rule of thumb to determine when this is necessary is as follows: *Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster*). For example, a 2-inch microstrip line over an $E_r = 4.0$ dielectric would have a delay of ~270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500 ps. A more conservative rule is to use a 2-inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, termination should be used.

For example, PCB tracks for high-speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

In the analog domain, it is important to note that this same 2-inch/nanosecond rule of thumb should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime t_r is related to this f_{max}. This limiting risetime, t_r, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 7-25}$$

The maximum PCB track length is then calculated by multiplying t_r by 2-inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a risetime of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required.

A general method of doing this is to use a series R at a logic driver output, and a shunt C at a CMOS gate input. The series resistance and the net input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 10 pF. Locate the series resistor close to the driving gate, adding an additional small capacitance, as needed. The resistor minimizes transient switching currents, and may also eliminate the necessity for transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the source and sink current which must flow through the resistor. Use of CMOS logic will simplify this, since the input currents are so low.

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Some useful EMC and signal integrity related URLs:

Eric Bogatin website, www.bogatinenterprises.com

Chip Center's "Signal Integrity" page, www.chipcenter.com/signalintegrity

Kimmel Gerke Associates website, www.emiguru.com

Henry Ott website, www.hottconsultants.com

IEEE EMC website, www.ewh.ieee.org/soc/emcs

Mark Montrose website, www.montrosecompliance.com/index.html

Tim Williams website, www.elmac.co.uk