Digital potentiometer autonulls op amp

STEPHEN WOODWARD, UNIVERSITY OF NORTH CAROLINA, CHAPEL HILL, NC

Op-amp applications that need the highest possible dc accuracy are generally best served by CMOS chopper-stabilized amplifiers, such as the LTC1050. But high-speed, low-noise applications may require high-performance rockets, such as the 700-MHz LT1226. So what to do for applications that need it *all*? Sometimes, a composite topology in which a bipolar amplifier provides gain-bandwidth and a CMOS chopper acts as an offset-nulling servo can do the job. Such arrangements can successfully null out offset-voltage errors. But these circuits can get messy if you also need bias-current-related error correction. The circuit in **Figure 1** offers an error-cancellation method that handles both error sources.

The circuit consists of op amp IC_1 (for example, Linear Technology's LT1226), CMOS multiplexer S_C (one-third of an HC4053), and digital potentiometer P_1 (Xicor's X9C103). The topology supports two modes of operation, as selected by the TTL/CMOS-compatible NADJ signal. NADJ=0 connects IC_1 as a standard noninverting gain block. The circuit values shown, combined with the impressive specs of the frequency-compensated LT1226, provide a gain of 1001 with bandwidth extending from dc to beyond 500 kHz and input-related noise of approximately 2 $nV\sqrt{Hz}$.

Null-adjustment mode occurs when NADJ=1 disconnects the input source and effectively causes IC_1's output to run open-loop. IC_1's output and then slews to one rail or the other, as determined by the sign of its net offset error. If $R_3=R_S-R_1||R_2$, where R_S is the dc source resistance, then IC_1's output reflects the sum of both voltage *and* current bias errors. The circuit level-shifts and filters IC_1's output and applies it to the up/down control input of P_1. This action sets up P_1's internal up/down-counter logic to increment or decrement one step, depending on the state of IC_1's output and thus on the sign of IC_1's offset. The counter step occurs on the subsequent NADJ=0 transition.

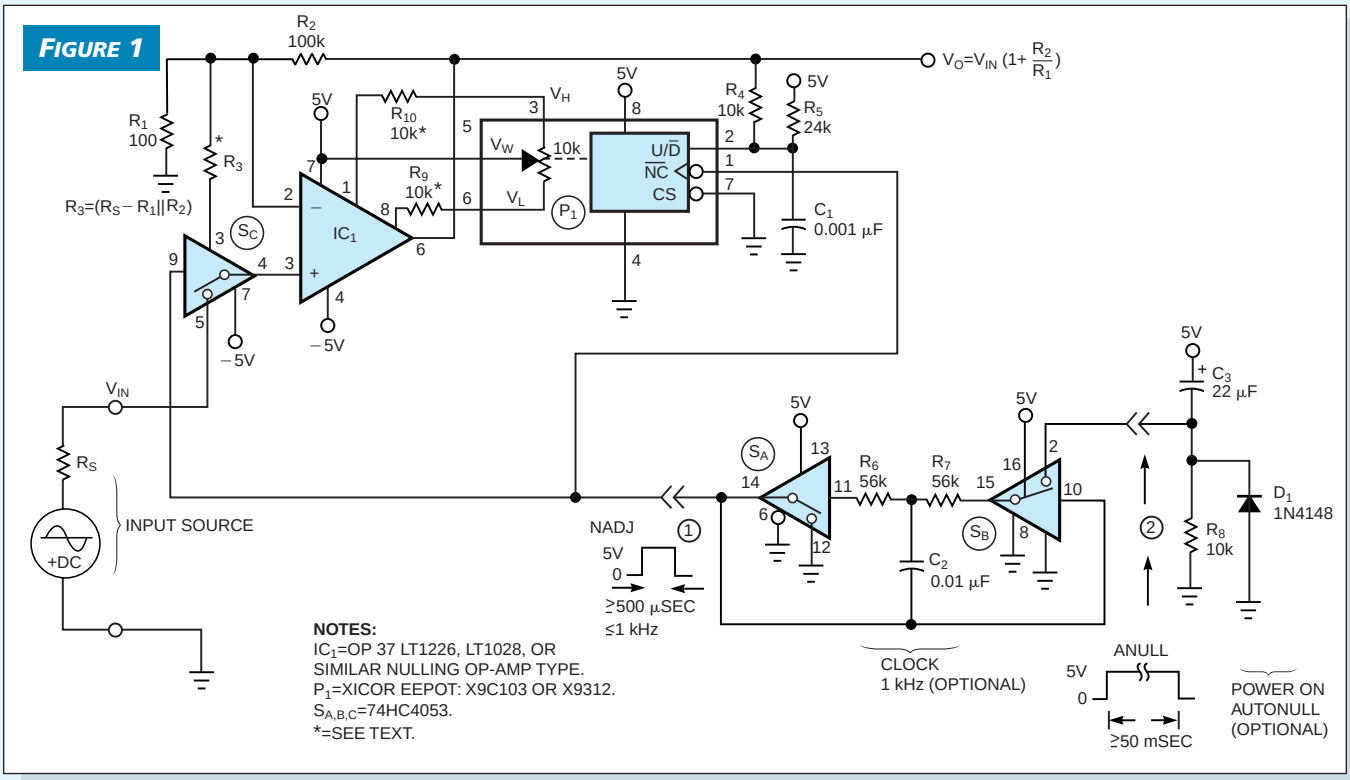
The connection of the V_L, V_W, and V_H terminals of P_1 to the nulling terminals of IC_1 closes a feedback loop that tends to push IC_1 one step toward null for every I/O cycle of NADJ. Because the X9C103 has 100 resolved settings, the technique requires a maximum of 99 NADJ pulses to complete the nulling process. After nulling, P_1 retains the final null setting in digital memory as long as the 5V supply remains connected or until the nulling process repeats. Observed performance reveals that using an OP37 consistently achieves residual-offset errors of less than 5 µV.

If it is inconvenient to provide an external NADJ clock source in a given application, you can add the S_A/S_B multivibrator at Node 1. This 1-kHz clock circuit receives its gating from the CMOS-compatible anull signal, such that anull=1 enables continuous null adjustment, and anull=0 enables normal amplifier operation. The maximum anull duration required to achieve initial null is 100 msec. If desired, you can also include D_1, R_8, and C_3 at Node 2 to provide an automatic null on each power-up cycle.

Although **Figure 1** shows an LT1226, the circuit works without modification with an OP37 and an LT1028. The circuit is also pin-compatible with the popular LT1128, OP07, OP77, OP177, and µ725 op amps. With these op amps, however, the circuit may require a slower NADJ clock rate and a longer nulling interval (increase C_2 and C_3), because of the lower gain-bandwidth product of these compensated types. The circuit can accommodate many other op-amp types with a simple change of pin connections. The circuit can handle 15V positive-rail operations by substituting an X9312 for the X9C103 with no other changes. (DI #2262). EDN

To Vote For This Design, Circle No. 348

FIGURE 1



Have your cake (high speed) and eat it (low dc errors) too, with this autonulling circuit, using a digitally controlled potentiometer.