Differential input to differential output circuit using a fully-differential amplifier

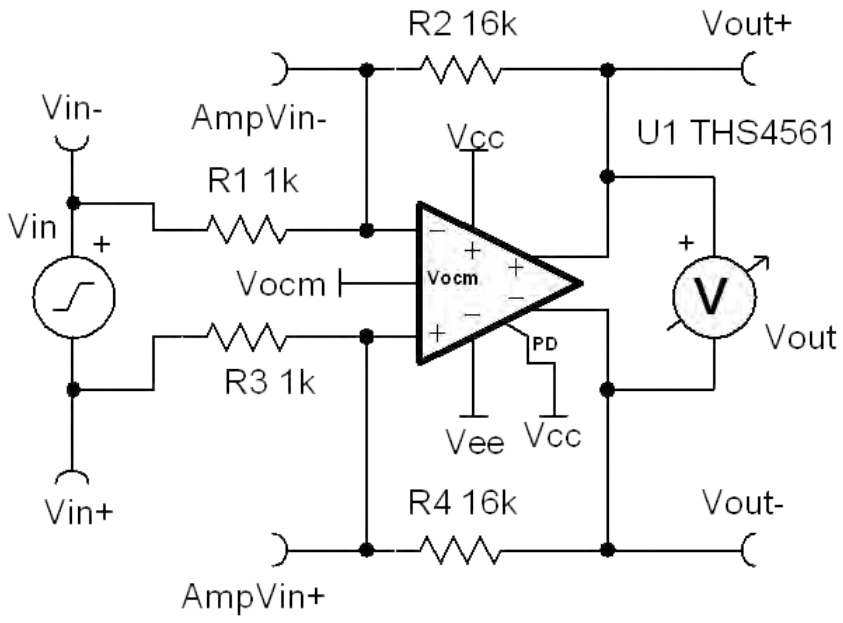
Design Goals

Input	Output	Supply	
Differential	Differential	V_{cc}	V_{ee}
1Vpp	16Vpp	10V	0V

Output Common-Mode	3dB Bandwidth	AC Gain (Gac)
5V	3MHz	16V/V

Design Description

This design uses a fully differential amplifier (FDA) as a differential input to differential output amplifier.



Design Notes

1. The ratio R2/R1, equal to R4/R3, sets the gain of the amplifier.
2. For a given supply, the output swing for and FDA is twice that of a single ended amplifier. This is because a fully differential amplifier swings both terminals of the output, instead of swinging one and fixing the other to either ground or a Vref. The minimum voltage of an FDA is therefore achieved when Vout+ is held at the negative rail and Vout- is held at the positive rail, and the maximum is achieved when Vout+ is held at the positive rail and Vout- is held at the negative rail.
3. FDAs are useful for noise sensitive signals, since noise coupling equally into both inputs will not be amplified, as is the case in a single ended signal referenced to ground.
4. The output voltages will be centered about the output common-mode voltage set by Vocm.
5. Both feedback paths should be kept symmetrical in layout.

Design Steps

- Set the ratio R2/ R1 to select the AC voltage gain. To keep the feedback paths balanced,

  $R_1 = R_3 = 1K\Omega$ (STANDARDVALUE)

  $R_2 = R_4 = R_1 \bullet (G_{AC}) = 1K\Omega \bullet \left(16\frac{V}{V}\right) = 16K\Omega$ (STANDARDVALUE

- Given the output rails of 9.8V and 0.2V for Vs = 10V, verify that 16Vpp falls within the output range available for V_{ocm} = 5V.

  In normal operation:

  $AMPV_{IN+} = AMPV_{IN-}$

  $V_{OUT+} - V_{OCM} = V_{OCM} - V_{OUT-}$

  $V_{OUT} = V_{OUT+} - V_{OUT-}$

- Rearrange to solve for each output voltage in edge conditions

  $V_{OUT-} = 2V_{OCM} - V_{OUT+}$

  $V_{OUT-} = V_{OUT+} - V_{OUT}$

  $2V_{OUT+} = 2V_{OCM} + V_{OUT}$

  $V_{OUT+} = V_{OCM} + \frac{V_{OUT}}{2}$

  $V_{OUT-} = V_{OCM} - \frac{V_{OUT}}{2}$

- Verifying for Vout = +8V and Vocm = +5V,

  $V_{OUT+} = 5 + \frac{8}{2} = 9V < 9.8V$

  $V_{OUT-} = 5 - \frac{8}{2} = 1V > 0.2V$

- Verifying for Vout = -8V and Vocm = +5V,

  $V_{OUT+} = 5 + \frac{-8}{2} = 1V > 0.2V$

  $V_{OUT-} = 5 - \frac{-8}{2} = 9V > 9.8V$

Note that the maximum swing possible is:

$(9.8V - 0.2V) - (0.2V - 9.8V) = 18.4V_{PP}$, OR $\pm 9.4V$

- Use the input common mode voltage range of the amplifier and the feedback resistor divider to find the signal input range when the output range is 1V to 9V. Due to symmetry, calculation of one side is sufficient.

$MIN(AMPV_{IN+}) = MIN(AMPV_{IN-}) = VEE - 0.1V = -0.1V$

$MAX(AMPV_{IN+}) = MAX(AMPV_{IN-}) = VCC - 1.1V = 8.9V$

$$\frac{AMPV_{IN-} - V_{IN-}}{R_1} = \frac{V_{OUT+} - AMPV_{IN-}}{R_2}$$

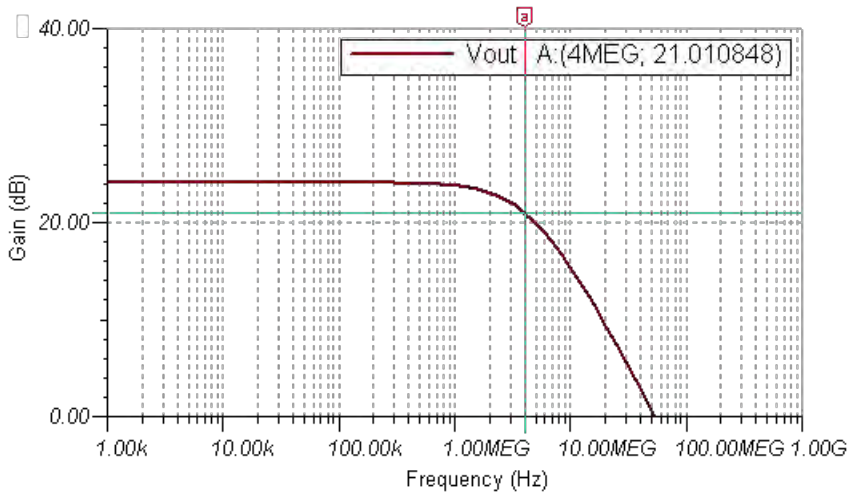
$$V_{IN-} = AMPV_{IN-} - \frac{V_{OUT+} - AMPV_{IN-}}{\frac{R_2}{R_1}}$$

$$MIN(V_{IN-}) = -0.1V - \frac{9V - (-0.1V)}{16\,\frac{V}{V}} = -0.65V$$

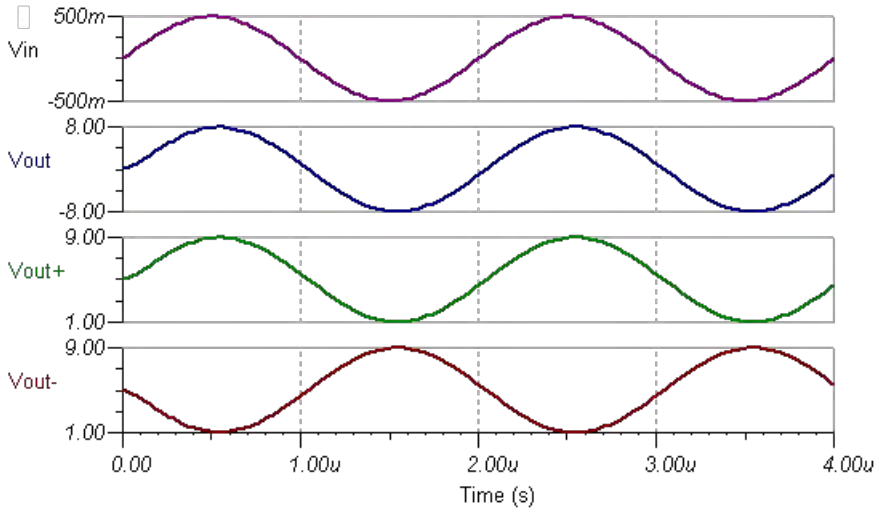
$$MAX(V_{IN-}) = 8.9V + \frac{8.9V - 1V}{16\frac{V}{V}} = 9.4V$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the TIDA-01036 tool folder for more information.

Design Featured Op Amp

THS4561	
V_{ss}	3V to 13.5V
V_{inCM}	Vee-0.1V to Vcc-1.1V
V_{out}	Vee+0.2V to Vcc-0.2
V_{os}	TBD
I_q	TBD
I_b	TBD
UGBW	70MHz
SR	4.4V/µs
#Channels	1
http://www.ti.com/product/THS4561	

Design Alternate Op Amp

THS4131	
V_{ss}	5V to 33V
V_{inCM}	Vee+1.3V to Vcc-0.1V
V_{out}	Varies
V_{os}	2mV
I_q	14mA
I_b	2uA
UGBW	80MHz
SR	52V/µs
#Channels	1
http://www.ti.com/product/THS4131	

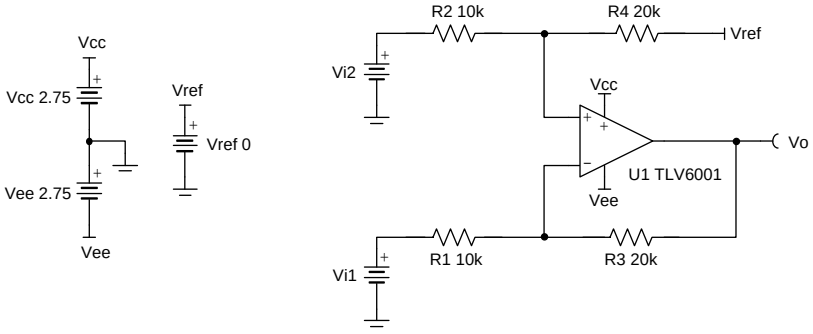
Difference amplifier (subtractor) circuit

Design Goals

Input (V_{i2}-V_{i1})		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	V_{oMin}	V_{oMax}	dB	V_{cc}	V_{ee}	V_{ref}
–1.25V	1.25V	–2.5V	2.5V	50	2.75V	–2.75V	0V

Design Description

This design inputs two signals, V_{i1} and V_{i2}, and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.



Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to R_3 and R_4. Adding capacitors in parallel with R_3 and R_4 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

Design Steps

The complete transfer function for this circuit is shown below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(\frac{R_4}{R_2+R_4}\right) \times \left(1+\frac{R_3}{R_1}\right) + Vref \times \left(\frac{R_2}{R_2+R_4}\right) \times \left(1+\frac{R_3}{R_1}\right)$$

If $R_1 = R_2$ and $R_3 = R_4$ the transfer function for this circuit simplifies to the following equation.

$$V_o = (V_{i2} - V_{i1}) \times \frac{R_3}{R_1} + Vref$$

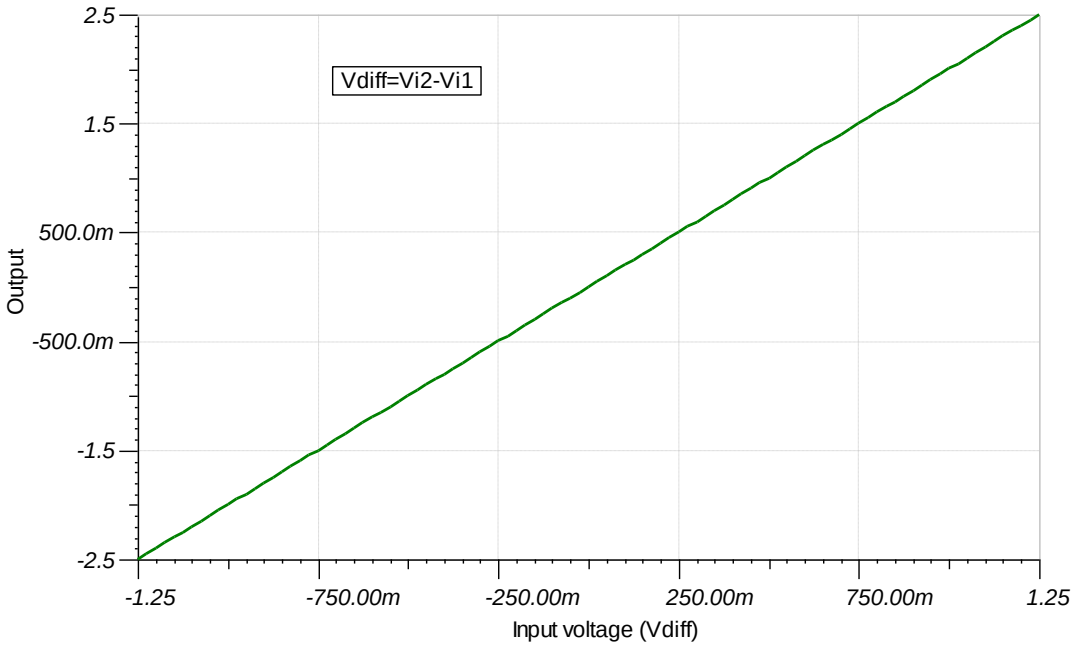
- Where the gain, G, is R_3/R_1.

1. Determine the starting value of R_1 and R_2. The relative size of R_1 and R_2 to the signal impedance of the source affects the gain error.
   $$R_1 = R_2 = 10k\Omega$$
2. Calculate the gain required for the circuit.
   $$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V-(-2.5V)}{1.25V-(-1.25V)} = 2\frac{V}{V} = 6.02dB$$
3. Calculate the values for R_3 and R_4.
   $$G = 2\frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$
4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR, α = 4. For a more probable, or typical value of CMRR, α = 0.33.
   $$CMRR_{dB} \cong 20\log10\left(\frac{1+G}{\alpha \times \varepsilon}\right)$$
   ( ) ( )
   $$\varepsilon = \frac{1+G}{\alpha \times 10^{\frac{CMRR_{dB}}{20}}} = \frac{3}{4 \times 10^{\frac{50}{20}}} = 0.024 = 0.24\% \rightarrow \text{Use } 0.1 \text{ \% resistors}$$
5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming G = 1 or G = 2. As shown above, as gain increases so does CMRR.

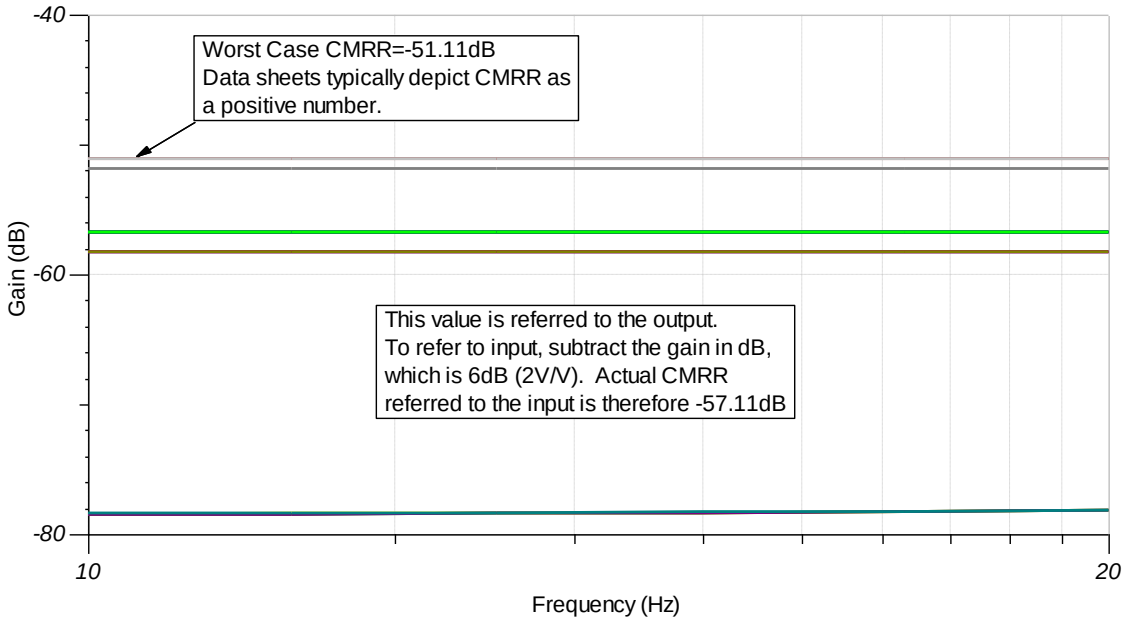
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01%=0.0001	74	95.6	77.5	99.2
0.1%=0.001	54	75.6	57.5	79.2
0.5%=0.005	40	61.6	43.5	65.2
1%=0.01	34	55.6	37.5	59.2
5%=0.05	20	41.6	23.5	45.2

Design Simulations

DC Simulation Results



CMRR Simulation Results



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC495.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs. For more information on difference amplifier CMRR, please read Overlooking the obvious: the input impedance of a difference amplifier .

Design Featured Op Amp

TLV6001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	750µV
I_q	75µA
I_b	1pA
UGBW	1MHz
SR	0.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv6001	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40µV
I_q	1.5mA
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2
www.ti.com/product/opa320	

Revision History

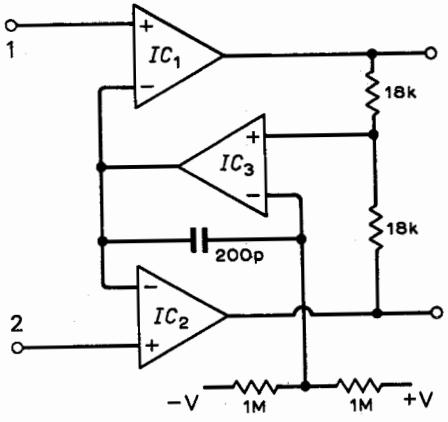
Revision	Date	Change
A	January 2019	Downscale title. Added link to circuit cookbook landing page.

Differential input and output with op-amps

This circuit uses three op-amps to provide an amplifier with differential output as well as differential input. It was designed to drive a meter with a signal of either polarity when a centre-tapped power supply was not available, but could have other uses.

The 18-kΩ resistors form a potential divider across the outputs of the complete amplifier. The voltage at the non-inverting input of IC_3 is therefore the average of the two output potentials. The divider consisting of the two 1-MΩ resistors maintains the inverting input of IC_3 at a fixed potential; IC_3 acts to keep its inputs nearly equal, as it forms part of a negative feedback loop, and therefore the average of the two output potentials, i.e. the common mode output, is determined by the resistor values.

To obtain negative differential feedback with the circuit as shown, output 1 should be connected to input 2 and output 2 to input 1, in both cases via a suitable resistor. If it is more convenient, the connections to the inputs of each op-amp could be reversed, in which case the feedback connections would be output 1 to input 1, and output 2 to input 2.



If IC_1 and IC_2 are combined in a dual op-amp, then p.c. board space will be saved, and differential temperature drift reduced. I used a 741 for IC_3 and a 747 (dual 741) for i.cs 1 and 2.

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