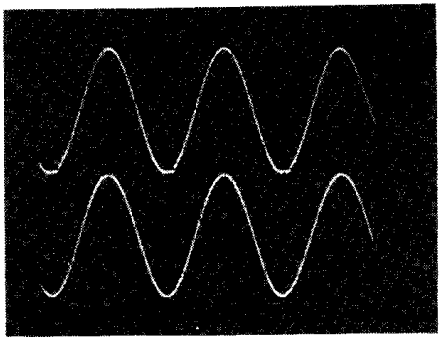
D.C. level clamp

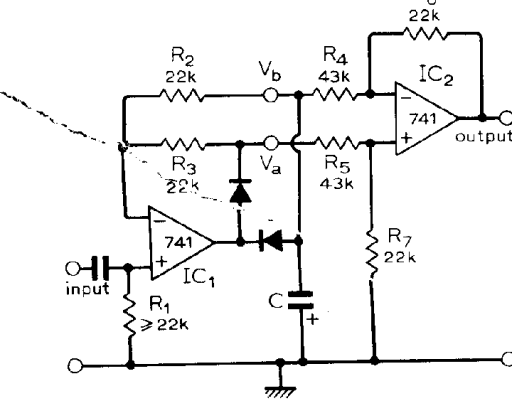
The need sometimes arises, e.g. after a stage of a.c. amplification, to clamp the minimum level of a signal voltage to a d.c. reference voltage. The circuit illustrated was developed to clamp, to the zero-volt level, signals having an amplitude of between 10mV and 10V. The familiar diode-and-capacitor clamp circuit is unsuitable here because of the diode's forward conduction characteristic.

In each cycle, the capacitor, C, charges to the peak negative value ($V_b = -V_p$) of the input voltage, V_i. The voltage V_a then follows the input voltage ($V_a = 2V_i + V_p$) while V_b remains at the level to which the capacitor was charged, decreasing only with a time constant

$$T \approx \frac{(R_4 + R_6)\, R_2\, C}{R_4 + R_6 + 2R_2}$$



Lower trace is the input signal; upper trace is the output from the restorer. Oscillogram was obtained with the circuit operating on a 150Hz signal with an amplitude of 40mV peak-to-peak.



The required voltage waveform, with its minimum d.c. level restored to zero, appears as $V_a - V_b$. A low-impedance single-ended output is provided by IC_2 and, in this case, unity gain overall.

Using a 250-μF electrolytic capacitor, the circuit clamps sinusoidal waveforms between 3Hz and 10kHz with little distortion. For use at higher frequencies, IC_1 should have a faster slew rate. Lower distortion can be achieved if IC_2 has a higher input impedance—allowing larger values of R_4 and R_5 to be used.

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