CURRENT INVERTER WITH WIDE DYNAMIC RANGE
A USEFUL ADJUNCT TO INTEGRATED-CIRCUIT LOG DEVICES

by Barrie Gilbert

The circuit described here provides an output current of opposite polarity to the input current. The output current can cover a range substantially greater than 4 decades without severe degradation of accuracy. The circuit is best-suited to drive a low-impedance load, such as an op-amp summing point.

The preferred direction of input current flow for logarithmic devices based on NPN "Paterson diode" transistor circuitry[1] is positive (from the signal source to the log-amp summing point). Unfortunately, many transducers (e.g., photomultipliers, ion chambers, chromatographs) provide a *negative* current flow, which calls for an additional inverting amplifier.*

The conventional current-to-voltage inverter (Figure 1) loads the log-amp summing point, increasing the overall "noise gain," and causing the offset voltage of the log amp to limit dynamic range at the low end (from 6+ decades down to about 3 decades). With a slight circuit change, it can be rewired as a current inverter (Figure 2), increasing the output impedance and unloading the log-amp summing point. However, dynamic range is still limited by the linear I-to-V conversion: the inverter's output rating at the high end and its V_{os} at the low end limit the practical range to about 3 decades of input current.

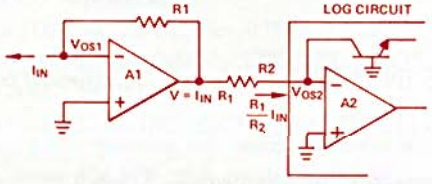

Figure 1. Current-to-voltage sign inversion. Offset error is $(|V_{os1}| + |V_{os2}|)/R_2$, adding to the signal and causing "nonlinear" logarithmic conversion at the low end.

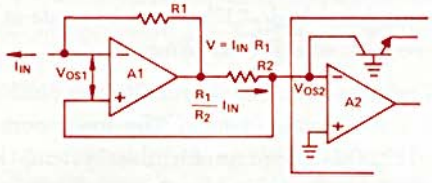

Figure 2. Linear current inverter. Offset error, V_{os1}/R_2, adds to the signal, causes nonlinear conversion for low I_{IN}.

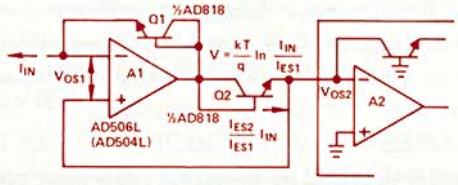

Figure 3. Logarithmic current inverter. Amplifier offset V_{os1} and V_{BE} mismatch errors affect scale factor only, result in an offset error following log conversion, independent of I_{IN} level.

Ideally, one might desire a resistance pair that changed with current, being low at high current and high at low current. Figure 3 shows such a resistance pair. The inverting-amplifier output voltage changes by a fixed amount (about 60mV) for each decade of input current change. An input/output current range of 10^6, for example, ideally requires an intermediate output voltage change of only 0.36V. Diode-connected transistor Q1 converts I_{IN} to a logarithmic output voltage; and Q2, with an (ideally) equal voltage drop, converts the voltage back to a reverse current outflow, equal to I_{IN}.

SOURCES OF ERROR

1. V_{BE} mismatch in the log transistors introduces a scaling factor equal to I_{ES2}/I_{ES1}, or, in terms of the measured ΔV_{BE}, $\exp(\Delta V_{BE_0} q/kT_0)$. Note that this factor is not fundamentally current- or temperature-dependent for well-matched and isothermal transistors, such as those in the monolithic AD818).

2. V_{os1} (the inverting op amp's offset) introduces a scale factor equal to $\exp(V_{os1} q/kT)$. It drifts with the op amp's thermal drift, at about 40ppm/μV in the vicinity of +25°C.

3. I_{os_1} (input offset current) of the op amp is translated as an offset error. Like the bias current of A2, it will be the major limiting parameter to operating range at the low end.

4. Because the salient factor in this circuit is *compression of dynamic range* (approximate log behavior would suffice), R_{EB} (emitter bulk resistance of the NPN's) doesn't seriously affect operation, since the current densities—and therefore the excess of emitter voltages (over the log term)—are nearly equal. Scale factor is determined at low I_{IN} by ΔV_{BE} and V_{os}, and at the milliampere level by R_{EB1}/R_{EB2}. This error, and the distortion of log behavior at low I_{IN} due to low β, can both be unimportant if the transistors behave alike and are thermally intimate.

IMPLEMENTATION

Almost any op-amp-dual-transistor pair would work well. A good cost/speed/accuracy compromise for wide-range I_{IN} would involve the AD506L and the AD818.† The AD818 provides good initial match and low R_{EB}. The FET-input AD506L's low bias current permits wide dynamic operating range; its low drift (10μV/°C *max*) provides a reasonably-constant scale factor. With its fast slewing rate (3V/μs *min*), speed is limited principally by small-signal behavior, even for a many-decade step change. For narrower ranges, the AD504L's† low V_{os} drift gives better gain stability vs. temperature. Fig. 3 is still preferred to Fig. 2, because the required slewing rate is at least an order of magnitude smaller for a full-scale step, which befits AD504.

†For data on the AD818, AD506, and the AD504, request **N26**.

[1] An extensive treatment of logarithmic circuitry can be found in the Analog Devices' *Nonlinear Circuits Handbook*, available for $5.95, P.O. Box 796, Norwood, MA 02062.

*Most log modules are available in two "sexes," e.g., 752N & 752P, 755N and 755P, 756N & 756P (request **N25** for information), but a user employing this approach will not have to stock both types. More important, the earliest IC log devices have been limited by available technology to the use of NPN log transistors.