Circuit simultaneously delivers square and square root of two input voltages

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This Design Idea requires inputs from the circuit in a previous Design Idea (**Reference 1**). IC_1 and IC_3 are ADG5213 quad switches with individual logic-level control inputs (**Figure 1** and **Reference 2**). With a high input, switches S_2 and S_3 are open, and switches S_1 and S_4 are closed. The switches toggle to opposite states with their control inputs low. The circuit is in the idle pretriggered condition. During the initial idle condition before a clock rising-edge trigger, Q is high and, through IC_8, holds switches S_2 and S_3 of IC_1 in the open position.

$\overline{Q}$ is low, and, through IC_7's Reset high closes IC_1's S_1 and S_4, discharging C_{T2} and C_{T4} and zeroing the input voltage to unity-gain amplifiers IC_{2D} and IC_{2C}. $\overline{Q}$ low also sets Track 2 low through IC_6 and holds IC_3's S_1 and S_4 in the open position. The circuit retains any sampled voltages from a previous operation in sample-and-hold capacitors C_{S1} and C_{S2}; these voltages appear at V_{OUTX} and V_{OUTY} through unity-gain amplifiers IC_{2A} and IC_{2B}.

Signals V_{OUTL} and V_{OUTQ} from the linear and quadratic pulse generator are at 0V during idle, holding comparator outputs IC_4 and IC_5 low. A rising trigger edge at the clock signal begins the ramp generation of V_{OUTL} and V_{OUTQ}. The Q and IC_8 outputs fall low, closing IC_1's S_2 and S_3 and ensuring that Track 2 remains low. $\overline{Q}$ rises and forces Reset low through IC_7, opening S_1 and S_4 of IC_1 and allowing C_{T2} to follow the rising V_{OUTQ} and C_{T4} to follow the rising V_{OUTL}.

When linear ramp V_{OUTL} rises to

analog input V_X, IC_4's output rises and, through IC_8, Track 1L opens S_2 of IC_1 and allows C_{T2} to hold the present level of V_{OUTQ}. In a similar manner, when quadratic ramp V_{OUTQ} rises to analog input V_Y, IC_5's output rises and, through IC_8, Track 1Q opens IC_1's S_3 and allows C_{T4} to hold V_{OUTL}'s present level. The pulse generator terminates when the ramps reach 5V. The ramps then fall back to 0V, Q returns high, and $\overline{Q}$ returns low.

The rise of Q immediately triggers IC_6 to generate a high pulse of approximately 20 µsec on Track 2 based on R_{D1} and C_{D1}. This action closes IC_3's S_1 and S_4, allowing the sampled voltages on C_{T2} and C_{T4} to transfer to C_{S1} and C_{S2} through unity-gain amplifiers IC_{2D} and IC_{2C}. Unity-gain amplifiers IC_{2A} and IC_{2B} present the C_{S1} and C_{S2} voltages at V_{OUTX} and V_{OUTY}. When Track 2 returns low, IC_3's S_1 and S_4 open, and the sampled voltages on C_{S1} and C_{S2} are retained.

The fall of $\overline{Q}$ triggers IC_7 to produce a 50-µsec delayed rise on Reset, which R_{D2} and C_{D2} time to occur after Track 2 has returned low and the sampled voltages are safely captured on C_{S1} and C_{S2}. Reset's high state closes IC_1's S_1 and S_4, discharging C_{T2} and C_{T4} in preparation for the next trigger. V_{OUTX} is the squared voltage of input V_X, and V_{OUTY} is the square root of the voltage of input V_Y. You can view the equations at www.edn.com/120301dia. EDN

REFERENCES

1 Štofka, Marián, "Positive edges trigger parabolic timebase generator," *EDN*, July 28, 2011, pg 51, http://bit.ly/yYvu3F.

2 "ADG5212/ADG5213 High Voltage Latch-up Proof, Quad SPST Switches," Analog Devices, 2011, http://bit.ly/w6XTO3.

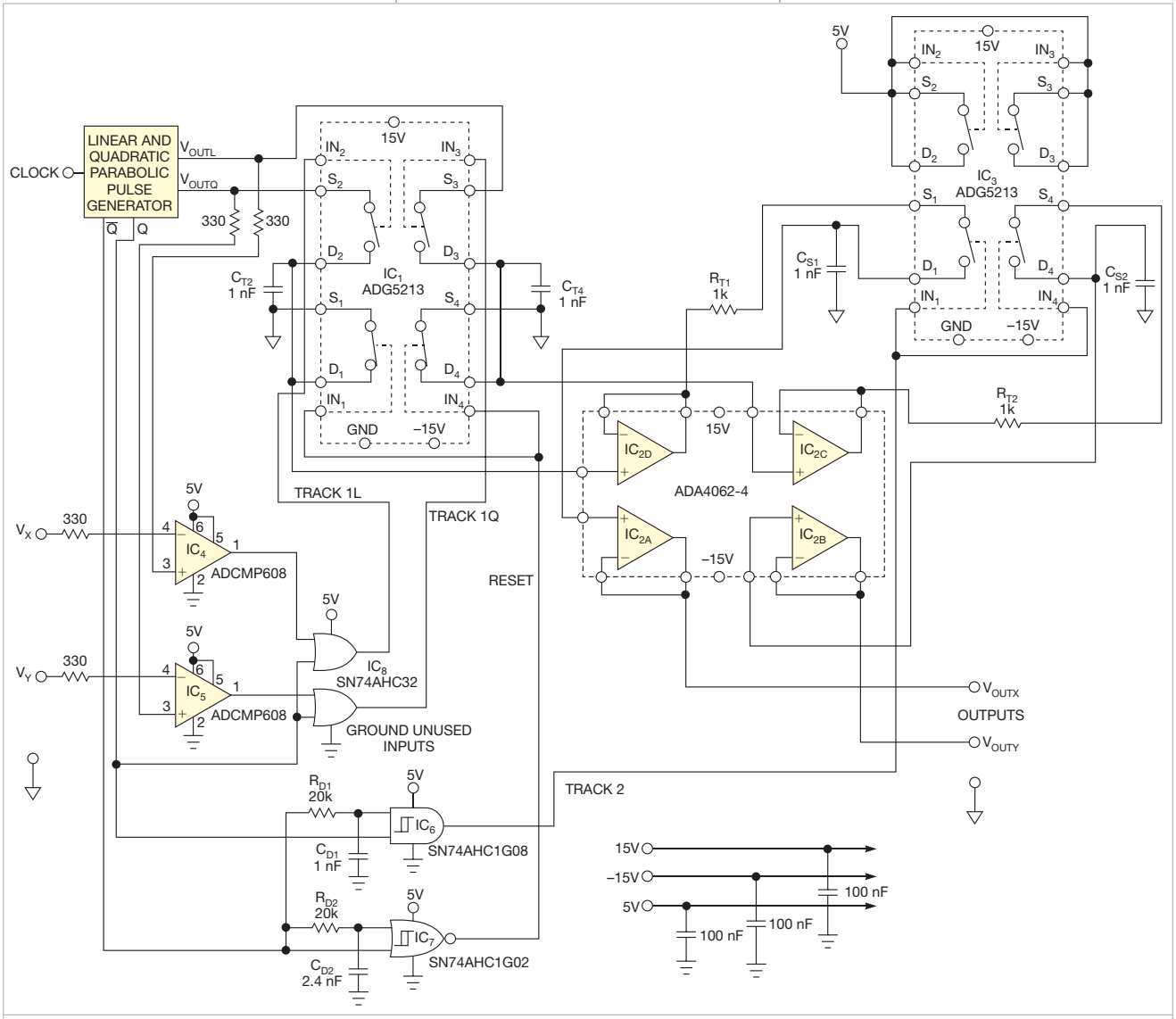

Figure 1 With this circuit, you can find the square at Channel X and the square root at Channel Y for any positive dc or slowly varying voltages of 0 to 5V.