BY MIRO OLJACA AND BONNIE C BAKER • TEXAS INSTRUMENTS

Start with the right op amp when driving SAR ADCs

USING THE RIGHT OPERATIONAL AMPLIFIER IN FRONT OF YOUR DATA CONVERTER WILL GIVE YOU GOOD PERFORMANCE. ADJUSTING COMPONENT VALUES BY PRODUCTION LOT WILL GIVE YOU THE BEST PERFORMANCE.

SAR (successive-approximation-register) ADCs (analog-to-digital converters) are playing an increasingly prominent role in the design of highly effective data-acquisition systems for automatic test equipment, instrumentation, spectrum analysis, and medical instruments. SAR ADCs make it possible to deliver high-accuracy, low-power products with excellent ac performance, such as SNR (signal-to-noise ratio) and THD (total harmonic distortion), as well as good dc performance.

For optimum SAR-ADC performance, the recommended driving circuit is an op amp in combination with an RC filter (**Figure 1**). Although this circuit commonly drives ADCs, it has the potential to create circuit-performance limitations. If you don't properly select the input resistor, R_{IN}, and the input capacitor, C_{IN}, values, the circuit could produce ADC errors. Worse yet, it could cause the amplifier to become unstable. If you ignore the op-amp open-loop output impedance and UGBW (unity-gain bandwidth), you may run into amplifier-stability issues.

The optimized ADC-driver circuit in **Figure 1** uses an op amp to separate the ADC from high-impedance signal sources. The following RC lowpass filter, R_{IN} and C_{IN}, performs functions going back to the op amp and forward to the ADC. R_{IN} keeps the amplifier stable by "isolating" the amplifier's output stage from the capacitive load, C_{IN}. C_{IN} provides a nearly perfect input source to the ADC. This input source tracks the voltage of the input signal and charges the ADC's input sampling capacitor, C_{SH}, during the converter's acquisition time.

In evaluating the circuit in **Figure 1**, you can determine the guidelines and constraints for selecting the value of R_{IN}. The op amp's open-loop output resistance, R_O, and the UGBW or the unity crossover frequency, f_U, as well as the value of C_{IN}, govern this issue (**Reference 1** and **Figure 2**). After defining the design formulas for R_{IN}, you can determine the value of C_{IN}. The ADC's acquisition time and input sample-and-hold capacitance, C_{SH}, as well as R_{IN}, influence the value of C_{IN}.

Once you understand how this circuit operates, you can establish the criteria for a stable system and define an appropriate design strategy. A proof of concept uses two sample circuits. The first is relatively stable; the second is marginally stable.

OP-AMP STABILITY WITH R_{IN} AND C_{IN}

The ADC in **Figure 1** cycles through two stages while converting the input signal to a digital representation. Initially, the converter must acquire the input signal. After acquiring the signal, the converter changes the sampled information, or "snapshot," of the input signal to a digital representation. A critical part of this process is to obtain an accurate snapshot of the input signal. If this ADC-data-conversion process is to run smoothly, the driving amplifier must charge the input capacitor to the proper value and maintain stability during the ADC's acquisition time.

You can determine the stability of an amplifier with a Bode plot, a tool that helps you approximate the magnitude of an amplifier's open- and closed-loop-gain transfer functions. In **Figure 2**, the units along the Y axis describe the gain in decibels of the amplifier in **Figure 1**. The units along the X axis describe the frequency in log, hertz of the open- and closed-loop-gain curves.

If the closure rate of the closed- and open-loop-gain curves

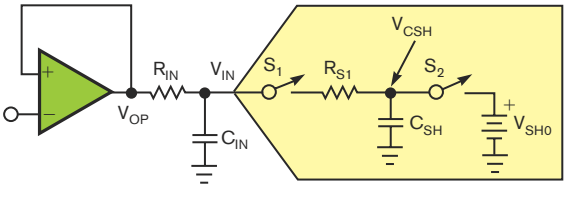

Figure 1 In this circuit, R_{IN} "isolates" C_{IN} from the op-amp output stage. C_{IN} provides a charge reservoir for the SAR ADC during the sampling period.

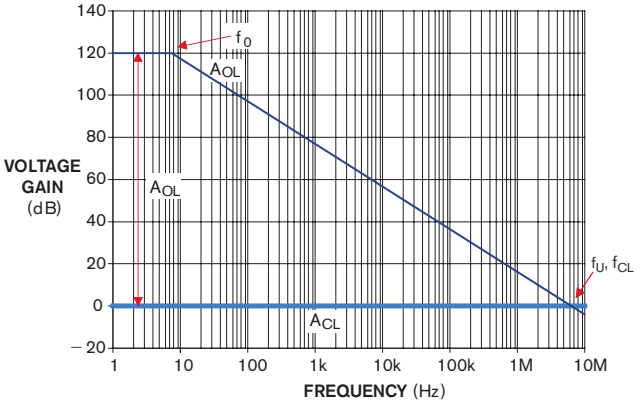

Figure 2 The open- and closed-loop-transfer function of the amplifier in **Figure 1** does not contain R_{IN} and C_{IN} as loads.

is greater than 20 dB/decade, the amplifier circuit will be marginally stable or completely unstable. For example, if the open-loop-gain curve, A_{OL}, is changing at −40 dB/decade, the amplifier circuit is unstable where the slope of the closed-loop-gain curve, A_{CL}, is zero at the intersection with the open-loop-gain curve.

You can evaluate the stability of the circuit in **Figure 1** with the op amp's open-loop-gain function, A_{OL} (**Figure 2**). The amplifier's dc open-loop gain is 120 dB. At approximately 7 Hz (f_0), the op amp's open-loop curve leaves 120 dB and progresses down at a rate of −20 dB/decade. As the frequency increases, this attenuation rate continues past 0 dB. The open-loop-gain curve, A_{OL}, crosses 0 dB at approximately 7 MHz (f_U). Because this curve represents a single-pole system, the crossover frequency, f_U, is equal to the amplifier's UGBW. This plot represents a stable system because the closure rate of the closed- and open-loop-gain curve is 20 dB/decade.

Figure 3 provides an accurate picture of the amplifier's performance minus the ADC's impact. Introducing the external RC on the op amp's output modifies the amplifier open-loop-gain curve.

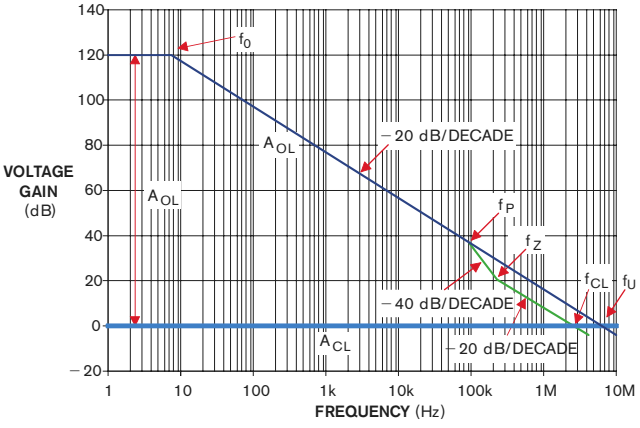

Figure 3 The pole, f_P, modifies the open-loop-gain curve of the amplifier by introducing a −20-dB/decade change to the −20-dB/decade slope of the open-loop-gain curve, making the slope −40 dB/decade. The added zero at frequency f_Z changes the open-loop-gain curve back to −20 dB/decade.

When evaluating the amplifier's open-loop-gain curve with R_{IN} and C_{IN} in the circuit, you need to include the effect of the amplifier's open-loop output resistance, R_O. The combination of R_O, R_{IN}, and C_{IN} modifies the open-loop-response curve by introducing one pole, f_p (**Equation 1**), and one zero, f_Z (**Equation 2**). The values of R_O, R_{IN}, and C_{IN} determine the corner frequency of f_P. The values of R_{IN} and C_{IN} determine the corner frequency of the zero.

$$f_P = \frac{1}{2\pi(R_0 + R_{IN})C_{IN}}. \quad (1)$$

$$f_Z = \frac{1}{2\pi R_{IN}C_{IN}}. \quad (2)$$

The pole, f_P, modifies the open-loop-gain curve of the amplifier by introducing a −20-dB/decade change to the already-−20-dB/decade slope of the open-loop-gain curve, making the slope equal to −40 dB/decade. The added zero at frequency f_Z changes the open-loop-gain curve back to −20 dB/decade.

In the interest of stability, the effects of f_Z must occur at a frequency lower than the intersect frequency of the open-loop- and closed-loop-gain curves (f_{CL}). **Figure 4** illustrates a condition in which f_Z is higher than the open-loop/closed-loop-intersection frequency, f_{CL}. In this situation, the amplifi-

TABLE 1 SAR-ADC WORST-CASE SETTLING TIME

ADC Resolution (bits)	**K** (time-constant multiplier to ½-LSB accuracy)
8	6.24
10	7.62
12	9.01
14	10.4
16	11.78
18	13.17

Note: Using worst-case values, V_{IN}= full-scale voltage, or 2^N, and V_{SH0}=0V.

TABLE 2 MEASUREMENT RESULTS OF ADS7886 DIGITAL OUTPUT WITH OPA364

Time (nsec)		60	120	180	240	300	360	420	480	540	600	660	720
	Bin	**Frequency** (Hz)											
Histogram (code)	2044	0	0	0	0	0	0	0	0	0	0	0	0
	2045	0	0	0	0	0	0	0	0	0	0	0	0
	2046	4095	4095	4095	4095	4095	4095	4091	4052	4007	4001	3981	4028
	2047	0	0	0	0	0	0	4	43	88	94	114	67
	2048	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0
Sigma		0	0	0	0	0	0	0.031242	0.101946	0.145027	0.149778	0.164531	0.126877
Mean		2046	2046	2046	2046	2046	2046	2046.001	2046.011	2046.021	2046.023	2046.028	2046.016
Peak-to-peak noise (code)		0	0	0	0	0	0	0.2062	0.67284	0.957181	0.988533	1.085904	0.837385
		0	0	0	0	0	0	0.000977	0.010501	0.02149	0.022955	0.027839	0.016361

Note: Resistance is 66.5Ω, and input capacitance is 1500 pF for the relatively stable circuit.

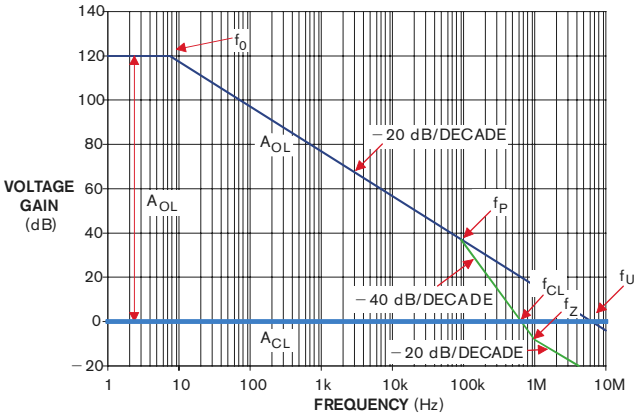

Figure 4 The pole and zero pair modify the amplifier's open-loop gain curve. R_{IN}, R_O, and C_{IN} generate the pole, causing a 40-dB/decade attenuation of the open-loop-gain plot. R_{IN} and C_{IN} generate the zero, which occurs after the frequency of the modified open-loop/closed-loop intersection (f_{CL}).

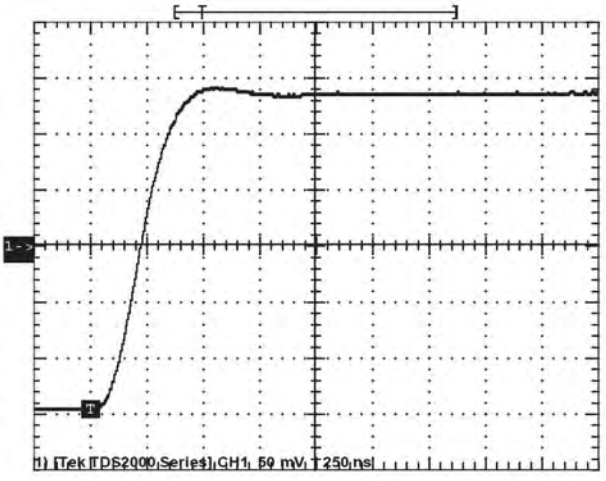

Figure 5 Measuring a 280-mV-p-p, small-signal step response (250 nsec/division, 50 mV/division) at V_{IN} with the OPA364 op amp yields an input resistance of 66.5Ω and an input capacitance of 1500 pF.

er circuit is marginally stable, with a phase margin of less than 45°. For this circuit, marginal stability can occur if the closure rate between the open- and closed-loop-gain curves is greater than 20 dB/decade.

You can find the modified closed-loop bandwidth, f_{CL}, by using the amplifier UGBW, the open-loop gain at the pole frequency (f_P), and the modified open-loop gain at the zero frequency (f_Z). The following **equations** describe the curves in **figures 2** and **3** and identify f_{CL}:

$$G_P = -20\log\left(\frac{f_P}{f_U}\right), \quad (3)$$

$$G_Z = G_P - 40\log\left(\frac{f_Z}{f_P}\right), \quad (4)$$

$$G_{CL} = G_Z - 20\log\left(\frac{f_{CL}}{f_Z}\right), \text{ if } G_Z > 0\ \text{dB}, \quad (5)$$

TABLE 3 MEASUREMENT RESULTS OF ADS7886 DIGITAL OUTPUT WITH OPA364

Time (nsec)		60	120	180	240	300	360	420	480	540	600	660	720
	Bin	Frequency (Hz)											
Histogram (code)	2044	0	0	0	0	0	0	0	0	0	0	0	0
	2045	0	0	0	0	0	0	0	0	0	0	0	0
	2046	3617	4070	4091	4095	4095	4084	3707	1708	1370	1654	2230	3278
	2047	465	25	4	0	0	11	387	2284	2528	2355	1833	817
	2048	13	0	0	0	0	0	1	103	197	86	32	0
		0	0	0	0	0	0	0	0	0	0	0	0
Sigma		0.334518	0.077905	0.031242	0	0	0.051765	0.294074	0.537307	0.548346	0.527598	0.514143	0.399682
Mean		2046.12	2046.006	2046.001	2046	2046	2046.003	2046.095	2046.608	2046.714	2046.617	2046.463	2046.2
Peak-to-peak noise (code)		2.207819	0.514174	0.2062	0	0	0.341651	1.940889	3.546228	3.619084	3.482145	3.393341	2.637901
		0.119902	0.006105	0.000977	0	0	0.002686	0.094994	0.608059	0.713553	0.617094	0.463248	0.199512

and

$$f_{CL} = (f_Z)\left(10^{(G_Z/20)}\right), \quad (6)$$

where G_P is the gain in decibels of the open-loop-gain curve at f_P, G_Z is the gain in decibels of the modified open-loop-gain curve at f_Z, and G_{CL} is the gain in decibels of the closed-loop-response frequency where the closed-loop response intersects with the modified open-loop-gain curve.

The frequency distance between the pole and zero must be equal to or less than one decade. This requirement is necessary because the phase change from zero negates the phase changes that the pole initiates. Note that the pole formula (**Equation 1**) includes R_{IN} and R_O; the formula for zero (**Equation 2**) includes only R_{IN}. If the distance between the pole and zero exceeds one decade, the phase response will not "recover" in time, and the output of the circuit will show more ringing.

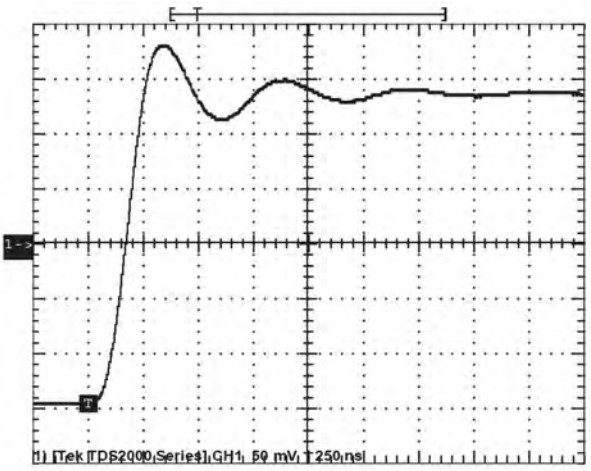

Figure 6 Measuring a 280-mV-p-p, small-signal step response (250-nsec/division, 50-mV/division scales) at V_{IN} with the OPA364 op amp yields an input resistance of 15Ω and an input capacitance of 1500 pF.

$$R_{IN} \geq \frac{R_O}{9}. \quad (7)$$

CORRECT VALUES OF R_{IN} AND C_{IN}

The primary purpose of capacitor C_{IN} is to charge the ADC's input sampling capacitor, C_{SH}, during the ADC's signal acquisition. With C_{IN} in the circuit, the amplifier should provide less than 5% of the charge to C_{SH} during signal acquisition, and C_{IN} provides more than 95% of the required charge. To ensure that C_{IN} provides most of the charge to the ADC's input during acquisition, C_{IN} should be greater than or equal to 20 times C_{SH} (**references 2** and **3**).

R_{IN} serves as the isolation resistor between the op amp and C_{IN}. R_{IN} assists in stabilizing the amplifier, but its secondary task is to ensure that the system can charge the input ADC capacitor in a timely fashion (**Reference 3**). The time-constant multiplier of this ADC acquisition time is K. As a first step, with these two variables and C_{IN},

$$R_{IN} \approx \frac{t_{ACQ}}{K \times C_{IN}}, \quad (8)$$

where t_{ACQ} is the ADC's acquisition time (**Reference 4**).

AMPLIFIER-FREQUENCY AND GAIN VALUES

As a first step to optimization, look at the C_{IN} and op-amp characteristics. During op-amp production, internal components can vary. Capacitances can change by as much as ±15%. Additionally, the op-amp transistor's transconductance can vary from ±5 to ±15%. So, if you are looking for a variation of f_U at 25°C with three times sigma, you can use ±20% as a good starting point.

It is good practice to use $f_{CL}=f_U/2$ and $f_Z=f_{CL}/2$ or $f_Z=f_U/4$ for good stability over different production lots. If these conditions are a concern, having G_Z equal to 6 dB or $f_Z=f_{CL}/2$ further stabilizes the system from production lot to production lot.

Using these gain and frequency points' definitions, you can make decisions about the best values for R_{IN} and C_{IN}. If you define G_Z as equal to 3 dB, then 0 dB=3 dB−20×log(f_{CL}/f_Z)

(**Equation 5**) or $f_{CL}=1.41\times f_Z(f_Z=f_{CL}/1.41)$. If you want $G_Z=6$ dB, then 0 dB=6 dB−20×log(f_{CL}/f_Z), or $f_{CL}=2\times f_Z(f_Z=f_{CL}/2)$.

PROOF OF CONCEPT

This theory is a good start, but proof of concept completes the picture. Two sample circuits tie this theory to reality. These designs use the OPA364 as the op amp with a UGBW of 6.45 MHz and open-loop output resistance, R_O, of 110Ω. Both designs also use a 1500-pF capacitor for C_{IN}. The target closed-loop bandwidth, f_{CL}, in the design is $f_U/2$, or 3.23 MHz, and the target frequency of added zero is $f_U/4$, or 1.61 MHz.

Two conditions are observable using an R_{IN} of 66.5Ω (Design 1, the relatively stable circuit) and 15Ω (Design 2, the marginally stable circuit). You can then observe the effects of a small-signal step response at the test point, V_{IN}. The op amps are in a buffer configuration, with a 1V/V closed-loop gain. The second series of tests uses the ADS7886 for the SAR ADC.

In the first design, R_{IN} is 66.5Ω. Combining the effects of C_{IN}, R_{IN}, and R_O produces a pole frequency, f_p (**Equation 1**), at 601 kHz with an open-loop gain, G_p (**Equation 3**), of 20.6 dB. This combination of C_{IN}, R_{IN}, and R_O also produces a zero, f_Z (**Equation 2**), at 1.596 MHz with an open-loop gain, G_Z (**Equation 4**), of 3.65 dB. **Figure 3** shows the system's Bode plot. **Figure 5** shows the response of V_{IN} when the noninverting input of the op-amp buffer sees a 280-mV-p-p, small-signal step response. The signal at V_{IN} is stable within 1 μsec. This condition is desirable for this SAR ADC.

In the second design, R_{IN} is 15Ω. With the values of R_{IN}, C_{IN}, and R_O, the pole frequency, f_p, is 849 kHz at an open-loop gain, G_p, of 17.6 dB. The zero frequency, f_Z, is 7.074 MHz with an open-loop gain, G_Z, of −19.22 dB. **Figure 4** shows the system's Bode plot. **Figure 6** shows the response of V_{IN} when the noninverting input of the op-amp buffer sees a 280-mV-p-p, small-signal step response.

This marginally stable test circuit generates an overshoot with ringing, which is undesirable. The ADS7886 produces an unstable and inaccurate result from the signal in **Figure 6**.

These measurements show how the system responds to an input step without the ADS7886 connected. You can expect similar results when the load changes with the ADS7886. Closing the ADS7886 sampling switch generates a kickback current. Adding the ADS7886 to the circuit makes it difficult to observe 12-bit-accurate changes with an oscilloscope. Therefore, you apply a new measurement technique.

The test begins with the addition of the ADS7886 to the circuit (**Figure 1**). This circuit applies a constant voltage at the noninverting input of the OPA364. Testing began with an ADS7886 acquisition time of 300 nesec and 4096 measurements; testing continued with an acquisition time of 60 nsec, again with 4096 measurements. The acquisition time continued to increase by increments of 60 nsec until the test was complete for both designs.

After collecting this data, calculations of sigma and mean values for every ADS7886 acquisition point yield the results in **tables 2** and **3**. In the **tables**, the top line identifies the additional acquisition for the ADS7886 beyond the initial acquisition time of 300 nsec from test to test. The far left column lists the output-data codes and the number of times these codes appear in the body of the **table**. The statistical summary of the body of both **tables** appears at the bottom.

The data shows that the stable design has a lower sigma and more consistent mean. The mean value of the unstable system has an error of more than 0.7 LSB, whereas the stable system has an error of less than 0.03 LSB.

DESIGNING THE ADC SYSTEM

Choosing the right op amp for the ADC is critical. Be sure to compare issues such as amplifier noise, bandwidth, and settling time to the ADC's SNR, SFDR (spurious-free dynamic range), input impedance, and sampling time. The primary purposes of capacitor C_{IN} are to provide charge to the ADC's input sampling capacitor, C_{SH}, during the ADC's signal-acquisition time and to offload the amplifier from dynamic activity from the ADC. The proper design equation when determining C_{IN} is:

$$20\times C_{SH} \le C_{IN} \le 60\times C_{SH}. \quad (9)$$

Determining this value allows you to calculate the new time-constant multiplier, K_1, with N equal to the number of ADC bits:

$$K_1 = \ln\left[\frac{2^{N+1}}{(C_{IN}/C_{SH}+1)}\right]. \quad (10)$$

As design requirements and ADC performances set up the ADC's acquisition times, calculate the frequency of the added zero, f_Z:

$$f_Z = \frac{K_1}{2\pi t_{ACQ}}. \quad (11)$$

After determining these quantities, verify that the system is stable with this **equation**:

$$f_Z \le \tfrac{1}{4} f_U. \quad (12)$$

With the frequency of the added zero and C_{IN}, determine the value of R_{IN} using the following two **equations**:

$$R_{IN} = \frac{1}{2\pi\times C_{IN}\times f_Z}. \quad (13)$$

$$R_{IN} \ge \frac{R_O}{9}. \quad (14)$$

Calculate the frequency of the added pole, f_P:

$$f_P = \frac{1}{2\pi\times(R_{IN}+R_O)\times C_{IN}}. \quad (15)$$

Check the gain of the added zero on the modified open-loop-gain curve. For a stable design, this value needs to be greater than or equal to 6 dB:

$$6\ \text{dB} \le G_Z = -20\log\left(\frac{f_P}{f_U}\right) - 40\log\left(\frac{f_Z}{f_P}\right). \quad (16)$$

Once the design process is complete, it is critical that you benchtest the circuit to verify stability. EDN

ACKNOWLEDGMENT

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AUTHORS' BIOGRAPHIES

Miro Oljaca is a senior applications engineer at Texas Instruments, where he is responsible for high-precision linear products focusing on industrial applications. Oljaca has more than 20 years of design experience in motor control and power conversion. He received bachelor's and master's degrees in electrical engineering from the University of Belgrade (Serbia) and is a member of AEI, CNI, IEE, and IEEE.

Bonnie Baker is a senior applications engineer at Texas Instruments and has been involved with analog and digital designs and systems for nearly 20 years. Baker has written more than 250 articles, design notes, and application notes. She is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers *and the co-author of* Circuit Design: Know It All *and* Analog Circuits: World-Class Designs. *In addition, Baker writes the column "Baker's Best" for* EDN.